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AN-8009

FMS6146 Evaluation Board Application Note

Description

The FMS6146 evaluation board provides a flexible base for evaluating the performance of the FMS6146. The board operates from a standard supply voltage of +5V \pm 5%.

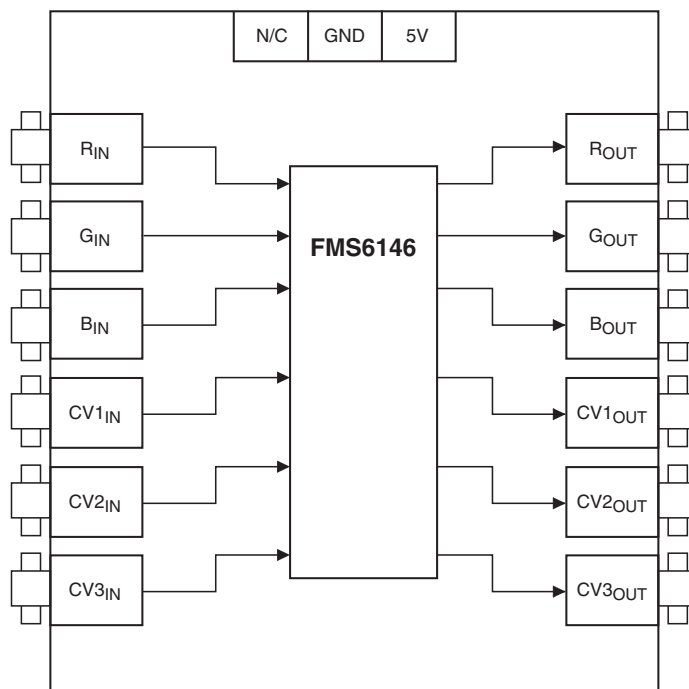
The FMS6146 Low Cost Video Filter (LCVF) is intended to replace passive LC filters and drivers with a low-cost integrated device. Six 4th order filters provide improved image quality compared to typical 2nd and 3rd order passive solutions.

Applications

- Cable set top boxes
- Satellite set top boxes
- DVD players
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

For a complete description of the FMS6146 please refer to the FMS6146 data sheet.

Evaluation Board Block Diagram



Evaluation Kit Contents

The FMS6146 Evaluation Kit contains the following items:

- AN-8009 – FMS6146 Evaluation Board Application Note
- The latest revision of the FMS6146 data sheet, which also can be obtained from <http://www.fairchildsemi.com>.
- Fully functional FMS6146 eval board
- Female power connector

Board Setup and Test

Use the following procedure to verify that the FMS6146 eval board is functional. This only verifies functionality. These instructions do not test any parameters outlined in the datasheet. The following test equipment is necessary to test the FMS6146 eval board.

- One power supply +5V $\pm 5\%$, 250mA
- One high resolution CRT monitor (2 channel with RGB)
- One NTSC or PAL video signal source capable of generating necessary outputs (RGB, Y, C & Composite)
- One video measurement set (VM700)
- Assorted video cables

DO NOT turn on power supply until all connections are completed.

1. Set the power supply to 5.0V. Connect the power supply to the input voltage terminals of the evaluation board.
2. Connect the R_{OUT} signal from the signal source to the R_{IN} connector on the FMS6146 eval board.
3. Connect the G_{OUT} signal from the signal source to the G_{IN} connector on the FMS6146 eval board.
4. Connect the B_{OUT} signal from the signal source to the B_{IN} connector on the FMS6146 eval board.
5. Connect R_{IN} of the monitor to the R_{OUT} connector on the FMS6146 eval board.
6. Connect G_{IN} of the monitor to the G_{OUT} connector on the FMS6146 eval board.
7. Connect B_{IN} of the monitor to the B_{OUT} connector on the FMS6146 eval board.
8. Turn on the power supply.
9. Verify monitor is setup to receive RGB signals.
10. Verify test pattern that is produced from the generator is the same as the pattern on the monitor screen.
11. Turn off the power supply
12. Connect CV_{OUT} of the monitor to the CV1_{IN} connector on the FMS6146 eval board.
13. Connect CV_{IN} of the monitor to the CV1_{OUT} connector on the FMS6146 eval board.
14. Turn on the power supply.
15. Verify monitor is setup to receive composite video.
16. Verify test pattern that is produced from the generator is the same as the pattern on the monitor screen.
17. Turn off the power supply.
18. Connect CV_{OUT} of the monitor to the CV2_{IN} connector on the FMS6146 eval board.
19. Connect CV_{IN} of the monitor to the CV2_{OUT} connector on the FMS6146 eval board.
20. Turn on the power supply.
21. Verify monitor is setup to receive composite video (if not done previously).
22. Verify test pattern that is produced from the generator is the same as the pattern on the monitor screen.
23. Turn off the power supply.
24. Connect CV_{OUT} of the monitor to the CV3_{IN} connector on the FMS6146 eval board.
25. Connect CV_{IN} of the monitor to the CV3_{OUT} connector on the FMS6146 eval board.
26. Turn on the power supply.
27. Verify monitor is setup to receive composite video (if not done previously).
28. Verify test pattern that is produced from the generator is the same as the pattern on the monitor screen.
29. Functional test is now complete.

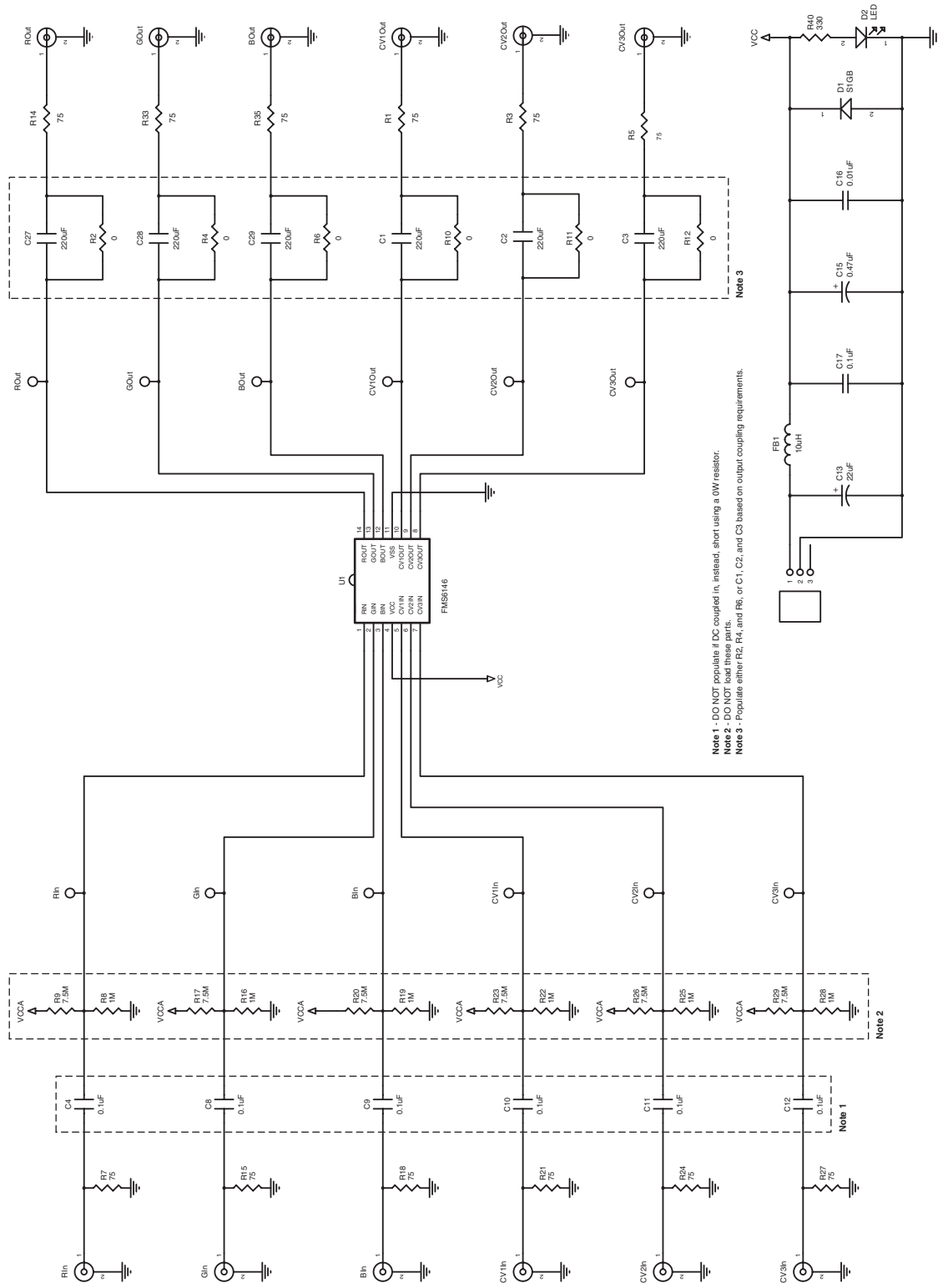


Figure 1. FMS6146 Schematic Diagram

Bill of Materials

Item	Quantity	Reference	Part
1	12	CV1OUT, CV1IN, CV2OUT, CV2IN, CV3OUT, CV3IN, ROUT, RIN, GOUT, GIN, BOUT, BIN	BNC Connectors
2	6	C1, C2, C3, C27, C28, C29	220 μ F
3	7	C4, C8, C9, C10, C11, C12, C17	0.1 μ F
4	1	C13	22 μ F
5	1	C15	0.47 μ F
6	1	C16	0.01 μ F
7	1	D1	S1GB
8	1	D2	LED
9	1	FB1	10 μ H
10	1	JP1	PWRCON3
11	12	R1, R3, R5, R7, R14, R15, R18, R21, R24, R27, R33, R35	75 Ω
12	6	R2, R4, R6, R10, R11, R12	0 Ω
13	6	R8, R16, R19, R22, R25, R28	1M Ω
14	6	R9, R17, R20, R23, R26, R29	7.5M Ω
15	1	R40	330 Ω
16	1	U1	FMS6146

Applications

The FMS6146 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required. The outputs can drive AC or DC-coupled single (150 Ω) or dual (75 Ω) loads. DC-coupling the output removes the need for output coupling capacitors. The input DC levels will be offset approximately +280mV at the output. The FMS6146 Low Cost Video Filter (LCVF) provides 6dB gain from input to output. In addition, the input will be slightly offset to optimize the output driver performance. The FMS6146 provides an internal diode clamp to support AC-coupled input signals. If the input signal does not go below ground, the input clamp will not operate. This allows DAC outputs to directly drive the FMS6146 without an AC coupling capacitor (usually 220 μ F). The input level set by the clamp combined with the internal DC offset will keep the output within its acceptable range.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance and thermal characteristics. The FMS6146DEMO is a 4-layer board with a full power and ground plane. Following this layout configuration will provide the best performance and thermal characteristics. For optimum results, follow the steps below as a basis for high frequency layout.

- Include 10 μ F and 0.1 μ F ceramic bypass capacitors
- Place the 10 μ F capacitor within 0.75 inches of the power pin
- Place the 0.1 μ F capacitor within 0.1 inches of the power pin
- For multi-layer boards, use a large ground plane to help dissipate heat
- For 2 layer boards, use a ground plane that extends beyond the device by at least 0.5 inches
- Minimize all trace lengths to reduce series inductance

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