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Majid Dadafshar, Field Application Engineering
Fairchild Semiconductor Corporation
www.fairchildsemi.com

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Low Drop Out, Phase Margin, and Stability

Summary

Low drop-out (LDO) regulators are one of the basic building blocks of most power supplies used in today's electronics. Their ease of use, low cost, and small size makes them ideal in portable and handheld applications. They are available in wide variety of voltage & current levels with their primary function, to provide power to low-voltage digital circuits. The only other necessary components are external capacitances, which, in conjunction with the LDO, create a complete power solution. This application note reviews the effect of these components and their phase shifts on the LDO's loop stability and show how to tailor the compensation to obtain a stable circuit.

Analysis

The linear regulator operates by using a voltage-controlled current source to force a fixed voltage at the regulator output terminal. The control circuitry must monitor the output voltage and adjust the current source, as required by the load, to hold the output voltage at the desired value. The design limit of the current source defines the maximum load current the regulator can source and maintain regulation.

The main use of LDO regulators is to convert an input voltage into a stable DC output voltage and maintain that voltage through a range of load and line variation. The drop-out voltage, which is the minimum voltage across any regulator to maintain the Vo within its regulation band, is comparably lower than standard regulators. This allows the output regulation to cover a wider input voltage range during battery discharge, desirable in portable applications.

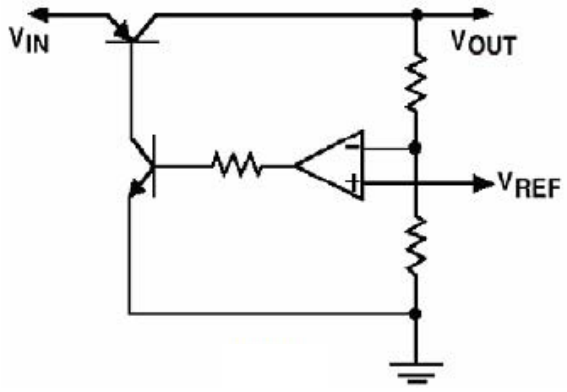

Figure 1. V_{OUT} Sensed Through Divider Network

The output voltage is sensed through the divider network, shown in Figure 1, which is fed into the inverting error amplifier pin and compared to the V_{REF} on the non inverting pin of the error amplifier. Output voltage can be set at any level by either changing the resistive divider or changing the reference voltage, V_{REF}.

The error amplifier supplies current as needed by the main switch to maintain the output voltage at a correct level. As the load in a digital circuit changes, it changes the amount of current to the LDO, which requires time for the output to correct itself, defined by transient response time. Transient response indicates how fast the loop adjusts the output voltage to the steady-state nominal value.

In general, the stability of LDO is the same as any other operational amplifier and the inverting nature of the feedback forces the loop to start with -180 degrees of phase shift. When an LDO is connected to a load and output capacitance, these added components create some additional poles and zeros and, as the signal goes through a feedback loop, it experiences some gain and phase changes, which change the overall phase shifts within the loop. Attention must be paid to proper selection of these components and placement of the added zero at a specific frequency to obtain and maintain a stable loop.

Looking at the impedance of any capacitor, notice that it has a capacitive behavior at low frequency; it becomes resistive near its resonant frequency, where the Xc=Xl, and becomes inductive at some higher frequency.

It is, therefore, possible to model a real capacitor, in series with a resistor (ESR) and inductance (ESL), and study the combined effects to understand the output voltage signal. As the load change occurs, there is a voltage drop across each of these parasitic elements, which affects the transient response in different ways.

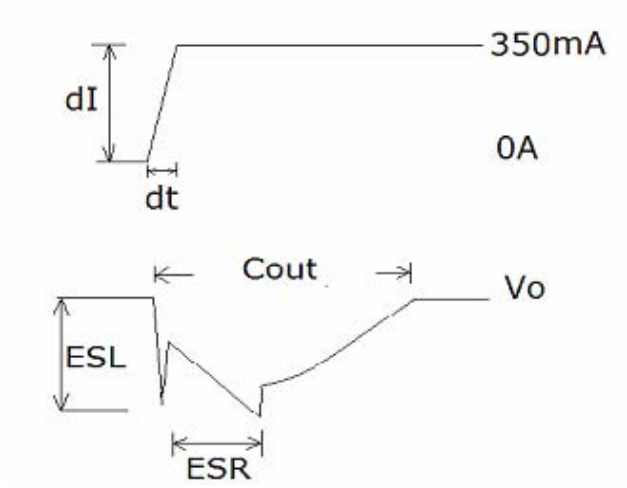

Figure 2. Parasitic Effects

Figure 2 shows the effect of each parasitic element on the output voltage. The first peak is the effect of ESL, which, for a given current pulse (dI=350mA) and a given rise time (dt), causes a voltage drop across the inductance (ESL) equal to V=ESL*(di/dt). This value can have different peak levels, based on the ESL value and traces on the PCB, forcing the designer to pay a close attention to the layout in optimizing and reducing the effect of parasitic inductances.

When output capacitance (C_{OUT}) starts to supply the dI current, there is a voltage drop (ESR*dI) with a time width that is a function of how fast the loop responds. Since the voltage change across C_{OUT} is a function of dI/C_{OUT} or (I=C.dv/dt), the amount of cap value changes the dip voltage and duration of the voltage sag. There is also a certain time after a load change that the loop needs to adjust the current demand and bring back the voltage to a nominal value, which is dominated by the value of C_{OUT}.

Once C_{OUT} and its parasitic effect on the output voltage ripple are understood, examine the affect on loop and compensation. LDOs usually have an internal fixed pole at low frequency of near 100Hz, which is set in the error amplifier section with some DC gain, such as 80db. The main pass transistor's parasitic capacitance and its driver usually have an additional pole at few hundreds of KHz, such as 275KHz. The combination of the output load impedance and output capacitance creates a pole (211Hz) that can be calculated using the equation:

$$\text{LoadPole} := \frac{1}{2 \cdot \pi \cdot \text{RLoad} \cdot \text{Cout}}$$

The two poles caused by the LDO and load force the total phase shift to reach -180 degrees and roll off the gain with a slope of -40db/decade. There is a need for a zero to reduce the excess negative phase shift of -180 degrees to avoid the -180-degree phase shift, plus -180 degrees for the inverting amplifier, becoming 360 degrees and creating a positive feedback loop (a sign of instability) instead of the needed negative feedback. The job of the zero, with its +90 degrees of phase shift, is to cancel the effect of one of the two poles.

$$\text{Fzero} := \frac{1}{2 \cdot \pi \cdot \text{Cout} \cdot \text{ESR}}$$

Figure 3 shows the overall and individual phase shifts for all poles and the zero within the loop with the respective phase shifts and roll-off frequencies. The importance of the zero caused by ESR, its value, and the crucial placement at a specific frequency is illustrated by Figure 3.

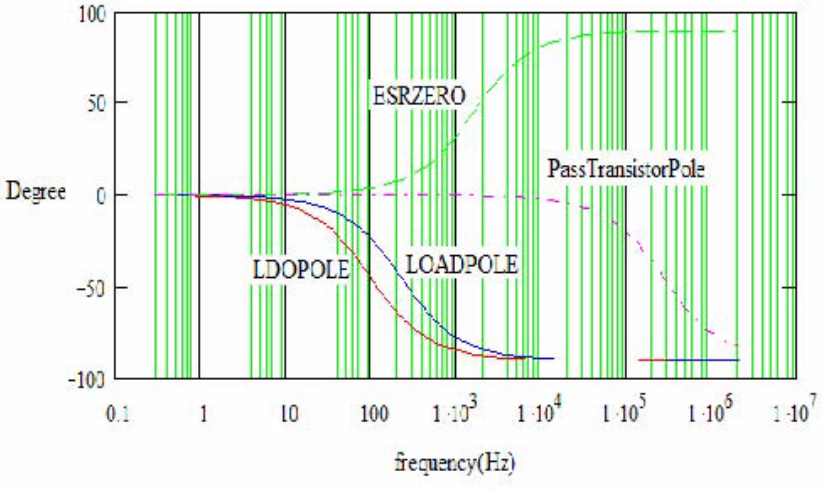

Figure 3. Individual Phase Shifts

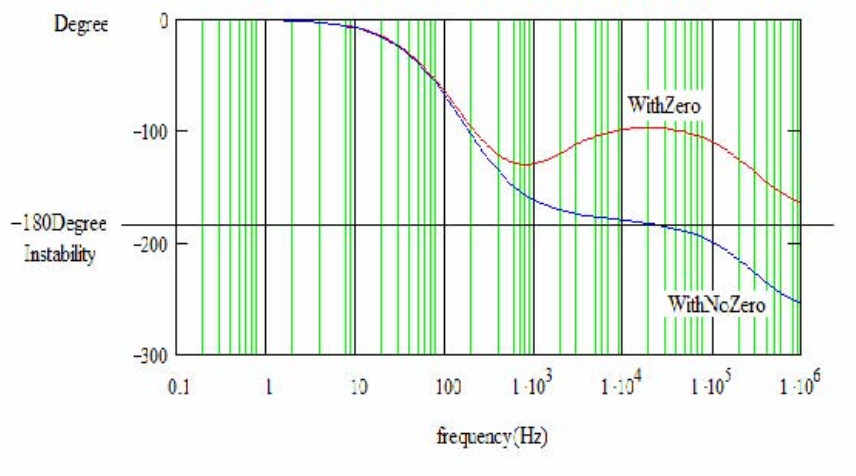

Figure 4. Total Phase Shift

Figure 4 shows the phase shifts with and without the ESR. Without a zero, the total phase shift is approaching the -180 degree line, a clear sign of instability. When a zero is added, it forces the added gain in phase, boosting the total phase shift away from the -180 degree line.

The phase margin is a critical factor in determining whether a loop is stable, which is defined as the difference between the total phase shift of the feedback signal and the -180 degree line, at the frequency where the loop gain is equal to 0db. With all added phase shifts, the overall open-loop gain must drop to less than zero decibels.

The graphs in Figure 5 show how phase margin and BW for a given ESR range (0.1-1.0Ω) change and the effect on the loop. This is the main reason suppliers provide graphs of the range of ESR values necessary for a stable loop.

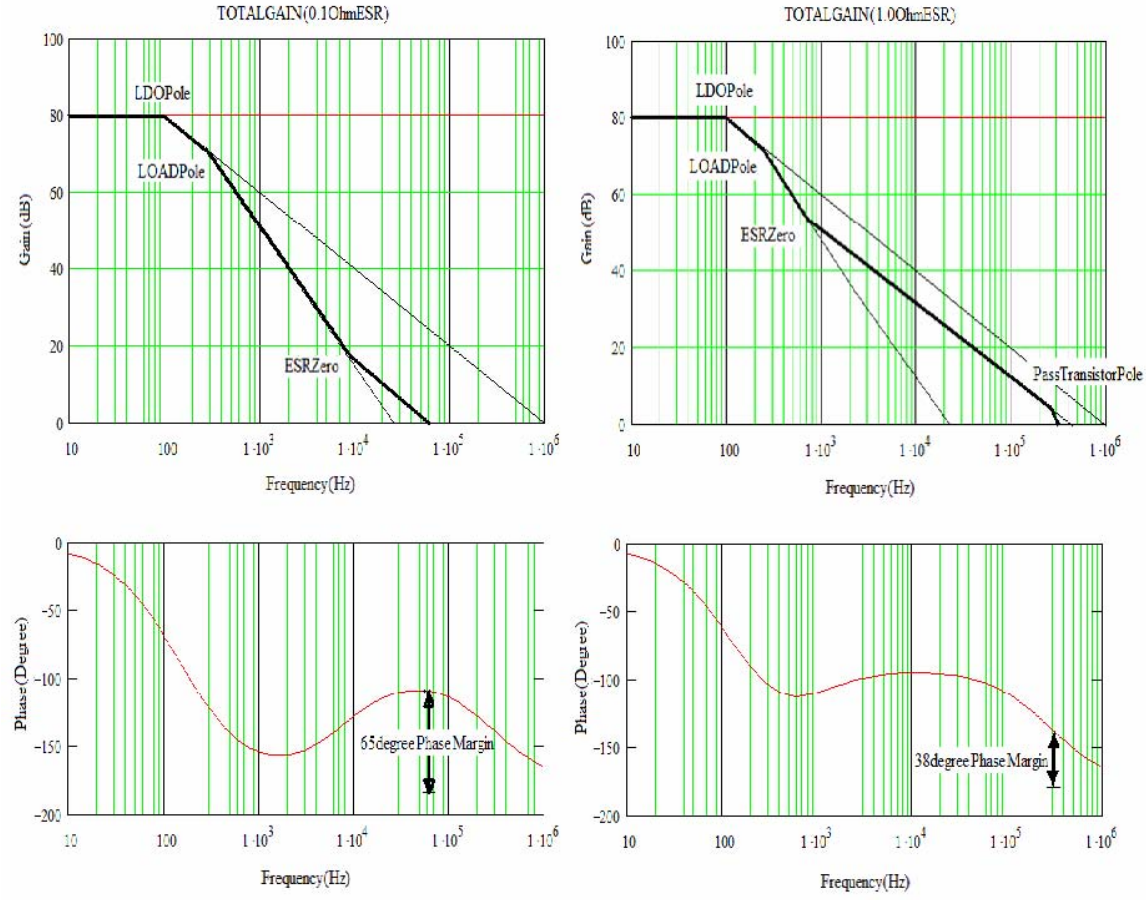

Figure 5. Phase Margin for ESR Range 0.1 – 1.0Ω

Figure 5 shows that .1Ω of ESR provides adequate phase margin at 0dB, but higher ESR optimizes the loop further. ESR of .34Ω, as shown in Figure 6, results in a more robust phase characteristic over the entire frequency spectrum and pushes the phase slightly higher (at blue circle in graph), causing a slight reduction of phase margin at 0db.

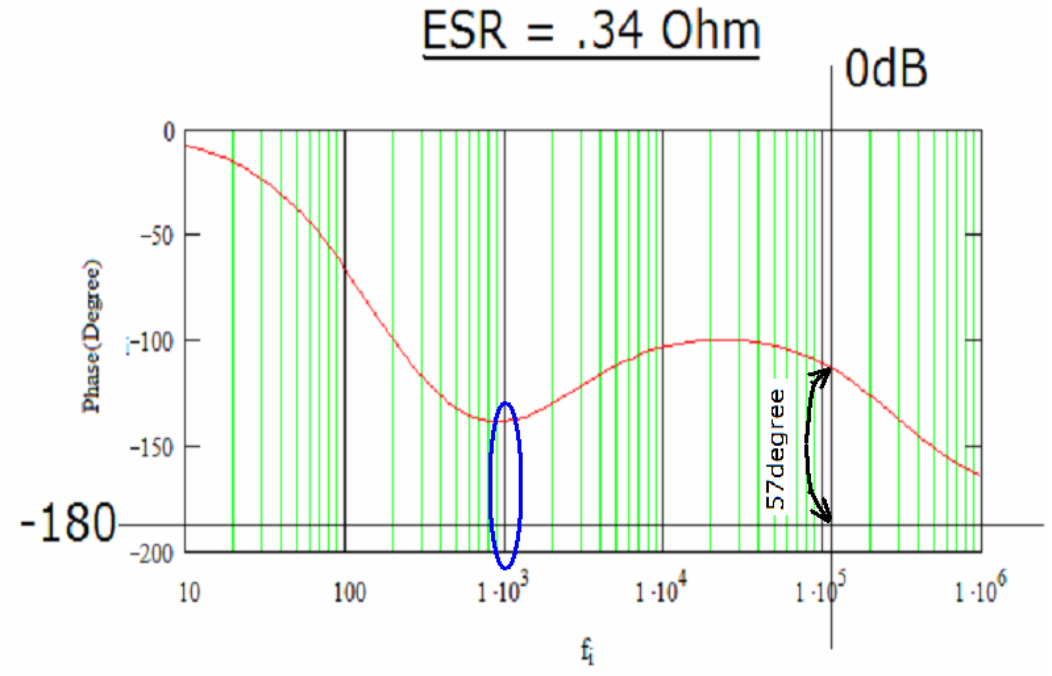

Figure 6. ESR of .34Ω Impacting Phase Margin

Example

For example, if: V_{IN} = 5V and V_{OUT} = 1.2V, the maximum ESR for a stable loop would need to be below 800m Ω of resistance, which needs to be maintained through temperature variation.

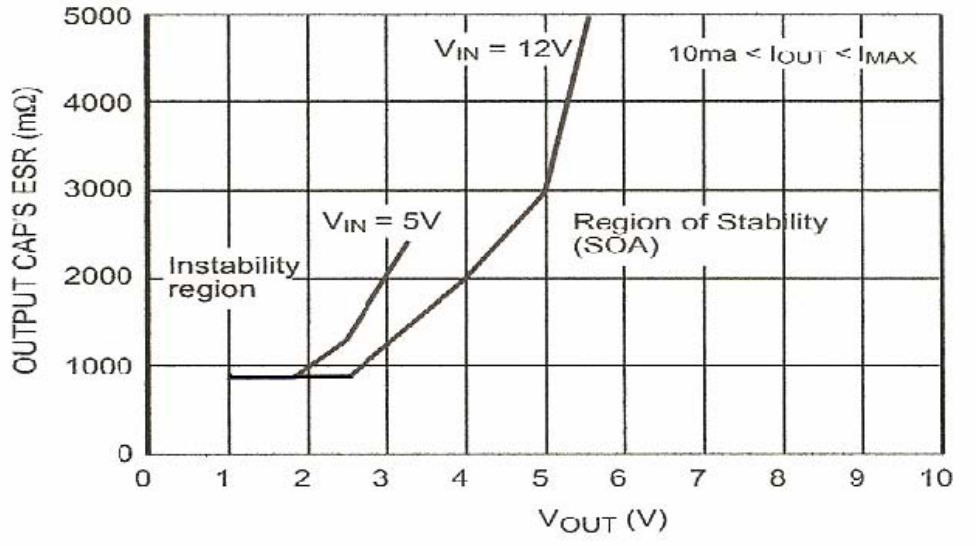

Figure 7. Stability Region (SOA) vs. ESR of the C_{OUT}

While LDOs are simple to use, attention should be given to proper selection of the components connected to them. For a stable loop, the gain must cross below 0dB before the phase shift reaches 180 degrees. The ESR value, which is often neglected by designers, can be used to effectively tailor the loop response with a proper phase and gain margin.

The effect of temperature on the ESR and types of capacitances also need to be considered. Select output capacitance to have an ESR value such that, when the closed-loop gain is greater than or equal to 1, the closed-loop phase never reaches near 30- 35 degrees of the remaining 180 degrees. Systems with less than 30 degrees of phase margin respond with an under-damped behavior when exposed to a small transient and shows signs of oscillation at their outputs.

Conclusion

Careful consideration of the forces that degrade stability and the parasitic effect of external components can result in designs that compensate for these factors and provide a complete power solution robust enough for the load and temperature variations of the ultra-portable applications in today's market.

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