

# LC898240

## Advance Information

# High Efficient Stepper Motor Controller

### Overview

The LC898240 is a current controller IC for a stepper motor, co-working with a conventional driver. It provides additional functions to a stepper motor control system. The drive current of a motor coil is adopted for the motor load, so that minimize the waste of power. By this current control, the stepper motor moves smoothly. And, it gives higher efficiency power consumption, lower acoustic noise, lower vibration and lower heat generation.

The LC898240 also provides speed acceleration profile control function and step-out detection/prevention. These functions can be configured by the registers through an SPI serial port interface flexibly. The preset parameters and configuration can be stored to the companion non-volatile memory.

The LC898240 consists of the monitor inputs from motor terminal, serial port inter face, the step control signal inputs from a microprocessor and the outputs to a stepper motor driver. The topology of a microprocessor, a stepper motor driver and LC898240, can be arranged to match various drivers and system architecture. Thus, it can be used as an interface converter between a microprocessor and a driver with the advanced control functions.

### Features

- Unipolar and bipolar motor applicable
- Supported excitation mode:
  - Half step
  - Quarter step
  - 1/8 step
  - 1/16 step
  - Full step (high efficient function not applicable)
- SPI interface for the motor control and setting
- Interface for the driver control
- Non-volatile memory (E2PROM)
  - Setting of the controller
  - Acceleration curve: 9 curves, 440 steps for each

### Recommended Stepper Motor Driver

- LV8726TA
- LV8736V
- LV8740V
- STK672-6XXX
- STK672-4XXX

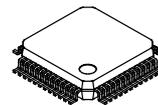
### Typical Applications

- Multi-Function Printer
- Consumer



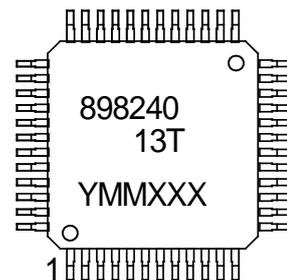
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### PACKAGE PICTURE



SQFP48  
0.5mm pitch

### MARKING DIAGRAM



Y: Year  
MM: Month  
XXX: ID

### ORDERING INFORMATION

Ordering Code:  
LC898240-2H (tray)  
LC898240-WH (reel)

Package  
SQFP48  
(Pb-Free / Halogen Free)

Shipping (Qty / packing)  
1250 / Tray  
1000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.  
[http://www.onsemi.com/pub\\_link/Collateral/BRD8011-D.PDF](http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

# LC898240

## LC898240 BLOCK DIAGRAM

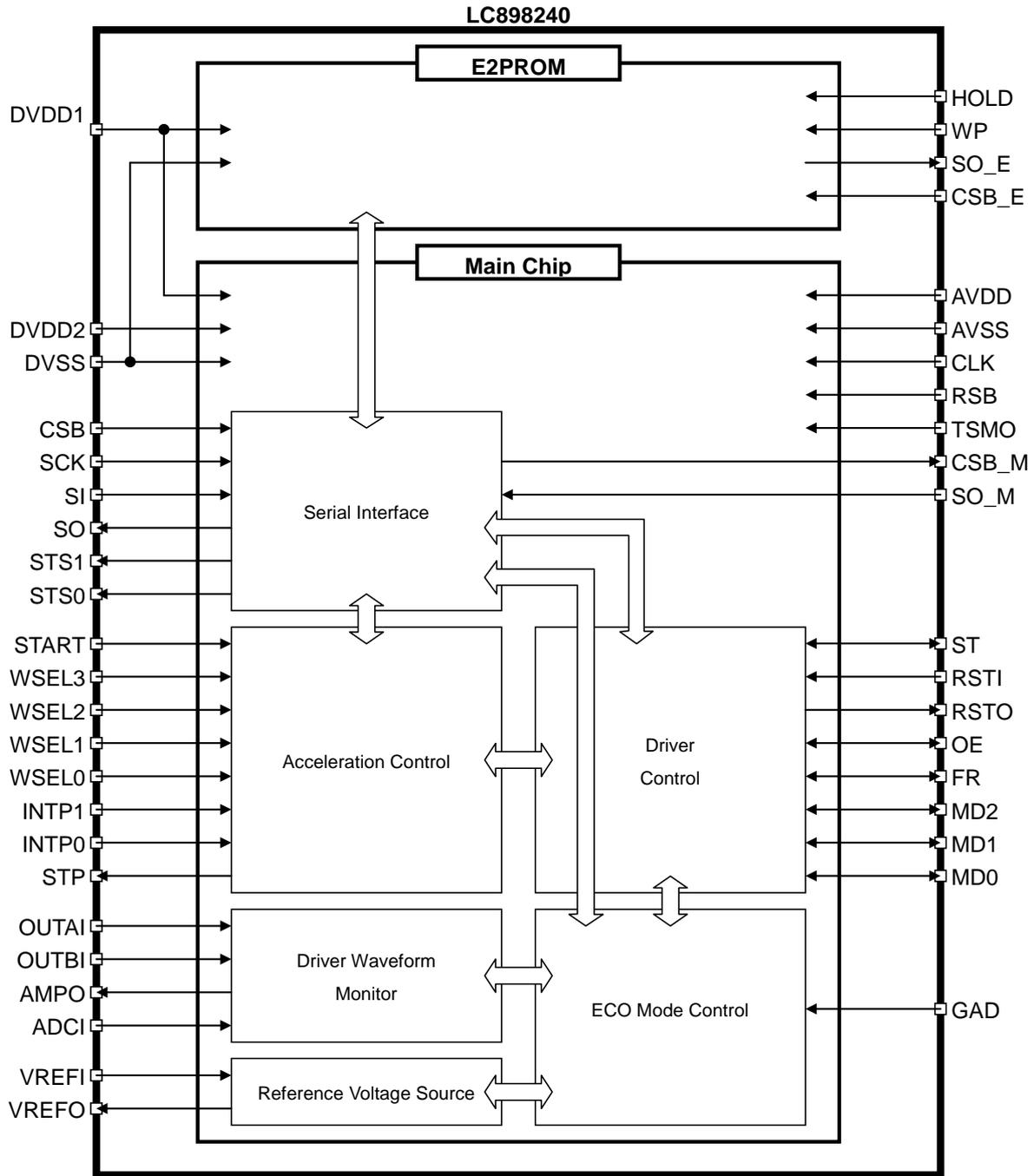


Figure 1 LC898240 Block Diagram

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## APPLICATION BLOCK DIAGRAM

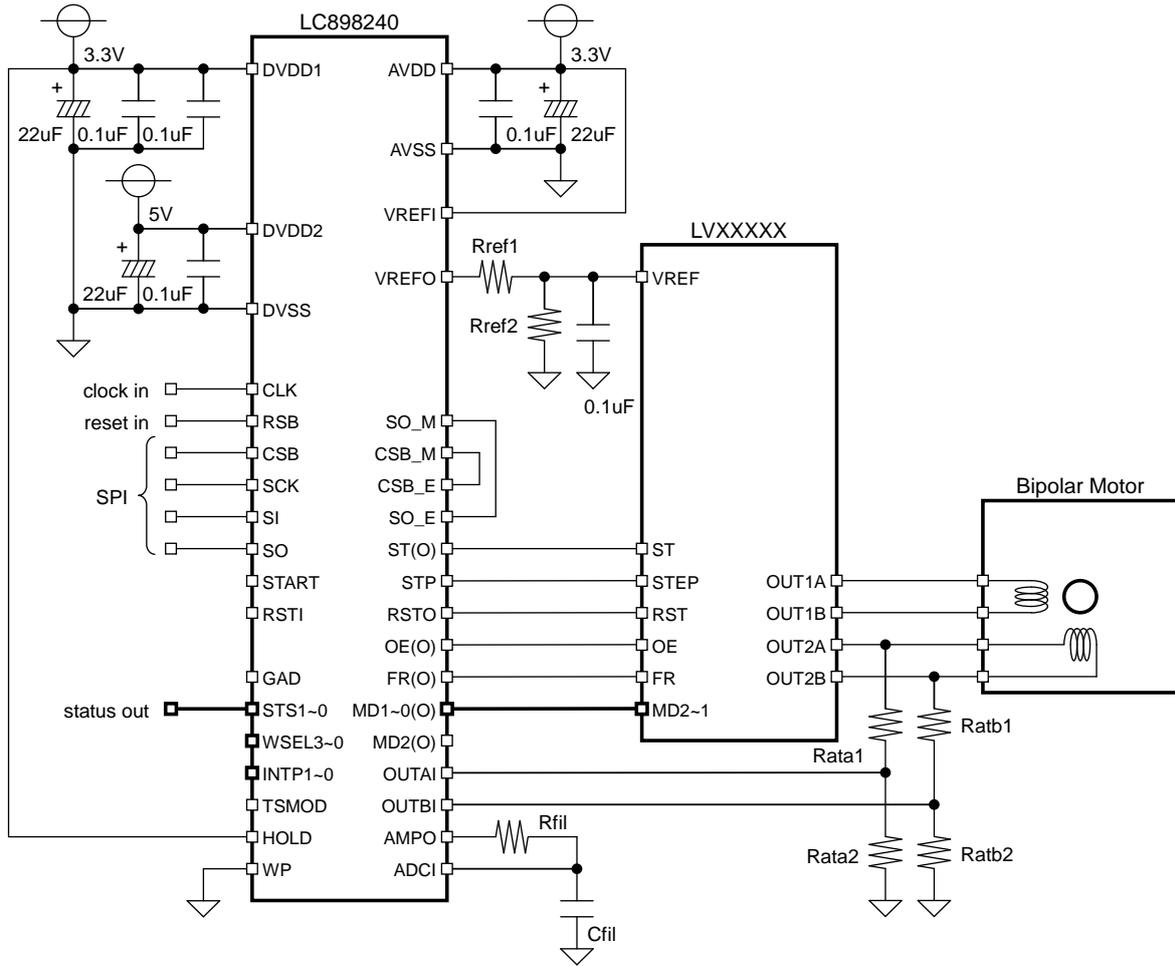


Figure 2 Example of SPI control for IO port control driver

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## PIN ASSIGNMENTS

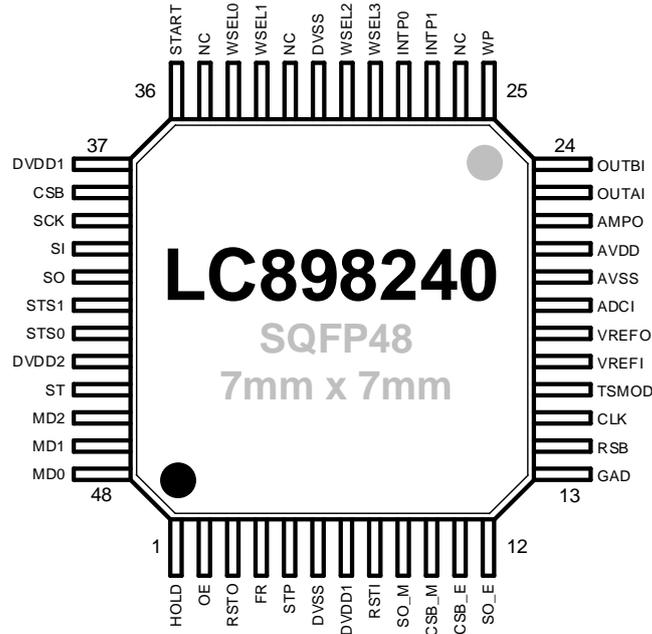


Figure 3: LC898240 Pinout

NUMBER	NAME	TYPE	NUMBER	NAME	TYPE
1	HOLD	I	48	MD0	B(I)
2	OE	B(I)	47	MD1	B(I)
3	RSTO	O	46	MD2	B(I)
4	FR	B(I)	45	ST	B(I)
5	STP	O	44	DVDD2	P
6	DVSS	P	43	STS0	O
7	DVDD1	P	42	STS1	O
8	RSTI	I	41	SO	O
9	SO_M	I	40	SI	I
10	CSB_M	O	39	SCK	I
11	CSB_E	I	38	CSB	I
12	SO_E	O	37	DVDD1	P
13	GAD	I	36	START	I
14	RSB	I	35	NC	-
15	CLK	I	34	WSEL0	I
16	TSMOD	I	33	WSEL1	I
17	VREFI	I	32	NC	-
18	VREFO	O	31	DVSS	P
19	ADCI	I	30	WSEL2	I
20	AVSS	P	29	WSEL3	I
21	AVDD	P	28	INTP0	I
22	AMPO	O	27	INTP1	I
23	OUTAI	I	26	NC	-
24	OUTBI	I	25	WP	I

Where,

- I : input
- O: output
- B(I) : bidirectional (input at reset)
- B(O) : bidirectional (output at reset)
- P: power supply

Termination of unused pins

- O: open
- I : pull-up or pull-down if no on-chip pull-up/down
- B: open (on-chip pull-down installed)

## PIN DESCRIPTION

1. HOLD  
Hold E2PROM. It must be connected to DVDD1.  
For more detail, see the E2PROM datasheet.
2. OE  
Output Enable  
For IO port control mode:
  - bit OERST = 0: OE acts as an input.
  - bit OERST = 1: OE acts as an output with respect to the pin ST transparently.
 For register control mode:
  - OE outputs the value of the bit OE\_REG.
3. RSTO  
Driver Reset Output  
To force synchronization of the step position with the driver, the driver reset pulse is output once an electrical cycle, while the bit RSTAD is set 1.  
For IO port control mode:
  - RSTO outputs with respect to the pin RSTI transparently.
 For register control mode:
  - RSTO outputs the value of the bit RST\_REG.
4. FR  
Rotation Direction  
For IO port control mode:
  - Input
 For register control mode:
  - FR outputs the value of the bit FR\_REG.
5. STP  
Step Pulse Output
6. DVSS  
Digital Ground
7. DVDD1  
Power Supply for the E2PROM and the Digital Portion of the Main Chip
8. RSTI  
Driver Reset Input for IO Port Control Mode  
For register control mode, it is ignored.
9. SO\_M and 12. SO\_E  
E2PROM output. They must be connected on a board.
10. CSB\_M and 11. CSB\_E  
E2PROM chip select pins. They must be connected on a board.
13. GAD  
High Efficient Current Control Mode  
The adaptive motor current control mode is enabled by GAD = H or the bit GAD\_REG = 1.
14. RSB  
System Reset Input  
LC898240 is reset by RSB = L. After the reset is released, it will start the E2PROM data download to the registers.
15. CLK  
Clock Input  
Frequency range is from 840kHz through 10MHz
16. TSMOD  
Test Mode  
It must be connected to DVSS or open.
17. VREFI  
Reference Voltage Input  
It must be connected to AVDD.
18. VREFO  
Current Control Reference Voltage Output
19. ADCI  
ADC Input
20. AVSS  
Ground of the Analog Portion
21. AVDD  
Power Supply for the Analog Portion
22. AMPO  
Amplifier Output
23. OUTAI and 24. OUTBI  
Motor Signal Input
25. WP  
Write Protection of E2PROM
26. NC, 32. NC and 35. NC  
No Connection
27. INTP1 and 28. INTP0  
Interpolation Setting for the Acceleration Curve  
For IO port control mode:
  - INTP[1:0] = 0h: not interpolation
  - INTP[1:0] = 1h: interpolate 1 point between the steps based on E2PROM data
  - INTP[1:0] = 2h: interpolate 3 point between the steps based on E2PROM data
  - INTP[1:0] = 3h: interpolate 7 point between the steps based on E2PROM data
 For register control mode, it is ignored.

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### 29. WSEL3, 30. WSEL2, 33. WSEL1 and 34. WSEL0

Acceleration Curve Selection

For IO port control mode:

- WSEL[3:0] = 0h: the acceleration curve #0
- WSEL[3:0] = 1h: the acceleration curve #1
- WSEL[3:0] = 2h: the acceleration curve #2
- WSEL[3:0] = 3h: the acceleration curve #3
- WSEL[3:0] = 4h: the acceleration curve #4
- WSEL[3:0] = 5h: the acceleration curve #5
- WSEL[3:0] = 6h: the acceleration curve #6
- WSEL[3:0] = 7h: the acceleration curve #7
- WSEL[3:0] = 8h: the acceleration curve #8
- WSEL[3:0] = 9h - Fh: N.A.

### 31. DVSS

Digital Ground

### 36. START

Motor Rotation Control

The bit STPSEL = 0: START acts as the step pulse input

The bit STPSEL = 1: START acts as the start/stop command input

### 37. DVDD1

Power Supply for the E2PROM and the Digital Portion of the Main Chip

### 38. CSB, 39. SCK, 40. SI and 41. SO

SPI Interface

### 42. STS1 and 43. STS0

Status Output of LC898240

### 44. DVDD2

Power Supply for the Digital Portion of the Main Chip

### 45. ST

Driver Standby

For IO port control mode:

- The bit DERST = 0: ST signal input
- The bit DERST = 1: ST signal input to output to OE

For register control mode:

- ST outputs the value of the bit ST\_REG.
- For the unipolar driver STK672-XXXX, this pin must be open.

### 46. MD2, 47. MD1 and 48. MD0

Mode Switch

For IO port control mode: MD signal input

For register control mode: the value of the register MD\_REG is output.

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## ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter		Pins	Ratings	Unit
Supply voltage		DVDD1	-0.3 to 4.6	V
		DVDD2	-0.3 to 6.0	V
		AVDD	-0.3 to 4.6	V
Input/output voltage	$V_{INd1}, V_{OUTd1}$		-0.3 to DVDD1 + 0.3	V
	$V_{INd1t}$		-0.3 to 6.0	V
	$V_{INd2}, V_{OUTd2}$		-0.3 to DVDD2 + 0.3	V
	$V_{INa}, V_{OUTa}$		-0.3 to AVDD + 0.3	V
Input/output current	$I_i, I_o$		±20	
Storage temperature	$T_{stg}$		-55 to 125	°C
Operating ambient temperature	$T_{opg}$		-40 to 85	°C

1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## ELECTRICAL CHARACTERISTICS $T_a: -40$ to $85^\circ\text{C}$ (Note 2)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply-voltage range	DVDD1	$ DVDD1 - AVDD  \leq 0.3$	3.0	3.3	3.6	V
	DVDD2	$DVDD1 \leq DVDD2 + 0.3$ $AVDD \leq DVDD2 + 0.3$	3.0	3.3	5.5	V
		$ DVDD1 - AVDD  \leq 0.3$	3.0	3.3	3.6	V
<b>DIGITAL INPUTS (HOLD, WP, CSB_E)</b>						
High level input voltage	$V_{IH}$		$0.7 \times DVDD1$		DVDD1	V
Low level input voltage	$V_{IL}$		0		$0.3 \times DVDD1$	V
<b>DIGITAL INPUTS (CLK)</b>						
High level input voltage	$V_{IH}$		$0.7 \times DVDD1$		5.5	V
Low level input voltage	$V_{IL}$		0		$0.2 \times DVDD1$	V
<b>DIGITAL INPUTS (RSB, RSTI, GAD, TSMOD, START, SO_M, WSEL3, WSEL2, WSEL1, WSEL0, INTP1, INTP0)</b>						
High level input voltage	$V_{IH}$		$0.75 \times DVDD1$		5.5	V
Low level input voltage	$V_{IL}$		0		$0.15 \times DVDD1$	V
<b>DIGITAL INPUTS (CSB, SCK, SI, OE, FR, ST, MD2, MD1, MD0)</b>						
High level input voltage	$V_{IH}$		$0.75 \times DVDD2$		DVDD2	V
Low level input voltage	$V_{IL}$		0		$0.15 \times DVDD2$	V
<b>DIGITAL OUTPUTS (SO_E)</b>						
High level output voltage	$V_{OH}$	$I_{OH} = -2\text{mA}$	$0.8 \times DVDD1$			V
Low level output voltage	$V_{OL}$	$I_{OL} = 2\text{mA}$			0.4	V
<b>DIGITAL OUTPUTS (CSB_M)</b>						
High level output voltage	$V_{OH}$	$I_{OH} = -2\text{mA}$	$DVDD1 - 0.4$			V
Low level output voltage	$V_{OL}$	$I_{OL} = 2\text{mA}$			0.4	V
<b>DIGITAL OUTPUTS (RSTO, STP, STS1, STS0, SO, OE, FR, ST, MD2, MD1, MD0)</b>						
High level output voltage	$V_{OH}$	$I_{OH} = -2\text{mA}$	$DVDD2 - 0.4$			V
Low level output voltage	$V_{OL}$	$I_{OL} = 2\text{mA}$			0.4	V

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>MOTOR SIGNAL INPUTS (OUTAI, OUTBI)</b>						
Input voltage range	V <sub>OUTI</sub>	T <sub>a</sub> : -40 to 85°C	0		AVDD	V
<b>AMPLIFIER OUTPUT (AMPO)</b>						
Output voltage range	V <sub>AMPO</sub>	T <sub>a</sub> : -40 to 85°C	0		AVDD	V
Maximum gain	G <sub>HAMPO</sub>	T <sub>a</sub> = 25°C		16		V/V
Minimum gain	G <sub>LAMPO</sub>	T <sub>a</sub> = 25°C		1		V/V
<b>ADC INPUTS (ADCI)</b>						
Input voltage range	V <sub>ADCI</sub>	T <sub>a</sub> : -40 to 85°C	0		AVDD	V
ADC offset error	IL <sub>ADCI</sub>	T <sub>a</sub> = 25°C			±2.0	LSB
ADC differential non-linearity	DIL <sub>ADCI</sub>	T <sub>a</sub> = 25°C			±1.0	LSB
<b>REFERENCE VOLTAGE INPUT (VREFI)</b>						
Input voltage range	V <sub>VREFI</sub>	T <sub>a</sub> : -40 to 85°C		AVDD	AVDD	V
<b>REFERENCE VOLTAGE OUTPUT (VREFO)</b>						
Output voltage range	V <sub>VREFO</sub>	T <sub>a</sub> : -40 to 85°C AVDD = 3.3V VREFI = 3.3V	0.24		3.07	V
DAC integral non-linearity	INL <sub>VREFO</sub>	T <sub>a</sub> = 25°C			±2.0	LSB
DAC differential non-linearity	DNL <sub>VREFO</sub>	T <sub>a</sub> = 25°C			±1.0	LSB
DAC zero scale voltage	V <sub>ZVREFO</sub>	T <sub>a</sub> = 25°C	0.14	0.24	0.34	V
DAC full scale voltage	V <sub>FVREFO</sub>	T <sub>a</sub> = 25°C	2.97	3.07	3.17	V

2. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## FUNCTIONAL DESCRIPTION

### Control Functions

LC898240 provides the following control functions.

- (1) Driver Control: It controls a stepper motor driver connected to LC898240.
- (2) Programmable Speed Control: The step pulses are generated based on the target speed and acceleration/deceleration curve.
- (3) High Efficient Current Control: The motor driving current is adapted against the load, and it gives high power efficiency.

### Power On/Off

Ideally, the power should be supplied to DVDD1, AVDD, DVDD2 and driver at the same time. But, if the simultaneity is impossible, the power-on sequence must be conformed to the following order within 100ms.

DVDD1 > AVDD > DVDD2 > driver

The power-off should also be done at the same time as well as power-on. And, the power-off sequence must be conformed to the following order within 100ms.

Driver > DVDD2 > AVDD > DVDD1

### Speed Acceleration Control

This function is activated by set 1 to the bit STPSEL. When the pin START is set H, or bit START\_REG is set 1, the step pulses are generated and output to the pin STP, based on the acceleration curve data written in the E2PROM.

### Current Control

The motor current is adjusted by the reference voltage at the pin VREFO driven by 8-bit DAC.

## REGISTER DESCRIPTION

## E2PROM

## Register Map

Address from	Address to	Description
0000h	002Fh	initial default settings for the main chip registers
0030h	003Fh	unused (filled by FFh)
0040h	03AFh	acceleration curve #0
03B0h	03BFh	unused (filled by FFh)
03C0h	072Fh	acceleration curve #1
0730h	073Fh	unused (filled by FFh)
0740h	0AAFh	acceleration curve #2
0AB0h	0ABFh	unused (filled by FFh)
0AC0h	0E2Fh	acceleration curve #3
0E30h	0E3Fh	unused (filled by FFh)
0E40h	11AFh	acceleration curve #4
11B0h	11BFh	unused (filled by FFh)
11C0h	152Fh	acceleration curve #5
1530h	153Fh	unused (filled by FFh)
1540h	18AFh	acceleration curve #6
18B0h	18BFh	unused (filled by FFh)
18C0h	1C2Fh	acceleration curve #7
1C30h	1C3Fh	unused (filled by FFh)
1C40h	1FAFh	acceleration curve #8
1FB0h	1FFFh	unused (filled by FFh)

Initial Default Settings

After the reset is released, the data written in the address 0000h to 002Fh of the E2PROM will be downloaded to the same address of the main chip registers. This function allows to set the initial default value for the registers. The register setting can be overwritten through the SPI.

Acceleration Curve

The E2PROM has the registers for nine acceleration curves with 440 steps for each. The step interval time is represented in 16-bit code.

$$T_{STP} = (D_{ROM} + 1) \times T_{CLK}$$

Where,

$T_{STP}$ : step interval time [s]

$D_{ROM}$ : E2PROM data. MSB in even address, and LSB in odd address.

$T_{CLK}$ : clock period [s]

The end of the acceleration curve sequence is set by  $D_{ROM} = \text{FFFFh}$ , and the motor rotation is kept in the constant speed.

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## Main Chip Register

### Register Map

ADDR[6:0]	Register Name	Default	Function	R/W
0000h	AIFSEL	00h	acceleration control interface configuration	R/W
0001h	START	00h	start/stop acceleration control	R/W
0002h	WSEL	00h	acceleration curve selection	R/W
0003h	INTP	00h	interpolation setting between steps	R/W
0004h	DSKIP	00h	skip setting at deceleration	R/W
0005h	SETST	00h	wait time for acceleration	R/W
0006h	SETED	00h	wait time for stop	R/W
0007h	STMODE	00h	constant speed period programming mode selection	R/W
0008h	STCNTL	00h	step counts for constant speed period (LSB)	R/W
0009h	STCNTH	00h	step counts for constant speed period (MSB)	R/W
0010h	DPSTG	00h	driver initial setting	R/W
0011h	DTSTG	00h	driver active setting	R/W
0012h	GCKRTO	00h	clock setting	R/W
0013h	GADSLIM	00h	speed setting for high efficient mode	R/W
0014h	GPSTG	00h	initial setting for High efficient mode	R/W
0015h	NMBUSTG	00h	NM/BU setting	R/W
0016h	BDSTG	00h	BD setting	R/W
0017h	SOSTG	00h	step out detection setting	R/W
0018h	GADMAX	00h	upper limit of VREFO level	R/W
0019h	GADSTOP	00h	VREFO level setting at motor stop	R/W
001Ah	GADSTAT	00h	FF value	R/W
001Bh	ADTDLT	00h	AD increment value target	R/W
001Ch	ADTBSE	00h	AD base value target	R/W
001Dh	ADTLIM	00h	AD minimum value target	R/W
001Eh	ADMDRTO2	00h	excitation mode ratio setting #2	R/W
001Fh	ADMDRTO3	00h	excitation mode ratio setting #3	R/W
0020h	ADMDRTO4	00h	excitation mode ratio setting #4	R/W
0021h	ADBURTO	00h	burst up threshold	R/W
0022h	ADSTO	00h	AD step out level	R/W
0023h	IPSTG	00h	analog portion	R/W
0024h	STSSEL	00h	status out setting	R/W
0025h	IFSEL	00h	interface setting	R/W
0030h	STS	-	status	R
0031h	PHSCNT	-	phase	R
0032h	SPDCEF	-	speed coefficient	R
0033h	ADDAT_LT_ADJ	-	ADC judgement point voltage	R
0034h	GADDAT	-	VREFO coefficient	R

### Register Function Description

AIFSEL: acceleration control interface configuration (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0000h	00h	-	-	-	-	-	-	-	AIFSEL

AIFSEL = 0: I/O port control mode, using pins; START, WSEL3/2/1/0 and INTP1/0.

AIFSEL = 1: register control mode, using registers; START\_REG, WSEL\_REG and INTP\_REG.

START: start/stop acceleration control (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0001h	00h	-	-	-	-	-	-	-	START_REG

It is effective during the register control mode (AIFSEL = 1).

Set START\_REG from 0 to 1 during motor stop: start acceleration

Set START\_REG from 1 to 0 during motor running in the constant speed: start deceleration

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WSEL acceleration curve selection (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0002h	00h	-	-	-	-	WSEL_REG[3:0]			

It is effective during the register control mode (AIFSEL = 1).

WSEL\_REG[3:0] = 0h: the acceleration curve #0  
 WSEL\_REG[3:0] = 1h: the acceleration curve #1  
 WSEL\_REG[3:0] = 2h: the acceleration curve #2  
 WSEL\_REG[3:0] = 3h: the acceleration curve #3  
 WSEL\_REG[3:0] = 4h: the acceleration curve #4  
 WSEL\_REG[3:0] = 5h: the acceleration curve #5  
 WSEL\_REG[3:0] = 6h: the acceleration curve #6  
 WSEL\_REG[3:0] = 7h: the acceleration curve #7  
 WSEL\_REG[3:0] = 8h: the acceleration curve #8  
 WSEL\_REG[3:0] = 9h - Fh: N.A.

INTP interpolation setting between steps (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0003h	00h	-	-	-	-	-	-	INTP_REG[1:0]	

It is effective during the register control mode (AIFSEL = 1).

INTP\_REG[1:0] = 0h: not interpolation  
 INTP\_REG[1:0] = 1h: interpolate 1 point between the steps based on E2PROM data  
 INTP\_REG[1:0] = 2h: interpolate 3 point between the steps based on E2PROM data  
 INTP\_REG[1:0] = 3h: interpolate 7 point between the steps based on E2PROM data

DSKIP skip setting at deceleration (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0004h	00h	-	-	-	-	-	-	DSKIP[1:0]	

The number of skip of the acceleration curve data for deceleration

DSKIP = 0: no skip  
 DSKIP = 1: 1 point skip  
 DSKIP = 2: 2 points skip  
 DSKIP = 3: 3 points skip

SETST wait time for acceleration R/W

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0005h	00h	SETST[7:0]							

Waiting time for acceleration

$$T_{WAIT} = T_{INIT} \times SETST[7:0]$$

Where,

$T_{WAIT}$ : waiting time [s]

$T_{INIT}$ : initial acceleration pulse width [s]

SETED wait time for stop R/W

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0006h	00h	SETED[7:0]							

Waiting time for stop

$$T_{WAIT} = T_{INIT} \times SETED[7:0]$$

Where,

$T_{WAIT}$ : waiting time [s]

$T_{INIT}$ : initial acceleration pulse width [s]

STMODE constant speed period programming mode selection (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0007h	00h	-	-	-	-	-	-	-	STMODE

STMODE = 0: continue rotation at the constant speed after the acceleration until START = 0

STMODE = 1: rotate at the constant speed after the acceleration for the number of steps which is set in the register STCNT, followed by automatic deceleration and stop

START must be set 0 after the motor stops.

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STCNTL step counts for constant speed period (LSB) (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0008h	00h	STCNT[7:0]							

STCNTL step counts for constant speed period (MSB) (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0009h	00h	-	-	-	-	-	-	-	STCNT[8]

The number of steps for the constant speed in STMODE = 1  
STCNT must not be zero.

DPSTG driver initial setting (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0010h	00h	RSTIV	RSTPHS	RSTAD	OERST	OEIV	OEMV	MDSEL[1:0]	

RSTIV

Polarity of RST signal.  
RSTIV = 0: low active (reset by L)  
RSTIV = 1: high active (reset by H)

RSTPHS

Synchronize with driver  
RSTPHS = 0: reset at 315 degree  
RSTPHS = 1: reset at 315 degree for full step excitation mode, reset at 0 degree for others

RSTAD

Reset phase adjustment  
RSTAD = 0: no adjustment for bipolar driver  
RSTAD = 1: adjustment enabled for unipolar driver

OERST

OE signal control  
OERST = 0: no OE signal control. The pin OE is switched to input of OE signal during I/O port control mode  
OERST = 1: activate OE single control. The pin OE is switched to output of OE signal. The pin ST is the OE signal input

OEIV

OE signal polarity  
OEIV = 0: high active  
OEIV = 1: low active

OEMV

OEMV = 0: ignore step pulse while the output is disabled  
OEMV = 1: advance phase with respect to the step pulse input even though the output is disabled

MDSEL[1:0]

MDSEL = 0h

MD = 0h: full step, both edges  
MD = 1h: half step, both edges  
MD = 2h: full step, rising edge  
MD = 3h: half step, rising edge  
MD = 4h: quarter step, both edges  
MD = 5h: 1/8 step, both edges  
MD = 6h: quarter step, rising edge  
MD = 7h: 1/8 step, rising edge

Pin connection

LC898240 pin MD2 --- open  
LC898240 pin MD1 --- STK672-6XXX pin MODE2  
LC898240 pin MD0 --- STK672-6XXX pin MODE1

## LC898240

### MDSEL = 1h

MD = 0h: half step, both edges  
 MD = 1h: quarter step, both edges  
 MD = 2h: 1/8 step, both edges  
 MD = 3h: 1/16 step, both edges  
 MD = 4h: full step, rising edge  
 MD = 5h: half step, rising edge  
 MD = 6h: quarter step, rising edge  
 MD = 7h: 1/8 step, rising edge

#### Pin connection

LC898240 pin MD2 --- STK672-4XXX pin MODE3  
 LC898240 pin MD1 --- STK672-4XXX pin MODE2  
 LC898240 pin MD0 --- STK672-4XXX pin MODE1

### MDSEL = 2h

MD = 0h: full step, rising edge  
 MD = 1h: half step, rising edge  
 MD = 2h: quarter step, rising edge  
 MD = 3h: 1/8 step, rising edge  
 MD = 4h: full step, rising edge  
 MD = 5h: half step, rising edge  
 MD = 6h: quarter step, rising edge  
 MD = 7h: 1/16 step, rising edge

#### Pin connection

LC898240 pin MD2 --- open  
 LC898240 pin MD1 --- LV8736V pin MD2  
 LC898240 pin MD0 --- LV8736V pin MD 1

### MDSEL = 3h

MD = 0h: full step, rising edge  
 MD = 1h: half step, rising edge  
 MD = 2h: half step, rising edge  
 MD = 3h: quarter step, rising edge  
 MD = 4h: full step, rising edge  
 MD = 5h: half step, rising edge  
 MD = 6h: quarter step, rising edge  
 MD = 7h: half step, rising edge

#### Pin connection

LC898240 pin MD2 --- open  
 LC898240 pin MD1 --- LV8740V pin MD2  
 LC898240 pin MD0 --- LV8740V pin MD 1

### DTSTG driver active setting (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0011h	00h	GAD_REG	ST_REG	RST_REG	OE_REG	FR_REG	MD_REG[2:0]		

#### GAD\_REG

Enable/disable the high efficient (adaptive current control) function  
 Enabled when bit GAD\_REG = 1 or pin GAD = H

#### ST\_REG

Outputs ST signal from the pin ST during the register control mode  
 When it used with the unipolar driver STK672-XXXX, ST\_REG value must be same as bit RST\_REG.  
 During IO port control mode, ST\_REG is ignored.

#### RST\_REG

Outputs RST signal from the pin RSTO during the register control mode  
 During IO port control mode, RST\_REG is ignored.

#### OE\_REG

Outputs OE signal from the pin OE during the register control mode  
 During IO port control mode, OE\_REG is ignored.

## LC898240

### FR\_REG

Outputs FR signal from the pin FR during the register control mode  
During IO port control mode, FR\_REG is ignored.

### MD\_REG[2:0]

Outputs MD signal from the pins MD2, MD1 and MD0 during the register control mode  
During IO port control mode, MD\_REG is ignored.

### GCKRTO clock setting (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0012h	00h	-	-	GCKRTO[5:0]					

### GCKRTO[5:0]

Defines the ratio between CLK and virtual clock (GCK = 840kHz)

$$\frac{f_{gck}}{f_{clk}} = 2^{-1}GCKRTO[5] + 2^{-2}GCKRTO[4] + \dots + 2^{-6}GCKRTO[0]$$

For example, in case of a clock of 4MHz at the pin CLK,

$$\frac{f_{gck}}{f_{clk}} = \frac{0.84}{4} = 0.21$$

$$GCKRTO[5:0] = 0Dh \rightarrow 0.203125$$

The virtual step pulse velocity is defined by,

$$f_{VSTP} = \frac{f_{STP} \times f_{gck}}{f_{clk} \times GCKRTO[5:0] \times k_{MD}}$$

$f_{VSTP}$ : virtual step pulse velocity [pps]

$f_{STP}$ : step pulse velocity [pps]

$k_{MD}$ : excitation mode factor (1 for half, 2 for quarter, 4 for 1/8 and 8 for 1/16 step)

### GADSLIM speed setting for smooth stepper mode (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0013h	00h	-	GADAC	GADSLIM[5:0]					

### GADAC

The high efficient mode (adoptive current control) and the acceleration control works concurrently.

GADAC = 0: not concurrent

GADAC = 1: high efficient mode activated after the acceleration completed

### GADSLIM

The high efficient mode is activated when the motor speed is faster than the speed specified by GADSLIM.

For example, to specify the virtual step pulse speed threshold 1900pps, set 0Bh for GADSLIM[5:0].

### GPSTG initial setting for high efficient mode (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0014h	00h	-	GADPHS	GADNUM[1:0]	OVPSLIM[3:0]				

### GADPHS

Defines the motor signal for OUTAI and OUTBI

GADPHS = 0: phase B (phase OUT2)

GADPHS = 1: phase A (phase OUT1)

### GADNUM

VREFO control frequency (over sampling)

GADNUM = 0h: default

GADNUM = 1h: 2x

GADNUM = 2h: 4x

GADNUM = 3h: 8x

### OVPSLIM

ADCI waveform tuning

## LC898240

NMBUSTG		NM/BU setting (R/W)							
Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0015h	00h	-	NMSEL	NMSTEP[1:0]		BUEN	BUSTEP[2:0]		

### NMSEL

VREFO adjust method

NMSEL = 0: constant type

NMSEL = 1: differential type

### NMSTEP

VREFO adjust step

NMSEL = 0

NMSTEP = 0h: 1/256 of VREFO full scale voltage

NMSTEP = 1h: 2/256 of VREFO full scale voltage

NMSTEP = 2h: 4/256 of VREFO full scale voltage

NMSTEP = 3h: 8/256 of VREFO full scale voltage

NMSEL = 1

NMSTEP = 0h:  $(|target - judge\ point| / 32) \times (1/256\ of\ VREFO\ full\ scale\ voltage)$

NMSTEP = 1h:  $(|target - judge\ point| / 16) \times (1/256\ of\ VREFO\ full\ scale\ voltage)$

NMSTEP = 2h:  $(|target - judge\ point| / 8) \times (1/256\ of\ VREFO\ full\ scale\ voltage)$

NMSTEP = 3h:  $(|target - judge\ point| / 4) \times (1/256\ of\ VREFO\ full\ scale\ voltage)$

### BUEN

BUEN = 0: burst up off

BUEN = 1: burst up on

### BUSTEP

VREFO adjustment resolution at the bust up

BUSTEP = 0h: 2/256 of the VREFO full scale voltage

BUSTEP = 1h: 4/256 of the VREFO full scale voltage

BUSTEP = 2h: 8/256 of the VREFO full scale voltage

BUSTEP = 3h: 16/256 of the VREFO full scale voltage

BUSTEP = 4h: 32/256 of the VREFO full scale voltage

BUSTEP = 5h: 64/256 of the VREFO full scale voltage

BUSTEP = 6h: 128/256 of the VREFO full scale voltage

BUSTEP = 7h: 256/256 of the VREFO full scale voltage

BDSTG		BD setting (R/W)							
Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0016h	00h	-	BDSEL	BDNUM[1:0]		BDEN	BDSTEP[2:0]		

### BDSEL

Burst down condition

BDSEL = 0: higher voltage than the judgement point

BDSEL = 1: ADCI waveform is convex.

### BDNUM

The bust down condition qualifier: when the event consecutively repeated for the following number of times, this function is activated.

BDNUM = 0h: twice

BDNUM = 0h: 4 times

BDNUM = 0h: 8 times

BDNUM = 0h: 16 times

### BDEN

BDEN = 0: burst down deactivated

BDEN = 1: burst down activated

### BDSTEP

VREFO adjustment resolution at the bust down

BDSTEP = 0h: 8/256 of the VREFO full scale voltage

BDSTEP = 1h: 12/256 of the VREFO full scale voltage

BDSTEP = 2h: 16/256 of the VREFO full scale voltage

BDSTEP = 3h: 24/256 of the VREFO full scale voltage

BDSTEP = 4h: 32/256 of the VREFO full scale voltage

BDSTEP = 5h: 48/256 of the VREFO full scale voltage

BDSTEP = 6h: 64/256 of the VREFO full scale voltage

BDSTEP = 7h: 96/256 of the VREFO full scale voltage

## LC898240

SOSTG step out detection setting (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0017h	00h	-	-	-	-	-	SOMD	SONUM	

SOMD

SOMD = 0: set the flag STPOUT = 1 whenever the step out is detected

SOMD = 1: latch the flag STPOUT = 1 when the step out is detected, and clear the flag by RST or ST reset

SONUM

The step out detection qualifier: when the event consecutively repeated for the following number of times, the step out detection is flagged.

SONUM = 0h: once

SONUM = 1h: twice

SONUM = 2h: 8 times

SONUM = 3h: 16 times

GADMAX upper limit of VREFO level (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0018h	00h	GADMAX[7:0]							

GADMAX[7:0]

Upper limit of VREFO voltage level

$$V_{LIMIT} = V_{FULL} \times \frac{GADMAX}{256}$$

GADSTOP VREFO level setting at motor stop (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0019h	00h	GADSTOP[7:0]							

GADSTOP

VREFO voltage level during motor stop (RDY = L and MACT L)

$$V_{STOP} = V_{FULL} \times \frac{GADSTOP}{256}$$

GADSTOP value must be equal to or less than GADMAX. If this function is not used, set the same value to GADSTOP as GADMAX.

GADSTAT FF value (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
001Ah	00h	GADSTAT[7:0]							

GADSTAT

The initial value of VREFO for the high efficient mode as feedforward control

$$V_{FF} = V_{FULL} \times \frac{GADSTAT}{256}$$

GADSTAT value must be equal to or less than GADMAX. If this function is not used, set the same value to GADSTAT as GADMAX.

ADTDLT AD increment value target (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
001Bh	00h	ADTDLT[7:0]							

See the illustration below.

ADTBSE AD base value target (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
001Ch	00h	ADTBSE[7:0]							

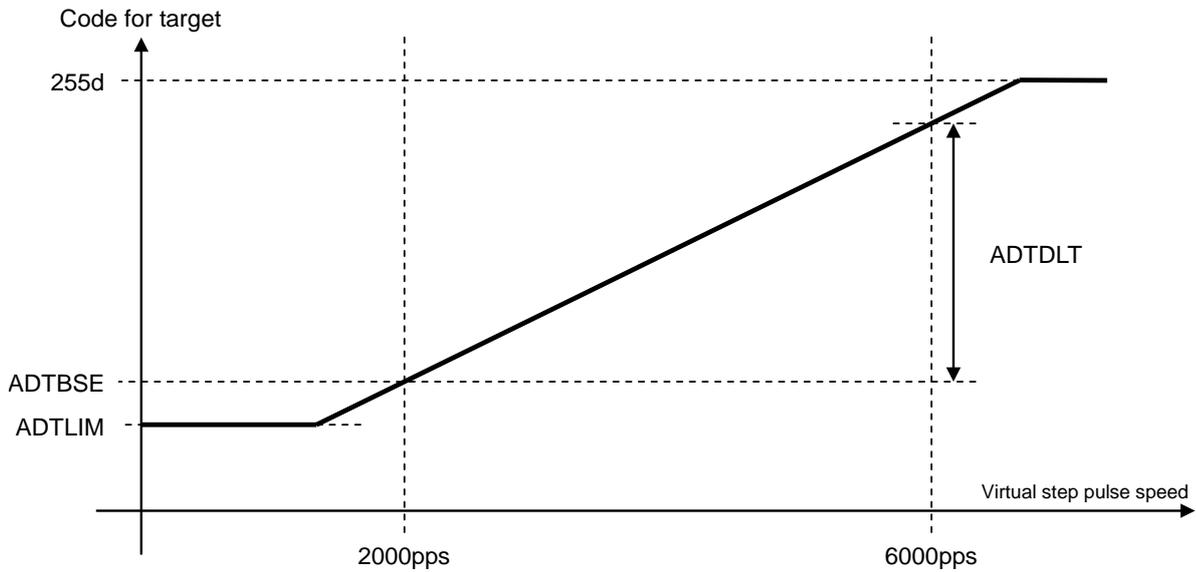
See the illustration below.

ADTLIM AD minimum value target (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
001Dh	00h	ADTLIM[7:0]							

See the illustration below.

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**ADMDRTO2** excitation mode ratio setting #2 (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
001Eh	00h	-	-	ADMDRTO2[5:0]					

ADMDRTO2[5:0]

The target value ratio between half step and quarter step excitation mode

$$\text{ratio} = 2^{-1}ADMDRTO2[5] + 2^{-2}ADMDRTO2[4] + \dots + 2^{-6}ADMDRTO2[0]$$

**ADMDRTO3** excitation mode ratio setting #3 (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
001Fh	00h	-	-	ADMDRTO3[5:0]					

ADMDRTO3[5:0]

The target value ratio between half step and 1/8 step excitation mode

$$\text{ratio} = 2^{-1}ADMDRTO3[5] + 2^{-2}ADMDRTO3[4] + \dots + 2^{-6}ADMDRTO3[0]$$

**ADMDRTO4** excitation mode ratio setting #4 (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0020h	00h	-	-	ADMDRTO4[5:0]					

ADMDRTO4[5:0]

The target value ratio between half step and 1/16 step excitation mode

$$\text{ratio} = 2^{-1}ADMDRTO4[5] + 2^{-2}ADMDRTO4[4] + \dots + 2^{-6}ADMDRTO4[0]$$

**ADBURTO** burst up threshold (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0021h	00h	-	-	ADBURTO[5:0]					

ADBURTO[5:0]

The target value ration against the burst up threshold

$$\text{ratio} = 2^{-1}ADBURTO[5] + 2^{-2}ADBURTO[4] + \dots + 2^{-6}ADBURTO[0]$$

**ADSTO** AD step out level (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0022h	00h	ADSTO[7:0]							

ADSTO[7:0]

The code for tentative step out judgement

## LC898240

IPSTG analog portion (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0023h	00h	-	-	ADCWDT[2:0]			AMPGN[2:0]		

ADCWDT[2:0]

Analog characteristics setting

It must be 2.

AMPGN[2:0]

Gain of the amplifier for AMPO output

AMPGN = 0h: 1x

AMPGN = 1h: 2x

AMPGN = 2h: 4x

AMPGN = 3h: 8x

AMPGN = 4h: 16x

AMPGN = 5h to 7h: inhibited

STSSEL status out setting (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0024h	00h	STS1SEL[3:0]				STS0SEL[3:0]			

STS1SEL[3:0]

Status signal selection for the pin STS1

STS0SEL[3:0]

Status signal selection for the spin STS0

The spins STS1 and STS0 get H during E2PROM down load, after the reset by RSB is released.

STS1SEL = 0h: L

STS1SEL = 1h: RDY

STS1SEL = 2h: MACT

STS1SEL = 3h: ACB

STS1SEL = 4h: MONI (driver home position)

STS1SEL = 5h: STPOUT (step out detected)

STS1SEL = 6h: GAD\_EN (high efficient mode)

STS1SEL = 7h: ADJ\_EN (VREF adjusted)

STS1SEL = Ah: BSTDWN (bust down)

STS1SEL = Bh: BSTUP (burst up)

STS1SEL = Ch to Fh: not allowed

IFSEL interface setting (R/W)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0025h	00h	-	-	-	-	-	-	STPSEL	IFSEL

STPSEL

Step pulse source selection

STPSEL = 0: input from external through the pin START

STPSEL = 1: acceleration control mode. The step pulse is generated by the acceleration controller. The pin START is used for acceleration start (START = H) and deceleration start (START = L)

IFSEL

Control mode selection

IFSEL = 0: IO port control mode

Input pins: ST, FR, MD2, MD1, MD0, and either OE (OERST = 0) or ST (OERST = 1, OE output)

Registers ST\_REG, RST\_REG, OE\_REG, FR\_REG and MD\_REG are ignored.

IFSEL = 1: register control mode

Outputs ST, FR, MD2, MD1, MD0, OE and RSTO are driven by ST\_REG, FR\_REG, MD\_REG, OE\_REG and RST\_REG.

## LC898240

STS status (Read Only)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0030h	00h	-	GAD_EN	STPOUT	MONI	ACB	MACT	RDY	INIT

GAD\_EN

1: the high efficient mode

STPOUT

1: step out detected

MONI

1: driver home position

ACB

1: acceleration completed

MACT

1: motor active excluding wait time

0: motor inactive

If the acceleration function is not used, set 1 by step pulse input, and set 0 when speed gets lower than approximately 350pps (pulse interval equivalent to half step).

RDY

1: motor active including wait time

INIT

1: E2PROM download on-going

PHSCNT phase (Read Only)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0031h	00h	-	-	PHSCNT[5:0]					

PHSCNT

Phase count

$$\text{phase} = 360^\circ \times \frac{\text{PHSCNT}[5:0]}{64}$$

SPDCEF speed coefficient (Read Only)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0032h	00h	-	-	SPDCEF[5:0]					

SPDCEF[5:0]

Motor speed coefficient

ADDAT\_LT\_ADJ ADC judgement point voltage (Read Only)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0033h	00h	ADDAT_LT_ADJ[7:0]							

ADDAT\_LT\_ADJ[7:0]

Code of the ADC judgement point voltage

GADDAT VREFO coefficient (Read Only)

Address	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0034h	00h	GADDAT[7:0]							

GADAT

$$V_{DAT} = V_{FULL} \times \frac{GADDAT}{256}$$

# LC898240

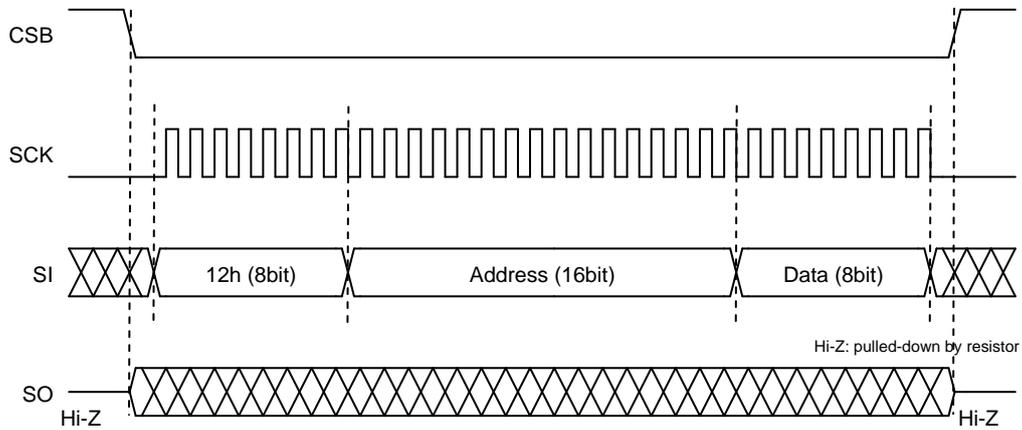
## SERIAL INTERFACE (SPI)

LC898240 has the main chip registers and the non-volatile memory (E2PROM). They can be accessed through a serial interface (SPI). During E2PROM data download to the main chip registers, the only status register STS can be read.

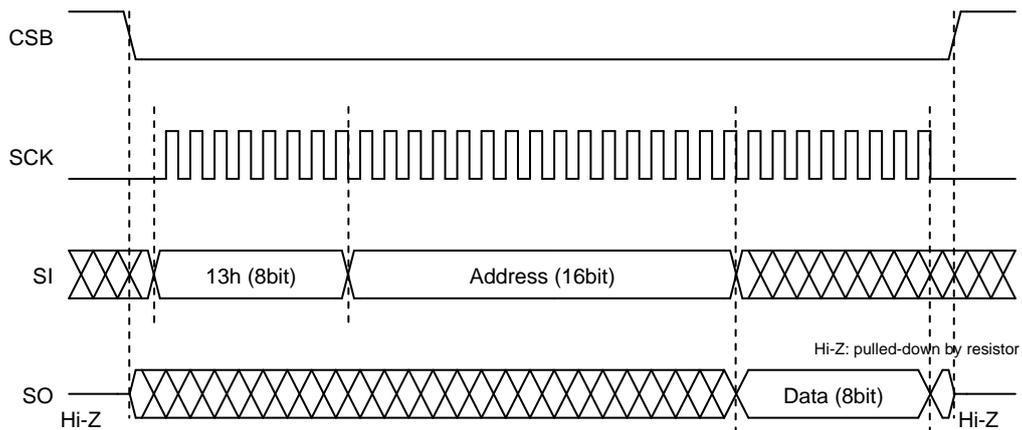
During acceleration operation, the only main chip registers can be access (write/read). Regarding E3PROM access, refer to the E2PROM datasheet.

### Write/Read Sequence

#### Main Chip Register Write

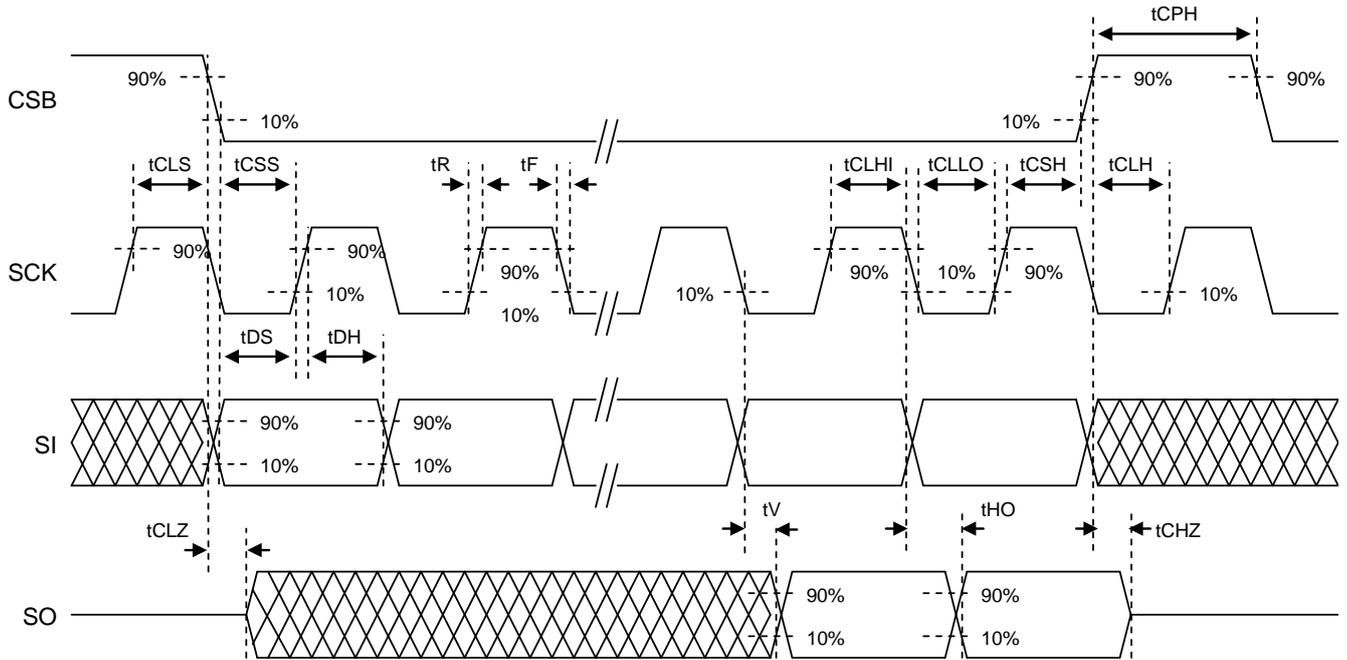


#### Main Chip Register Read



# LC898240

## SPI Timing



$T_a = -40$  to  $85^\circ\text{C}$ ,  $DV_{SS} = 0\text{V}$ ,  $DV_{DD1} = 3.0$  to  $3.6\text{V}$ ,  $DV_{DD2} = 3.0$  to  $5.0\text{V}$ ,  $SO$  load =  $30\text{pF}$

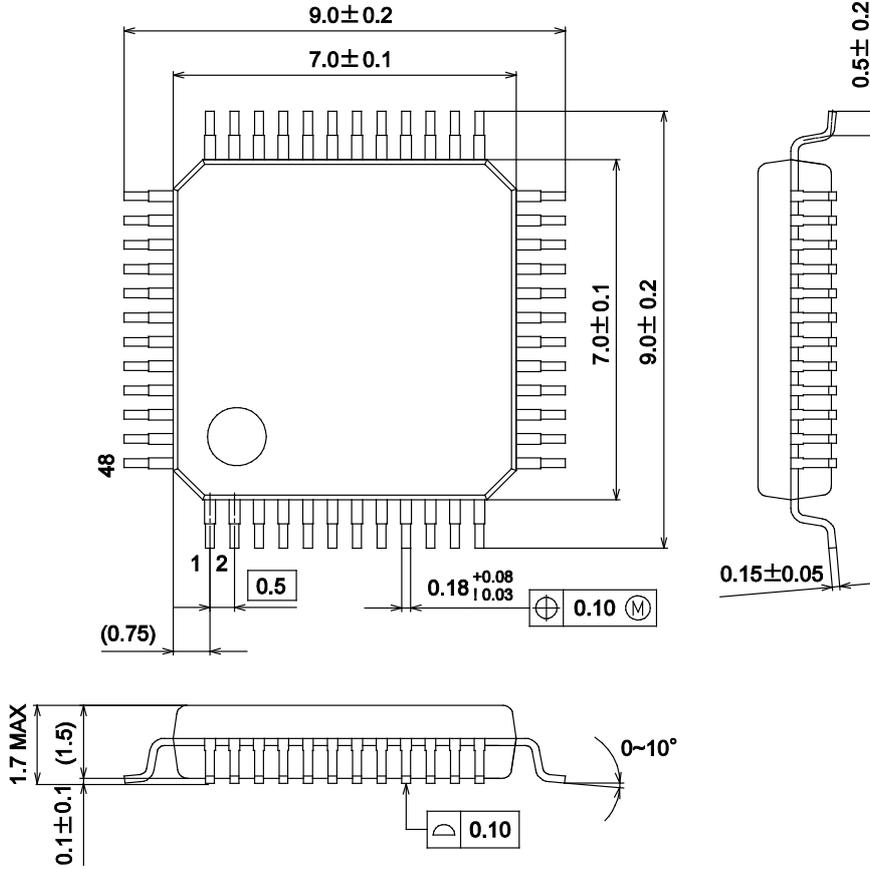
Symbol	Parameter	min.	typ.	max.	unit
FCLK	SCK clock frequency			5	MHz
$t_R$	SCK rising time			20	ns
$t_F$	SCK falling time			20	ns
$t_{CLHI}$	SCK H-pulse width	100			ns
$t_{CLLO}$	SCK L-pulse width	100			ns
$t_{CSS}$	CSB setup time	100			ns
$t_{CLS}$	SCK setup time	100			ns
$t_{DS}$	SI setup time	30			ns
$t_{DH}$	SI hold time	40			ns
$t_{CSH}$	CSB hold time	100			ns
$t_{CLH}$	SCK hold time	100			ns
$t_{CPH}$	CSB H-pulses width	100			ns
$t_{CHZ}$	SO transition time to high impedance state			170	ns
$t_V$	SO data transition time			90	ns
$t_{HO}$	SO data hold time	0			ns
$t_{CLZ}$	SO high impedance state hold time	0			ns

# LC898240

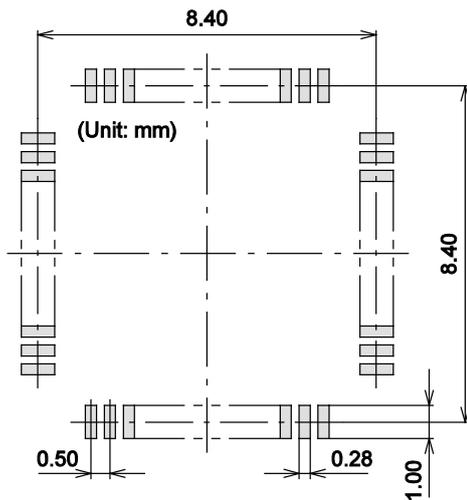
## PACKAGE DIMENSIONS

unit : mm

**SPQFP48 7x7 / SQFP48**  
**CASE 131AJ**  
**ISSUE A**



### SOLDERING FOOTPRINT\*



NOTE: The measurements are not to guarantee but for reference only.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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