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AN-8422

650 V Auto SPM® Series

Automotive 3-Phase IGBT Smart Power Module User's Guide

Table of Contents

1 Introduction

The Auto SPM® Series extends the existing Smart Power Module product portfolio, qualifying them to meet the performance and reliability requirements of automotive auxiliary motor drives in Hybrid and Electric Vehicle applications. Additionally, the Auto SPM® increases the component integration, reduces footprint and simplifies assembly.

This application note supports the 650 V Auto SPM® Series. It should be used in conjunction with the relevant datasheet FAM65V05DF1, which is the lead product of this portfolio. FAM65V05DF1 is a 27-pin 650 V/50 A, 3-phase Smart Power Module, Automotive qualified to meet the growing needs of the Hybrid & Electric Vehicles market.

1.1 Design Concept

The design provides a minimized package and low power consumption module with improved reliability. This is achieved by applying an automotive-qualified 650 V gate-driving High-Voltage Integrated Circuit (HVIC), Field Stop Trench IGBTs with Stealth diodes optimized for motor control, and improved Direct Bonded Copper (DBC) substrate transfer molded package. FAM65V05DF1 achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are automotive motor drives such as air conditioner compressors, oil pumps and other auxiliary motors in Hybrid and Electric Vehicles.

FAM65V05DF1 includes features to enhance system reliability, including temperature sensing, over-current detection with soft-shutdown, and under-voltage lockout. The temperature-sensing function is implemented in the LVIC, generating an analog voltage which is proportional to temperature.

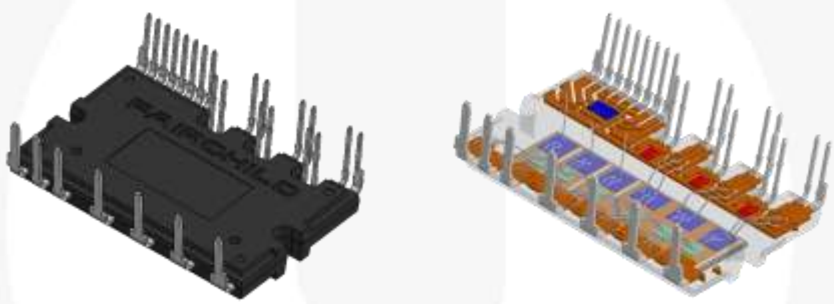


Figure 1. External View and Internal Structure of the Auto SPM® Series (FAM65V05DF1)

1.2 Ordering Information

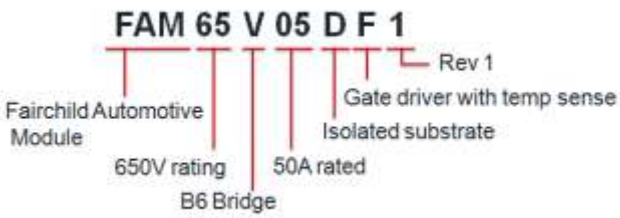


Figure 2. Ordering Information

1.3 Features and Integrated Functions

- DBC Substrate
  - Excellent Thermal Conductivity, Keeping 2500 V_{rms} Isolation Voltage from Pin to Heat Sink
- Integrated Components:
  - One-Channel HVIC (three HVICs) for High-Side Control
  - Three-Channel LVIC (one LVIC) for Low-Side Control
  - Six IGBT / Diode Power Switches
- Control Drive Supply:
  - Single DC Supply Compatible
- High-Side Gate Driver (One-Channel)
  - High-Voltage Level-Shift Circuit
  - Input interface: Active HIGH
  - Compatible for 3.3 V Controller Outputs
  - Under-Voltage Lockout without Fault Signal
- Low-Side Gate Driver (Three-Channel)
  - Input Interface: Active HIGH
  - Compatible for 3.3 V Controller Outputs
  - Under-Voltage Lockout with Fault Signal
  - Short-Circuit, Over-Current Protection
- Soft Turn-off Prevents Excessive Surge Voltage
- Temperature Sensing of LVIC

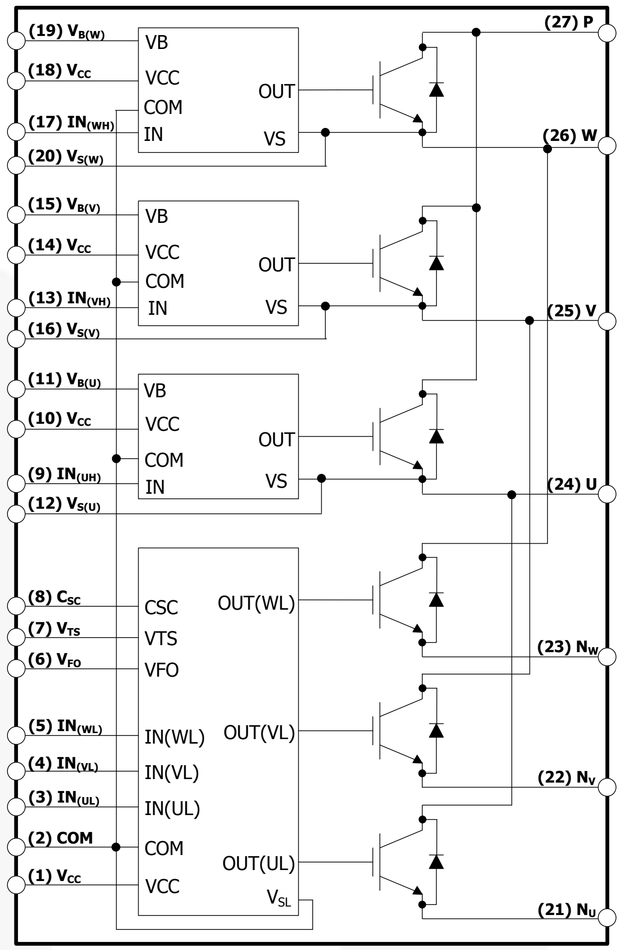


Figure 3. Internal Equivalent Circuit, Input / Output Pins

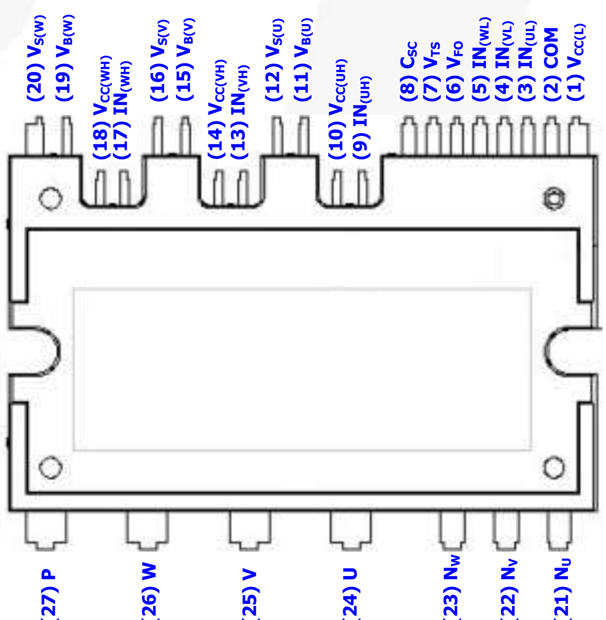


Figure 4. Package Top-View and Pin Assignment

2 Product Synopsis

This section discusses pin descriptions, electrical specifications, characteristics, and packaging.

Table 1. **Pin Description**

Pin Number	Name	Description
1	VCC(L)	Low-Side Common Bias Voltage for IC and IGBTs Driving
2	COM	Common Supply Ground
3	IN(UL)	Signal Input for Low-Side U Phase
4	IN(VL)	Signal Input for Low-Side V Phase
5	IN(WL)	Signal Input for Low-Side W Phase
6	VFO	Fault Output
7	VTS	Thermal Sensing Voltage in LVIC
8	CSC	Voltage Input for SC detection
9	IN(UH)	Signal Input for High-Side U Phase
10	VCC(UH)	High-Side Bias Voltage for U Phase IC
11	VB(U)	High-Side Bias Voltage for U Phase IGBT Driving
12	VS(U)	High-Side Bias Voltage Ground for U Phase IGBT Driving
13	IN(VH)	Signal Input for High-Side V Phase
14	VCC(VH)	High-Side Bias Voltage for V Phase IC
15	VB(V)	High-Side Bias Voltage for V Phase IGBT Driving
16	VS(V)	High-Side Bias Voltage Ground for V Phase IGBT Driving
17	IN(WH)	Signal Input for High-Side W Phase
18	VCC(WH)	High-Side Bias Voltage for W Phase IC
19	VB(W)	High-Side Bias Voltage for W Phase IGBT Driving
20	VS(W)	High-Side Bias Voltage Ground for W Phase IGBT Driving
21	NU	Negative DC-Link Input for U Phase
22	NV	Negative DC-Link Input for V Phase
23	NW	Negative DC-Link Input for W Phase
24	U	Output for U Phase
25	V	Output for V Phase
26	W	Output for W Phase
27	P	Positive DC-Link Input

2.1 Detailed Pin Description

- High-Side Bias Voltage Pins for Driving the IGBTs / High-Side Bias Voltage Ground Pins for Driving the IGBTs:
  - ▶ Pins: $VB_{(U)}$-$VS_{(U)}$, $VB_{(V)}$-$VS_{(V)}$, $VB_{(W)}$-$VS_{(W)}$
  - These are drive power supply pins for providing gate drive power to the high-side IGBTs.
  - The virtue of the bootstrap circuit scheme is that no external power supplies are required for the high-side IGBTs.
  - Each bootstrap capacitor is charged from the V_{CC} supply during ON state of the corresponding low-side IGBT.
  - To prevent malfunctions caused by noise and ripple in the supply voltage, a low-ESR, low-ESL filter capacitor should be mounted very close to these pins.
- Low-Side Bias Voltage Pin / High-Side Bias Voltage Pins:
  - ▶ Pins: $VCC_{(L)}$, $VCC_{(WH)}$, $VCC_{(VH)}$, $VCC_{(UH)}$
  - These are control supply pins for the built-in ICs.
  - These four pins should be connected externally.
  - To prevent malfunctions caused by noise and ripple in the supply voltage, a low-ESR, low-ESL filter capacitor should be mounted very close to these pins.
- Common Supply Ground Pin
  - ▶ Pin: COM
  - This is the supply ground pin for the built-in ICs.
  - Important! To avoid noise influences, the main power circuit current should not be allowed to flow through this pin.
- Signal Input Pins
  - ▶ Pins: $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$
  - These pins control the operation of the built-in IGBTs.
  - They are activated by voltage input signals. The terminals are internally connected to a Schmitt-trigger circuit composed of 5 V-class CMOS.
  - The signal logic of these pins is active HIGH. The IGBT associated with each of these pins is turned ON when a sufficient logic voltage is applied to these pins.
  - The wiring of each input should be as short as possible to protect the module against noise influences.
  - To prevent signal oscillations, RC coupling is recommended, as illustrated in *Figure 31*.
- Analog Temperature Sensing Output Pin
  - ▶ Pin: V_{TS}
  - This indicates the temperature of the 3-phase LVIC with an analog voltage output. The LVIC itself creates some heating, but it mostly indicates the heat generated from the IGBTs.
  - V_{TS} versus temperature characteristics are illustrated in *Figure 40*.
- Short-Circuit and Over-Current Detection Input Pin
  - ▶ Pin: C_{SC}
  - Depending on the current detecting resistor topology *(Figure 24)*, a low-pass filter may be inserted before the C_{SC} pin.
  - The shunt resistor should be selected to meet the detection levels matched for the specific application. An RC filter should be connected to the C_{SC} pin to eliminate noise.
  - The connection length between the shunt resistor and C_{SC} pin should be minimized.
- Fault Output Pin
  - ▶ Pin: V_{FO}
  - This is the fault output alarm pin. An active LOW output is given on this pin for a fault condition.
  - The alarm conditions are: Short-Circuit Protection (SCP) and low-side bias Under-Voltage Lockout (U_{VLO}).
  - The V_{FO} output is open drain configured. The V_{FO} signal line should be pulled to the 5 V logic power supply with approximately 4.7 kΩ resistance.
- Positive DC-Link Pin
  - ▶ Pin: P
  - This is the DC-link positive power supply pin of the inverter.
  - It is internally connected to the collectors of the high-side IGBTs.
  - To suppress surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (tip: metal film capacitor is typically used).

- Negative DC-Link Pins
  - ▶ Pins: NU, NV, NW
  - These are the DC-link negative power supply pins (power ground) of the inverter.
  - These pins are connected to the low-side IGBT emitters of each phase.
- Inverter Power Output Pins
  - ▶ Pins: U, V, W
  - Inverter output pins for connecting to the inverter load (e.g. motor).

2.2 Data Sheet Explanation

Table 2. **Inverter**

Symbol	Parameter	Explanation
$V_{PN(Surge)}$	Supply Voltage (Surge)	The package has internal stray inductance that will generate additional voltage surges to the IGBT and diodes during switching, compared to the device power leads. This parameter indicates the maximum voltage at the power pins during switching, so that the resulting internal voltage of the IGBT/diode remains below the avalanche breakdown rating (defined at room temperature). This parameter depends on the Breakdown Voltage (BV_{CESS}) of the selected IGBT/diode, gate driver resistance, and stray inductance of the module. These terms are defined and fixed by the design of the module. The $V_{PN(Surge)}$ of the datasheet excludes the stray inductance of the application itself. The stray inductance of the system as well as the selected V_{CC} and V_{BS} can also impact the dI/dt and consequently the voltage generated internally at the IGBT/diode. In case the dI/dt or stray inductance in the application is higher than the value reported in the data sheet condition, the user would need to recalculate the max $V_{PN(surge)}$ with reference to the Reverse Bias Safe Operating Area (RBSOA) curve of the datasheet, that can be applied safely to the module without risk of generating a surge voltage at the IGBT/diode beyond its rated BV_{CESS}.
V_{CES}	Collector-emitter Voltage at the IGBT/Diode	Rated breakdown voltage of the module, at room temperature, voltage beyond this level can cause an avalanche event
$\pm I_C$	IGBT Continuous Collector Current	Maximum continuous current resulting in T_J= 175°C
$\pm I_{CP}$	IGBT Peak Collector Pulse Current	Peak collector pulse current 1ms at V_{CC}=V_{BS}=15V, T_C= 25°C resulting in T_J= 175°C
P_C	Collector Dissipation	Calculated based on max rated T_J and R_{thjc}. Under this condition, T_C= 25°C, T_J= 175°C
T_J	Junction Temperature	Maximum operating temperature range for the IGBT/Diode and the driver IC.

Table 3. **Control Part**

Symbol	Parameter	Conditions	Rating Unit
V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$, $V_{CC(L)}$ - COM	Maximum rating based on design characteristics; condition beyond specification can damage the device
V_{BS}	High-Side Control Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM	
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} - COM	
I_{FO}	Fault Output Current	Sink Current at V_{FO} Pin	
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC} - COM	

Table 4. **Total System**

Symbol	Parameter	Explanations		
T_{STG}	Storage Temperature	This is the maximum storage temperature	-40~125	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1-Minute, Connect Pins to Heat Sink	2500	V_{rms}
T_{LEAD}	Max lead temperature at the base of the package during PCB assembly	To prevent re-melt of the leads at the base during soldering on the PCB	200	°C

Table 5. **Thermal Resistance**

Symbol	Parameter	Explanations
$R_{th(j-c)Q}$	Junction-to-Case Thermal Resistance	Maximum value for the IGBT, measurement based on the MIL STD 883-1012 under single chip heating condition, with the case reference point taken under the chip
$R_{th(j-c)F}$		Maximum value for the diodes; measurement based on the MIL STD 883-1012, under single chip heating condition, with the case reference point taken under the chip
L_{σ}	Package Stray Inductance from P to N_U, N_V, N_W	Stray inductance between P-U/V/W and U/V/W and –NU, NV, NW (total loop), measurement based on IEC 60747-15. This inductance will define the internal voltage overshoot at the IGBT/diode during switching based on the linear function ($V_{overshoot}$ = Lσ * di/dt)

Table 6. **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Explanation
V_{PN}	Supply Voltage	Applied between P - NU, NV, NW	Application testing under this condition shows margin against avalanche; In case the overshoot come closer to the device capability, it is better to place snubbers to reduce overshoot
V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$, $V_{CC(L)}$ - COM	This voltage is directly applied to the gate of the low/high side IGBTs. Lower voltage would result in higher losses; higher voltage would increase ringing during switching and also reduce the short circuit withstand time.
V_{BS}	High-Side Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	
dV_{CC}/dt, dV_{BS}/dt	Control Supply Variation		To prevent abnormal behavior of the gate driver
t_{DEAD}	Blanking Time for Preventing Short Circuit through High and Low Side IGBTs	For Each Input Signal	Prevent shoot through
f_{PWM}	PWM Input Signal	-40°C $\leq T_C \leq$ 125°C, - 40°C $\leq T_J \leq$ 150°C	Switching frequency is limited by the driver delay time and device efficiency
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W – COM (Including surge voltage)	Excessive offset between low-side emitter and gate driver ground can cause switching issues or trigger the Under Voltage Lockout.
T_J	Junction Temperature		Recommend operating junction temperature for long-term reliability

2.3 Electrical Characteristics (T_J=25°C, unless otherwise specified)

Table 7. **Inverter Part**

Symbol		Parameter	Explanations
$V_{CE(SAT)}$		Collector – Emitter Saturation Voltage	This is the maximum saturation voltage of the IGBT under given test conditions
V_F		Forward Voltage	This is the maximum forward voltage of the freewheeling diode under given test conditions
HS	t_{ON}	Switching Times	See Figure 6 (Switching Time Definition)
	$t_{C(ON)}$		
	t_{OFF}		
	$t_{C(OFF)}$		
	t_{rr}		
LS	t_{ON}		
	$t_{C(ON)}$		
	t_{OFF}		
	$t_{C(OFF)}$		
	t_{rr}		
I_{CES}		Collector – Emitter Leakage Current	This is the maximum leakage current of the IGBT and diode in blocking state under given test conditions
SCWT		Short Circuit Withstand Time	This is the duration the device can withstand a short circuit under given conditions. The system must shut down before this time to protect the IGBT from thermal failure. The short-circuit protection function helps to accomplish this.

Note:

1. t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching times of the IGBT itself under the given gate driving condition. *For detailed information, see Figure 5 and Figure 6*.

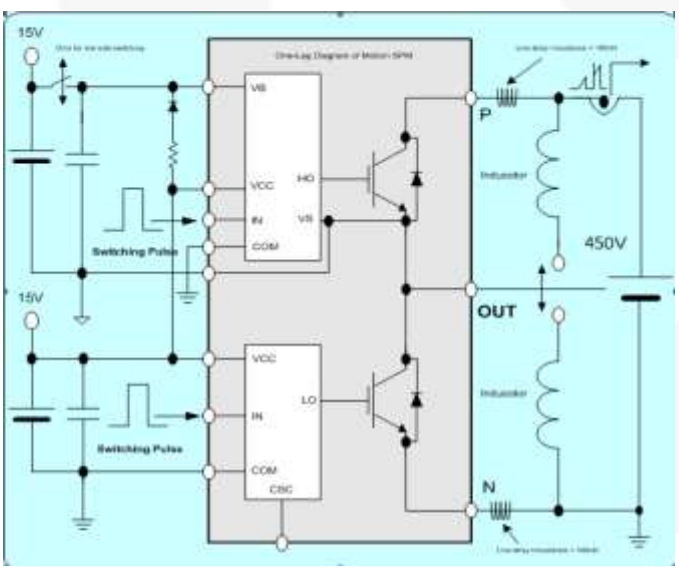


Figure 5. Switching Evaluation Circuit

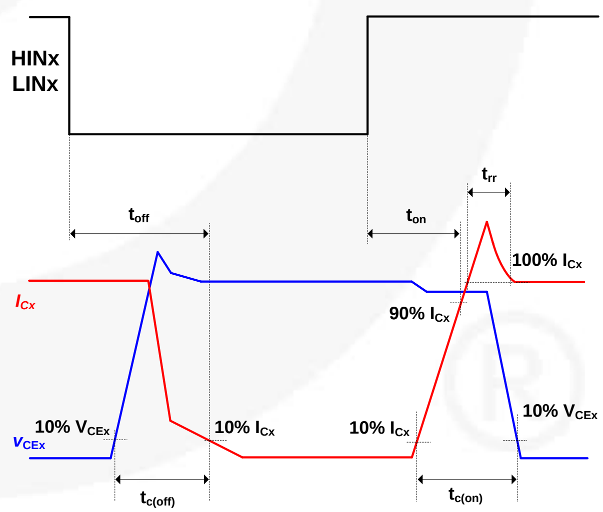


Figure 6. Switching Time Definition

Table 8. **Control Part**

Symbol	Parameter	Conditions
I_{QCCH}	Quiescent V_{CC} Supply Current	This is the leakage current of the ICs in non-operating mode, under given test conditions
I_{QCCL}		
I_{PCCH}	Operating High-Side V_{CC} Supply Current	This is the leakage current of the high side / low side ICs in operating mode, under given test conditions.
I_{PCCL}	Operating Low-Side V_{CC} Supply Current	
I_{QBS}	Quiescent V_{BS} Supply Current	This is the leakage current flowing through V_{BS} in non-operating mode
I_{PBS}	Operating V_{BS} Supply Current	This is the leakage current flowing through V_{BS} in operating mode.
V_{FOH}	Fault Output Voltage	See section 0
V_{FOL}		
$V_{SC(ref)}$	Short-Circuit Trip Level[2]	See section 4.1
UV_{CCD}	Supply Circuit, Under-Voltage Protection	See section 4.2
UV_{CCR}		
UV_{BSD}		
UV_{BSR}		
t_{FOD}	Fault-Out Pulse Width	This is the typical duration of the Fault Output flag
$V_{IN(ON)}$	ON Threshold Voltage	Input voltage of the IC needs to be higher to turn on the IGBT
$V_{IN(OFF)}$	OFF Threshold Voltage	Input voltage of the IC needs to be lower to turn off the IGBT

Note:

2. Short-circuit protection is implemented only by turn-off of the low-sides IGBTs.

3 Package

Heat dissipation is an important factor limiting the current capability of the power module. The characteristics of how the package dissipates heat are important in determining the performance. A trade-off exists among heat dissipation characteristics, package size, and voltage isolation characteristics. The key to good package technology lies in designing a small package size while maintaining outstanding heat dissipation characteristics and not compromising the isolation rating.

The 27 pin Auto SPM® Series is developed with a DBC substrate that results in good heat dissipation characteristics. Power die are attached directly to the DBC substrate. This technology achieves improved reliability and heat dissipation.

Figure 7 shows the vertical structure of the FAM65V05DF1.

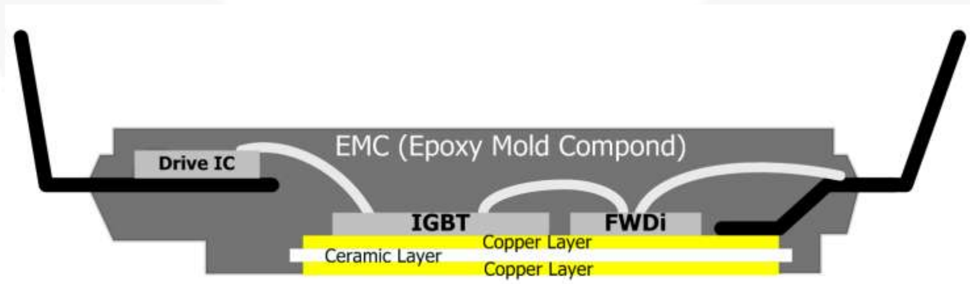


Figure 7. Vertical Structure of FAM65V05DF1

3.1 Isolation Distance

The isolation distances of the 27 pin Auto SPM® module are shown in *Figure 8*, *Figure 9*, *Figure 10*, and *Figure 11*.

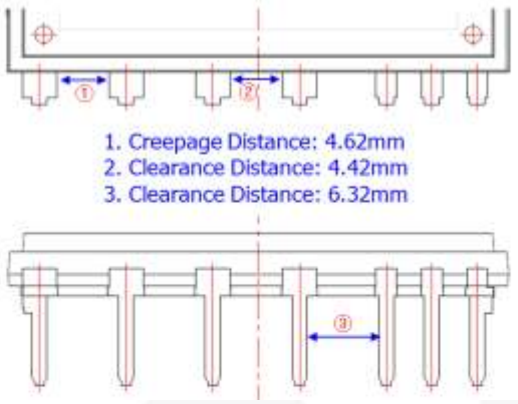


Figure 8. Isolation Distance between Power Pins

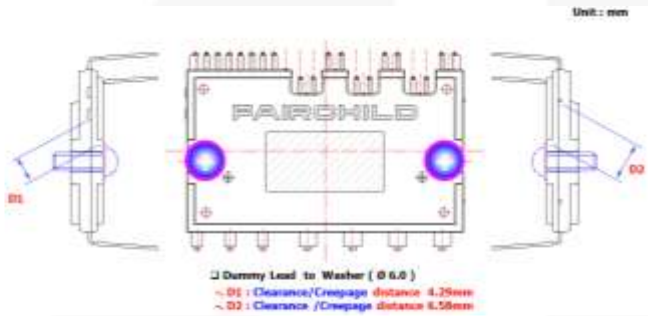


Figure 9. Isolation Distance between Live Dummy Pins and Mounting Screws

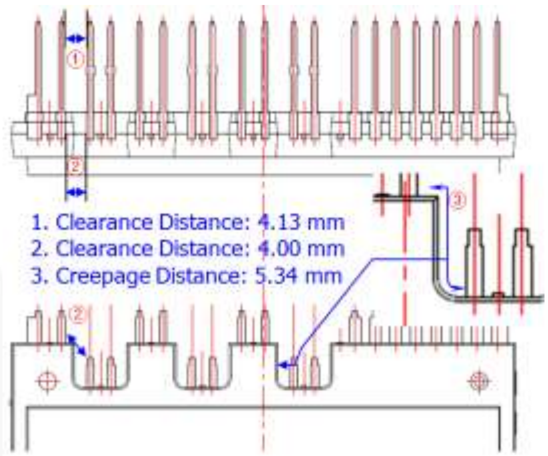


Figure 10. Isolation Distance between Signal Pins and High Potential Pins

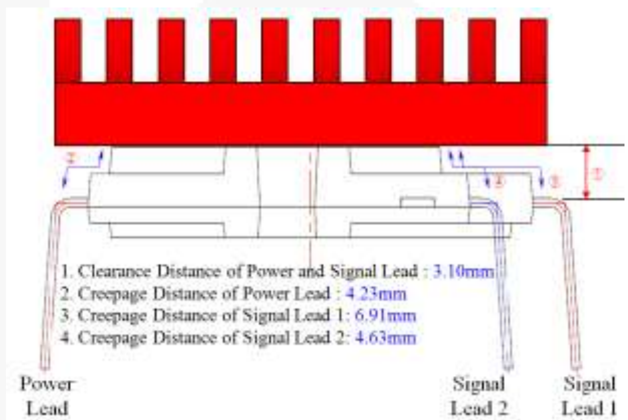


Figure 11. Isolation Distance between Heatsink and Pins

3.2 Mounting Method and Precautions

When installing a module to a heat sink, do not apply excessive torque on the mounting screws. This may cause ceramic cracks as well as destruction of screws and the heat sink. *Figure 12* shows the recommended fastening order. Avoid tightening one side at a time, as this can also damage the ceramic substrate. The pre-screwing torque should be set to 20~30% of the maximum torque rating. SEMS screws are recommended, including spring or plain washer.

Figure 12. Mounting Screws Fastening Order

Figure 13. SEMS Screw (Size M3, Spring Washer 5.0Φ, Plain Washer 7.5Φ)

Figure 14 and *Figure 15* show the flatness measurement points for the package and the heat sink. To get the most effective heat dissipation, it is necessary to enlarge the contact area between package and heat sink as much as possible.

Properly apply thermal-conductive grease over the contact surface between the module and the heat sink. Apply a minimum of 150 µm layer of thermal grease to the module base plate or heat sink. While fastening the module, a rim of thermal compound must be observed around the mounted module.

Thermal-conductive grease is also useful for preventing contact surface corrosion. Ensure the grease has stable quality and long endurance within the full operating temperature range. Use care to keep the contact surface free of any contaminants.

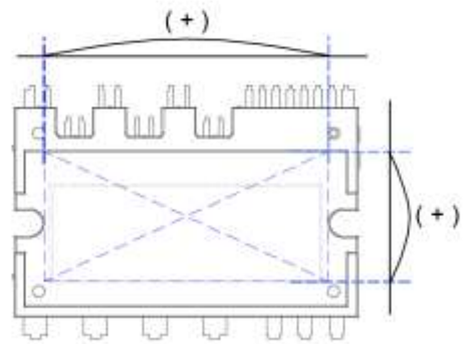


Figure 14. Package Surface Flatness

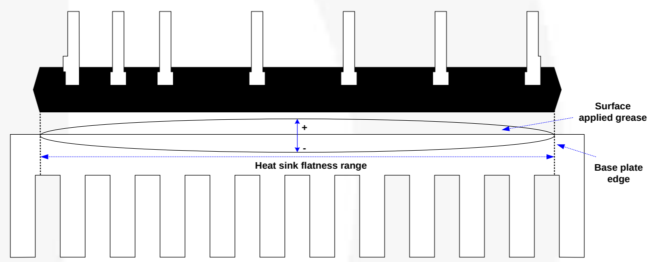


Figure 15. Heat Sink Flatness

Table 9. **Mechanical Characteristics and Ratings**

Parameter	Conditions		Value Min.	Value Typ.	Value Max.	Unit
Device Flatness	*See Figure 14*		0		+150	µm
Mounting Torque	Mounting Screw: M3	Recommended 0.7 N·m	0.6	0.7	0.8	N·m
		Recommended 7.1 kg·cm	6.2	7.1	8.1	kg·cm
Terminal Pulling Strength	Load 19.6 N		10			S
Terminal Bending Strength	Load 9.8 N, 90° Bend		2			Times
Weight				15		g

3.3 Thermal Impedance

Figure 16 shows the thermal equivalent circuit of the 27-pin Auto SPM® module mounted on a heatsink. For sustained power dissipation P_D at the junction, the junction temperature T_J can be calculated as:

$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \qquad (1)$$

Where T_A is the ambient temperature and $R_{\theta JC}$, $R_{\theta CS}$, and $R_{\theta SA}$ represent the thermal resistance from the junction-to-case, case-to-heatsink, and the heatsink-to-ambient for each IGBT and diode within the package, respectively. From equation (1), it is evident that for a limited $T_{J\text{-}max}$ (175°C), P_D can be increased by reducing $R_{\theta SA}$. This means that a more efficient cooling system will increase the power dissipation capability of Auto SPM® modules.

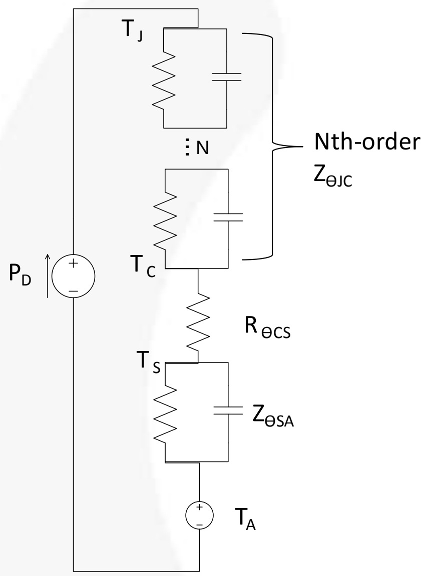


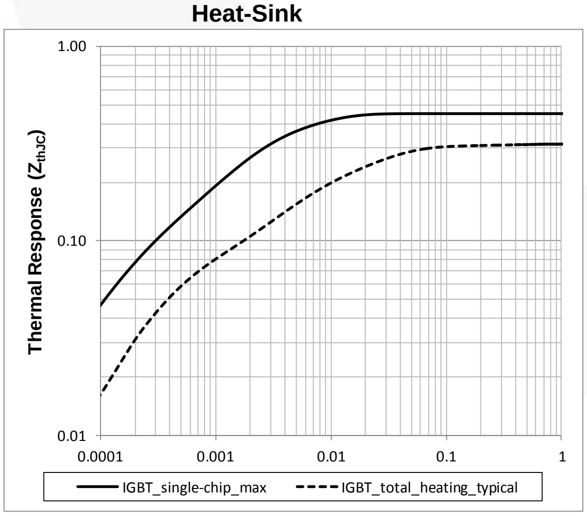
Figure 16. Transient Thermal Equivalent Circuit with a Heat-Sink

An infinite heat sink will result if $R_{\theta CS}$ and $R_{\theta SA}$ are reduced to zero and the case temperature T_c is locked at the fixed ambient temperature T_A.

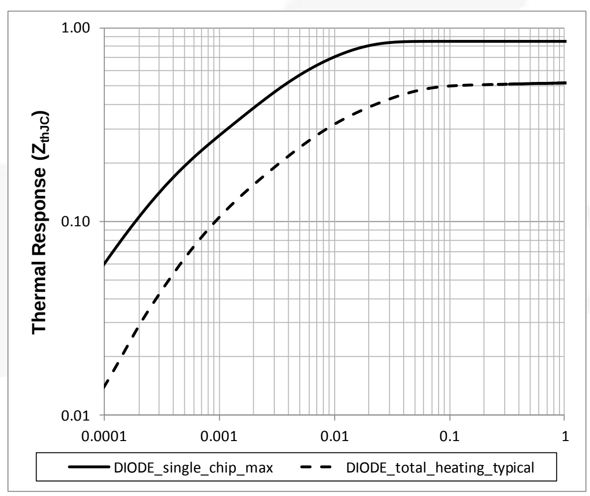
In practical operation, the power loss P_D is cyclical. Thermal capacitance delays the rise in junction temperature, and thus permits a heavier loading of the Auto SPM® package. Therefore the transient RC equivalent circuit shown in Figure 16 should be considered. For example, the RC values shown in *Table 10* represent a 6th-order Foster thermal model for a typical FAM65V05DF1 module, including 2% solder void. These values correspond to the typical impedance curves shown in *Figure 17*. This model can be used to simulate the thermal response of a given application within SPICE applications.

Table 10. **6th-Order Junction-Case Thermal Network**

N	IGBT		DIODE	
	R (Ω)	C (F)	R (Ω)	C (F)
1	0.088	0.341	-0.07	-1.429
2	-0.04	-0.025	0.105	0.762
3	-8e-4	-6.25e-3	0.1	0.4
4	0.16	0.05	0.26	0.038
5	-4e-3	-0.225	0.12	8.33e-3
6	0.105	4.76e-3	-5e-4	-2e-3



(1) Thermal Impedance Graph of IGBT



(2) Thermal Impedance Graph of FRD

Figure 17. Thermal Impedance Graphs (FAM65V05DF1)

3.4 Detailed Package Outline Drawings

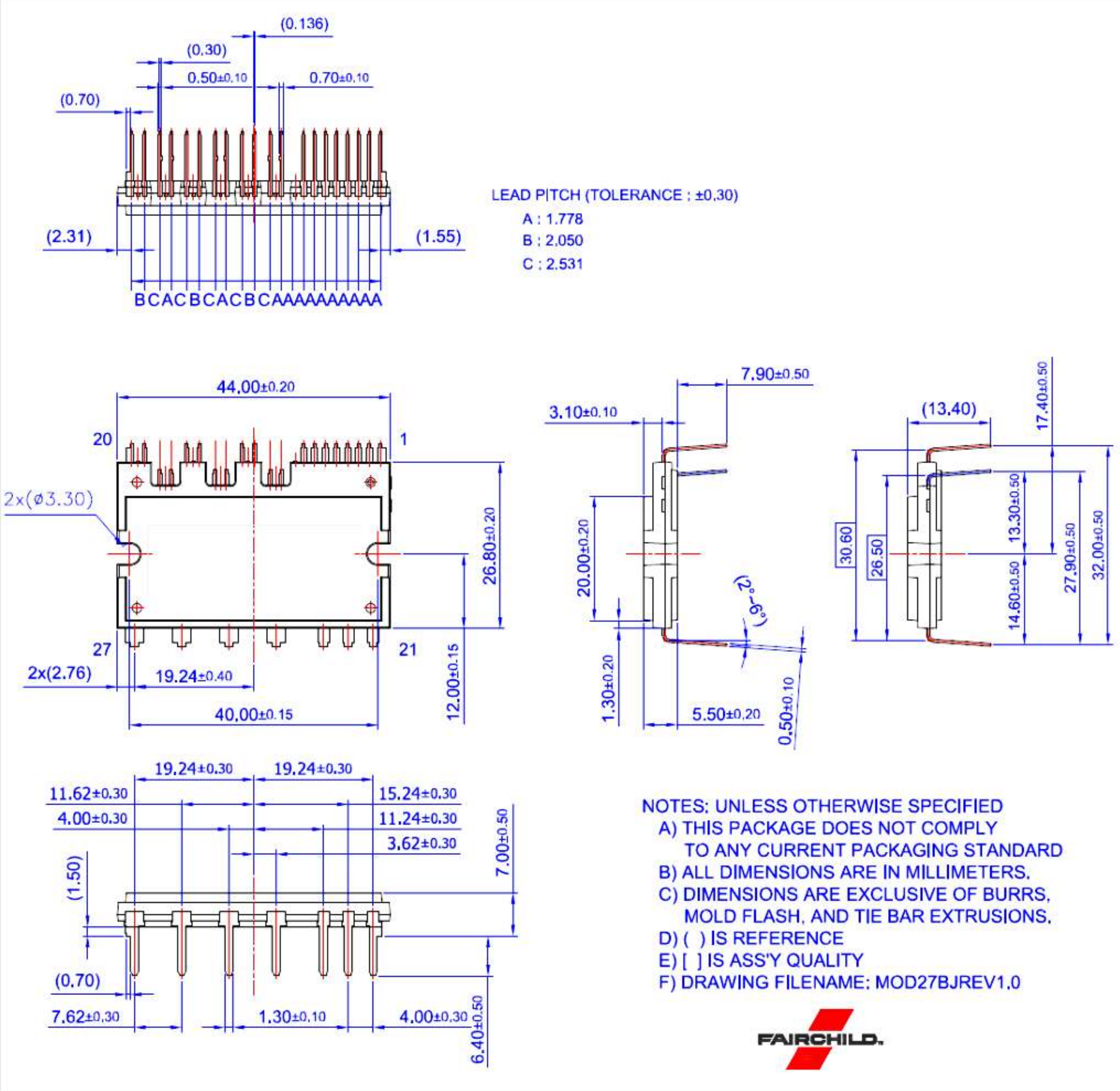
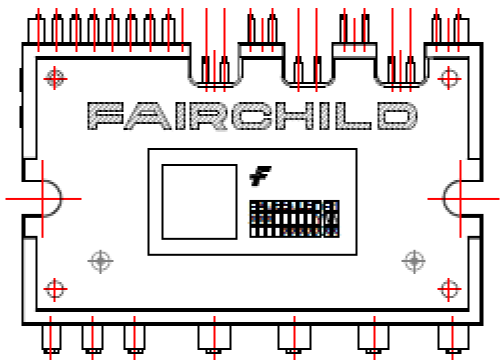


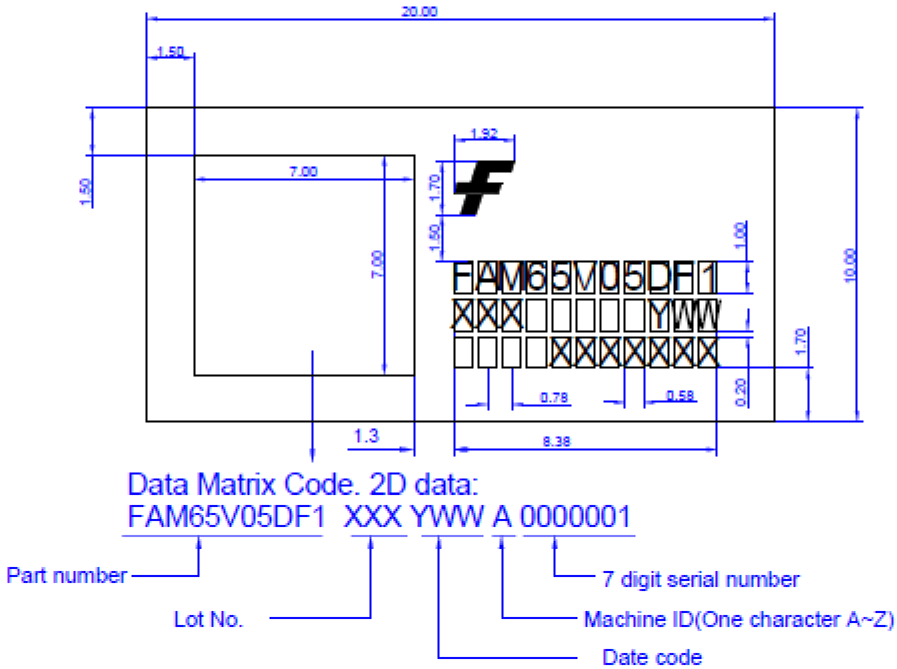
Figure 18. Package Drawings

3.5 Marking Information

* MARKING LAY-OUT



* MARKING DIMENSION



X	Alphabet
2010	A
2011	B
2012	C
2013	D
2014	E
2015	F
2016	G
2017	H
2018	J
2019	K
2020	A

Figure 19. Marking Information

Note: Marking pattern shown for final production version, which slightly differ from previous engineering versions.

4 Operating Sequence for Protections

4.1 Short-Circuit Protection (SCP)

The FAM65V05DF1 uses a shunt resistor for short-circuit detection, as shown in *Figure 20*. The low-side driver has a built-in short-circuit protection function. This function senses the voltage to the CSC pin. If this voltage exceeds the $V_{SC(ref)}$ (the threshold voltage trip level of the short-circuit, typical is 0.5 V), a fault signal is asserted and all low side IGBTs are turned off. Typically, the maximum short-circuit current magnitude is gate-voltage dependent: higher gate voltage (V_{CC} & V_{BS}) results in larger short-circuit current. To avoid potential problems, the maximum short-circuit trip level is set below 1.7 times the nominal rated collector current. The short-circuit protection timing chart is given in *Figure 21* and described in *Table 11*.

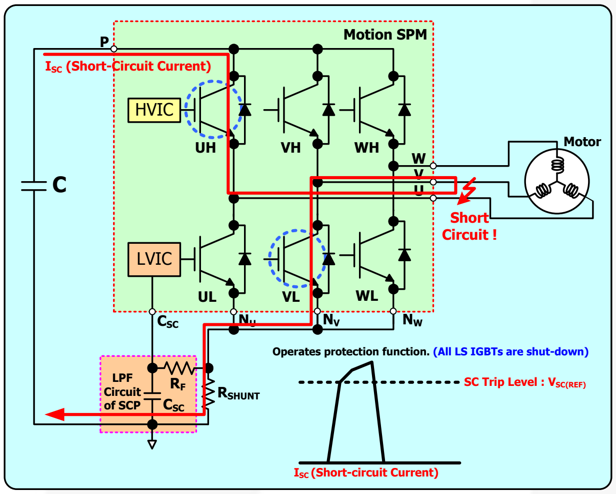


Figure 20. Operation of Short-Circuit Protection

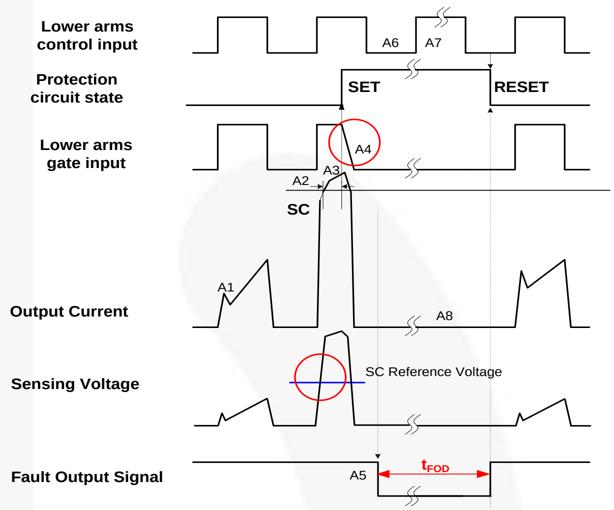


Figure 21. Timing Chart of Short-Circuit Protection Function

Table 11. **Timing Steps for Short-Circuit Protection Function**

Step	Description
A1	Normal operation. IGBT on and carrying current
A2	Short-circuit current threshold reached
A3	Protection function triggered
A4	IGBT turns off with soft turn-off
A5	Fault output activated (initial delay 2 μs, t_{FOD} min. 50 μs)
A6	IGBT “LO” input
A7	IGBT “HI” input is ignored
A8	Current stays at zero during fault state

4.2 Under-Voltage Lockout Protection

Both the low-side driver IC and the high-side driver IC have an Under-Voltage Lockout (UVLO) protection function to protect the IGBTs from operation with insufficient gate driving voltage. The low-side UVLO status is indicated with the fault output, while the high-side does not have a fault output. If the developer experiences unexpected shutdowns without an indication on the fault output, it is recommended to check the high side V_{CC} and V_B. The UVLO timing is illustrated in *Figure 22* and *Figure 23*. The timing steps are described in *Table 12* and *Table 13*.

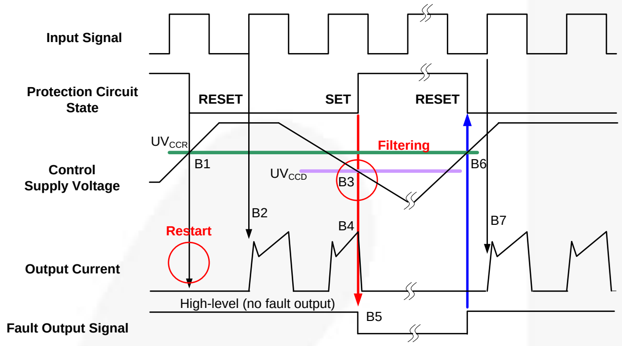


Figure 22. Timing Chart of Low-Side Under-Voltage Protection Function

Table 12. **Timing Steps for Low-Side Under-Voltage Protection Function**

Step	Description
B1	Control supply voltage rises above reset voltage UV_{CCR}
B2	Normal operation. IGBT on and carrying current
B3	Control supply voltage falls below detection voltage UV_{CCD}
B4	Filtered supply voltage falls below UV_{CCD} and IGBT turns off
B5	Fault output activated (initial delay 2 µs, t_{FOD} min. 50µs)
B6	Control supply voltage rises above reset voltage UV_{CCR}
B7	IGBT “HI” input is followed after fault output duration and supply voltage rise

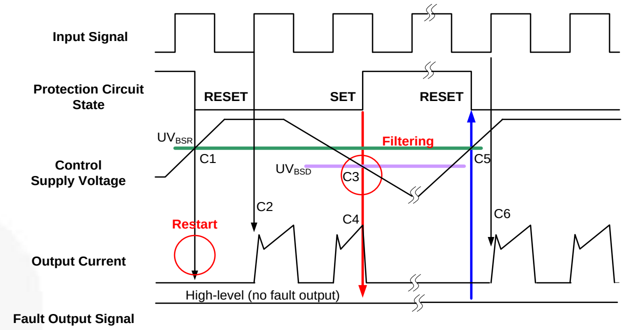


Figure 23. Timing Chart of High-Side Under-Voltage Protection Function

Table 13. **Timing Steps for High-Side Under-Voltage Protection Function**

Step	Description
C1	Control supply voltage rises above reset voltage UV_{CCR}
C2	Normal operation. IGBT on and carrying current
C3	Control supply voltage falls below detection voltage UV_{CCD}
C4	Filtered supply voltage falls below UV_{CCD} and IGBT turns off
C5	Control supply voltage rises above reset voltage UV_{CCR}
C6	IGBT “HI” input is followed after supply voltage rise

5 Key Parameter Design Guidance

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of the FAM65V05DF1.

5.1 Shunt Resistor Selection for Current Sensing & Protection

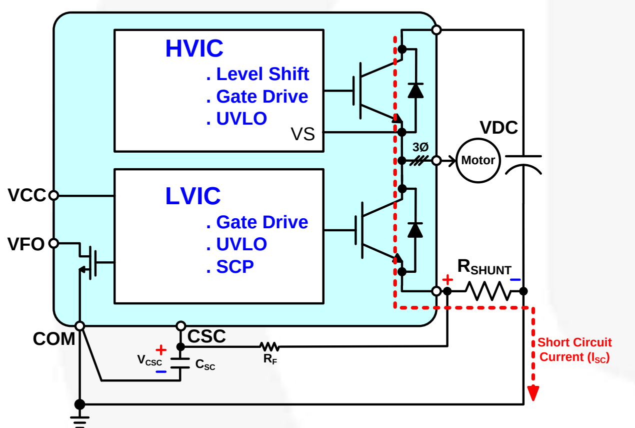
Figure 24 shows examples of recommended circuitry for over-current & short-circuit protection. For simplest operation, the shunt voltage can be connected to the CSC pin through an RC filter (*a*). The RC time constant should be lower than 2 µs to enable shutdown within the short-circuit safe operating area. If multiple shunt resistors are used, a voltage follower circuit may be implemented (*b*).

For best efficiency, it is recommended to connect the “N” power terminals directly to the low-side driver COM terminal (*c*). By adding a shunt between the low-side device emitters and the driver COM, the driver current loop is enlarged. This adds common inductance to the driver loop, which decreases the switching speed and increases device switching losses. In this case, an inverting op-amp circuit should be added to invert the shunt voltage. Using an op-amp circuit also adds the option of choosing the circuit gain. This enables the use of a smaller shunt resistor.

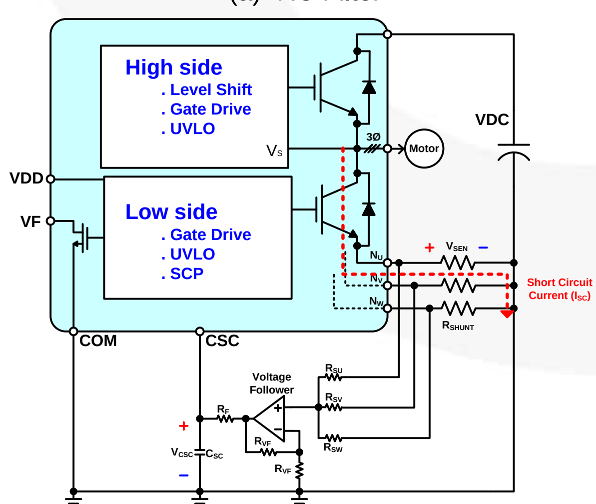
The specifications for the short-circuit reference are shown in *Table 14*.

Table 14. **OCP & SCP Level ($V_{SC(ref)}$) Specification**

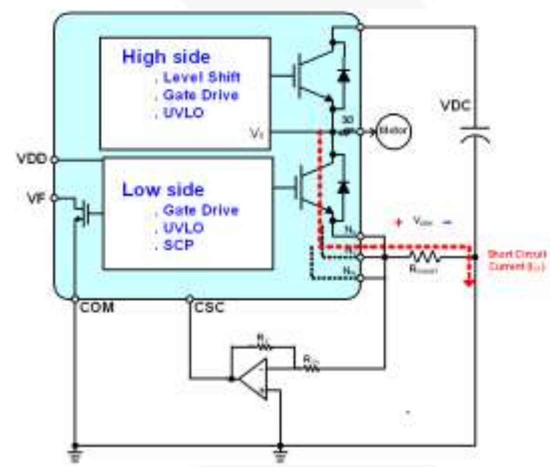
Conditions	Min.	Typ.	Max.	Unit
Specification at T_J=25°C, V_{CC}=15 V	0.43	0.50	0.57	V



(a) RC Filter



(b) Voltage Follower



(c) Recommended Circuit with Inverting Op-amp and Gain

Figure 24. Recommended Circuitry for Over-Current & Short-Circuit Protection

If an op-amp circuit is used to process the shunt voltage (recommended), the filter gain can be selected to choose the desired over-current trip level. The following is an example of shunt resistor selection.

Application Inputs:

- Over- Current Trip Level $I_{SC(max)} = 1.5 \text{ x } I_{C(max)}$
- DC Link Voltage $V_{DC} = 400$ V
- Max. Load Current $I_{RMS} = 25$ A
- Max. Peak Load Current $I_{C(max)} = 50$ A
- Modulation Index   MI = 0.9
- Power Factor   PF = 0.75
- Inverter Efficiency   Eff = 0.95

The following calculations consider a 1 W shunt resistor with 70% de-rating ratio at hot temperature. \An additional 50% safety factor is added to the rating.

- Output Voltage $V_{ll\text{-}rms} = \frac{\sqrt{3}}{\sqrt{2}} \times \text{MI} \times \frac{V_{DC}}{2} = 220.5\text{V}$
- $P_{OUT} = \sqrt{3} \times V_{ll-rms} \times I_{RMS} \times \text{PF}=7.16 \text{ kW}$
- Average DC Current $I_{DC} = P_{OUT}/\text{Eff} / V_{DC}=18.8$ A
- Shunt Resistance = 1.0 W * 70% * 50% / I_{DC}^2 =0.99 mΩ

The op-amp gain resistors (R_F and R_I) can then be set to match the desired trip level. The shunt and gain resistor tolerances can be chosen to match the desired trip tolerance. This example considers 1% tolerance resistors.

- Gain = $R_F / R_I = V_{sc(ref)} / (I_{SC(max)} {*} R_{shunt})=6.67$
- $R_F = 66.5\text{k}\Omega$, $R_{IN} = 10\text{k}\Omega$
- $I_{SC(typ)} = V_{sc(typ)} / (R_{sh(typ)} {*} R_{F(typ)} / R_{IN(typ)})= 75.2$ A
- $I_{SC(max)} = V_{sc(max)} / (R_{sh(min)} {*} R_{F(min)} / R_{IN(max)}) = 88.3$ A
- $I_{SC(min)} = V_{sc(min)} / (R_{sh(max)} {*} R_{F(max)} / R_{IN(min)}) = 62.8$ A

5.2 Shunt Voltage Filtering

Figure 25 shows the timing diagram of the FAM65V05DF1 for Short-Circuit Protection (SCP) circuit operation. Filtering the shunt voltage prevents SCP circuit malfunction. The filter time constant is determined by the applied noise time and the Short-Circuit Withstanding Time (SCWT) of the module. When the V_{CSC} voltage exceeds the SCP level, this is applied to the CSC pin via the filter. The filter delay (T1) is the time required for the CSC pin voltage to rise to the referenced SCP level. The LVIC has an internal filter time (logic filter time for noise elimination: T2). Consider this filter time when designing the filter of V_{CSC}.

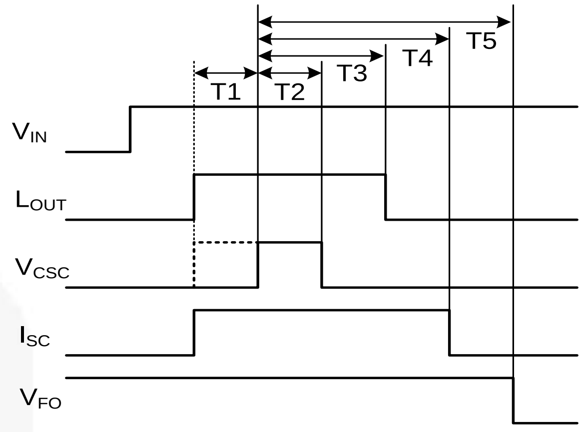


Figure 25. Timing Diagram

- V_{IN}: Voltage of input signal.
- L_{OUT}: V_{GE} of low-side IGBT.
- V_{CSC}: Voltage of CSC pin.
- I_{SC}: Short-circuit current.
- V_{FO}: Voltage of VFO pin.
- T1: filtering time of RC filter of V_{CSC}.
- T2: filtering time of CSC. If V_{CSC} width is less than T2, SCP does not operate.
- T3: delay from CSC triggering to gate-voltage down.
- T4: delay from CSC triggering to short-circuit current.
- T5: delay from CSC triggering to fault-out signal.

Table 15. **Over-Current Timing**

Typ. at T_J=25°C	Typ. at T_J=150°C	Max. at T_J=25°C
T2=0.25 μs	T2=0.09 μs	Considering ±20% Dispersion, T4=3.6 μs
T3=0.62 μs	T3=0.57 μs	
T4=3 μs	T4=3.3 μs	
T5=4.1 μs	T5=4.25 μs	

Note:

3. To guarantee safe short-circuit protection under all operating conditions, C_{SC} should be triggered within 1.0 μs after short-circuit occurs. (SCWT < 5.0 μs, Conditions: V_{DC}=450 V, V_{CC}=15 V, TJ=150°1).

5.3 Soft Turn-Off

The LVIC soft turn-off function protects the low side IGBTs from over-voltage during a short-circuit turn-off condition. During a short circuit, a large dI/dt of the collector current causes a large surge voltage across the IGBT. This surge voltage can cause destruction of the IGBT by over-voltage. The soft turn-off function prevents this by slowly discharging V_{GE} (gate-to-emitter voltage of IGBT).

An internal block diagram of LVIC is shown in *Figure 26*. The operation sequence of soft turn-off is shown in *Figure 27*. This function operates by two internal protection functions (UVLO and SCP). When the IGBT is turned off in normal conditions, the LVIC turns off the IGBT immediately by turn-off gate signal (IN(xL)) of the gate driver. The gate is discharged through the output buffer ①. When the IGBT is turned off by a protection function, the gate driver is disabled by the protection function signal and the protection circuit enables the soft-off function. V_{GE} (IGBT gate-emitter voltage) is discharged slowly through the soft turn-off path ②.

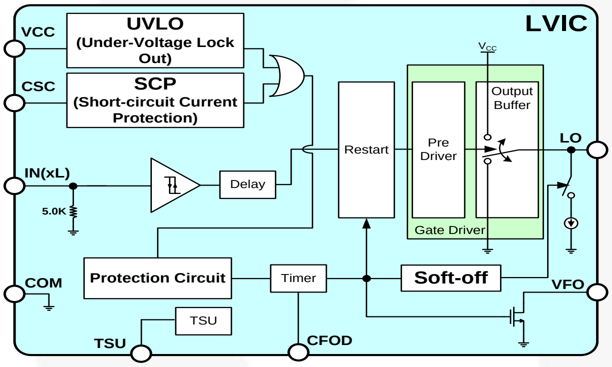


Figure 26. Internal Block Diagram of LVIC

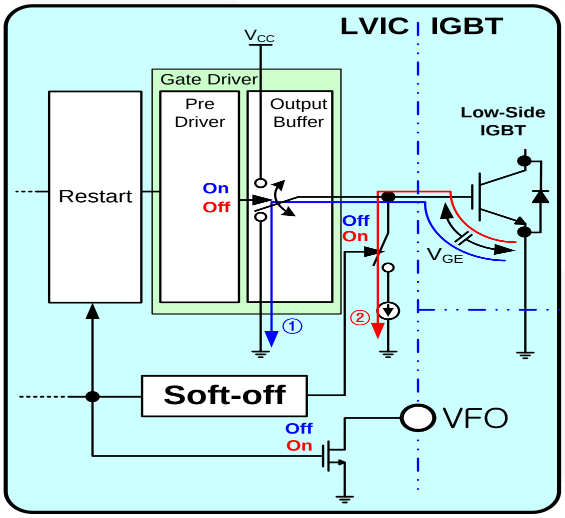


Figure 27. Operating Sequence of Soft Turn-Off

Figure 28 shows a normal turn-off switching operation performed at V_{DC} = 450 V. *Figure 29* shows a turn-off event that is triggered by the soft turn-off function. The hard turn-off of the IGBT creates a much larger overshoot (77 V compared to 10 V).

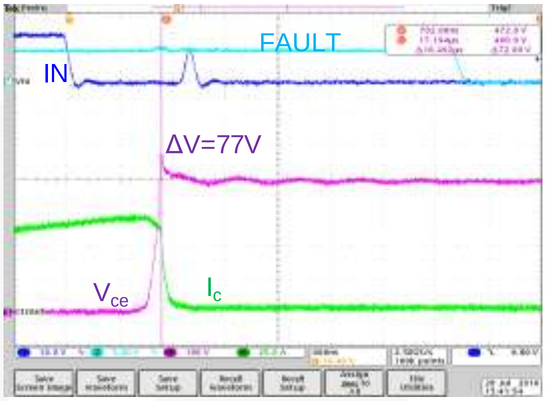


Figure 28. Turn-Off by Input
(FAM65V05DF1, V_{DC}=450 V, T_J=25°C, I_C=70 A)

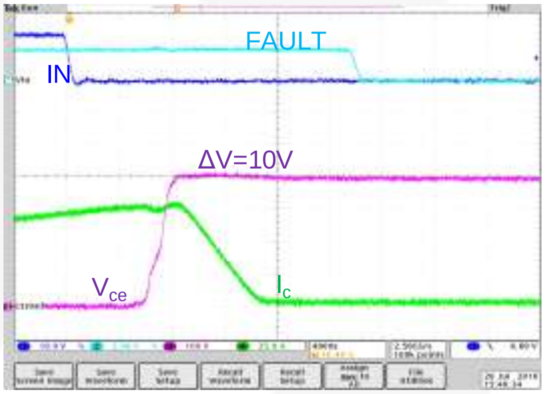


Figure 29. Turn-Off by Soft-Off Function
(FAM65V05DF1, V_{DC}=450 V, T_J=25°C, I_C=75 A)

5.4 Fault Output Circuit

The fault-output pin is open-drain configured, so an appropriate pull-up resistor should be used. The following information can be used to determine the fault-output configuration.

Table 16. **Fault-Output Maximum Ratings**

Symbol	Item	Condition	Rating	Unit
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO}-COM	-0.3 ~ V_{CC}+0.3	V
I_{FO}	Fault Output Current	Sink Current at VFO Pin	2	mA

Table 17. **Fault-Output Characteristics**

Symbol	Item	Conditions	Min.	Max.	Unit
V_{FOH}	Fault Output Supply Voltage	V_{CC}=15 V, V_{SC}=0, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-Up	4.5		V
V_{FOL}		V_{CC}=15 V, V_{SC}=1 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-Up		0.5	V

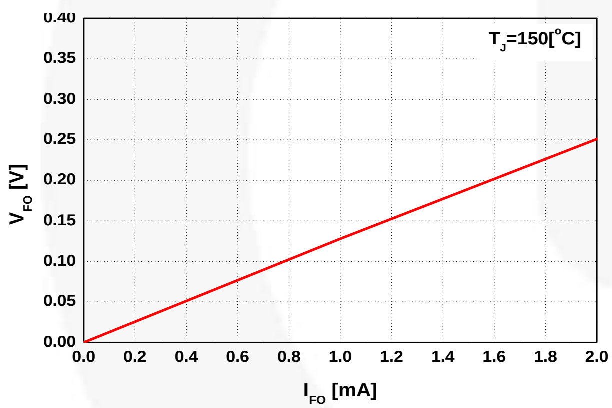


Figure 30. Voltage-Current Characteristics of V_{FO} Terminal

5.5 Circuit of Input Signal (IN(xH), IN(xL))

Figure 31 shows the I/O interface circuit between the MCU and FAM65V05DF1 product. Because the input logic is active HIGH and there are built-in pull-down resistors, external pull-down resistors are not needed.

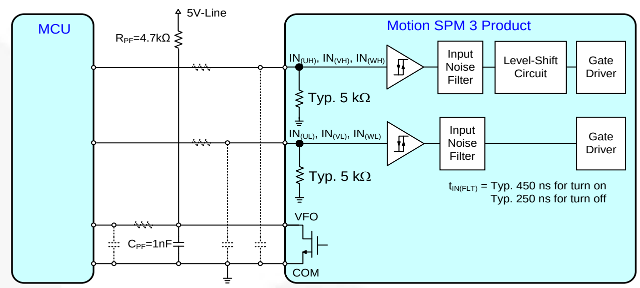


Figure 31. Recommended MCU I/O Interface Circuit

The input and fault-output maximum rated voltages are shown in *Table 18*. Since the fault-output is open drain, its rating is V_{CC}+0.3 V, and 15 V supply interface is possible. However, it is recommended that the fault output be configured with the same supplies as the input signals. It is also recommended that the de-coupling capacitors be placed at both the MCU and FAM65V05DF1 ends of the V_{FO} signal line, as close as possible to each device. The RC coupling at each input (parts shown dotted in *Figure 31*) can be changed depending on the PWM control scheme used in the application and the wiring impedance of the PCB layout.

The input signal section of the FAM65V05DF1 integrates a 5 kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between the MCU output and the module series input, attention should be given to the signal voltage drop at the module input terminals to satisfy the turn-on threshold voltage requirement. For instance, R = 100 Ω and C = 1 nF for the parts shown dotted in *Figure 31*.

Table 18. **Maximum Ratings of Input and VFO Pins**

Symbol	Item	Condition	Rating	Unit
V_{IN}	Input Signal Voltage	Applied between $IN_{(xH)}$, $IN_{(xL)}$ - COM(x)	-0.3 ~ V_{CC} +0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO}-COM(L)	-0.3 ~ V_{CC} +0.3	V

Table 19. **Input Threshold Voltage Ratings (V_{CC}=15 V, T_J=25°C)**

Symbol	Item	Condition	Min.	Max.	Unit
$V_{IN(ON)}$	Turn-On Threshold Voltage	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ - COM(H)		2.6	V
$V_{IN(OFF)}$	Turn-Off Threshold Voltage	$IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM(L)	0.8		V

5.6 Bootstrap Circuit Design

5.6.1 Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between V_B (U, V, W) and V_S (U, V, W), provides the supply to the HVIC within the FAM65V05DF1. This supply must be in the range of 13.0 V~18.5 V to ensure that the HVIC can fully drive the high-side IGBT. The under-voltage lockout protection for V_{BS} ensures that the HVIC does not drive the high-side IGBT if the V_{BS} voltage drops below a specific voltage (refer to the datasheet). This function prevents the IGBT from operating in a high-dissipation mode.

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here. This method has the advantage of being simple and inexpensive. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of a bootstrap diode, resistor, and capacitor. The current path of the bootstrap circuit is shown in *Figure 32*. When V_S is pulled down to ground (low-side IGBT turn-on or low-side FRD freewheeling), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{CC} supply.

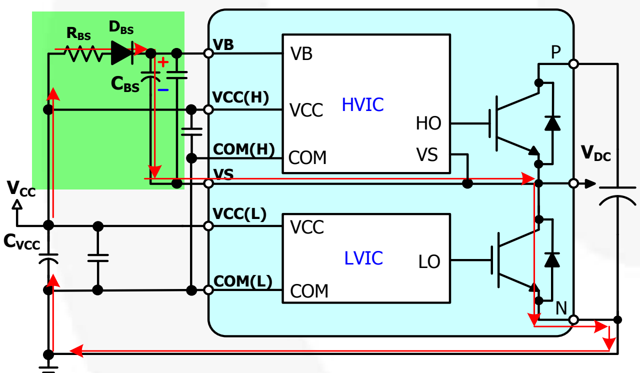


Figure 32. Current Path of Bootstrap Circuit for the Supply Voltage (V_{BS}) of HVIC with Low-Side IGBT On

5.6.2 Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on-time of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated by:

$$t_{charge} = C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln \frac{V_{CC}}{V_{CC} - V_{BS(min)} - V_F - V_{LS}} \qquad (2)$$

where:

V_F = Forward voltage drop across the bootstrap diode

$V_{BS(min)}$ = The minimum value of the bootstrap voltage

C_{BS} = Value of the bootstrap capacitor

V_{LS} = Voltage drop across the low-side IGBT or load

δ = Duty ratio of PWM (0 ~ 1).

The bootstrap capacitor is charged from the V_{CC} line while the low-side IGBT is turned on. Before normal PWM operation begins, the low-side IGBT on-time should be sufficient to fully charge the bootstrap capacitor. If V_{CC} voltage discharges to UV_{CCD} level, the low side is shut down and a fault signal is activated. To reduce V_{CC} voltage drop at initial charging, a large V_{CC} source capacitor and using a strategic start-up sequence is recommended.

Figure 33 shows an example of initial bootstrap charging sequence. Once V_{CC} is charged, V_{BS} needs to be charged by turning on the low-side IGBTs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency. Therefore, it is desired to maintain this structure without creating complementary high-side PWM signals. The capacitance of V_{CC} should be sufficient to supply necessary charge to V_{BS} capacitance in all three phases. If a normal PWM operation starts before V_{BS} reaches V_{UVLO} reset level, the high-side IGBTs cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications.

The effects of the bootstrap charging sequence are shown in *Figure 34*. With proper capacitor sizing, the low-side inputs can be turned on to charge the bootstrap capacitors *(a)*. Alternatively, each phase may be charged individually *(b)*. Poor capacitor sizing can cause V_{CC} discharge and a fault condition *(c)*. If using a PWM startup sequence, longer charge time will be required (*(d) & (e)*).

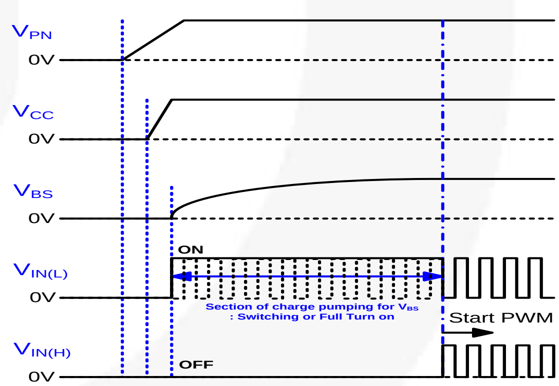
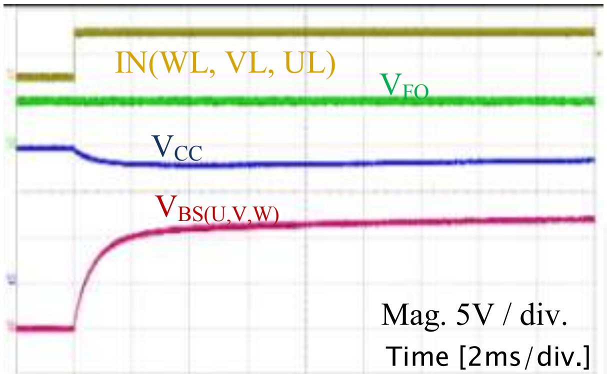
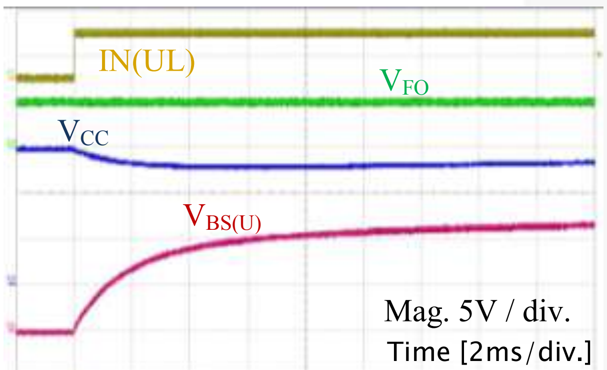


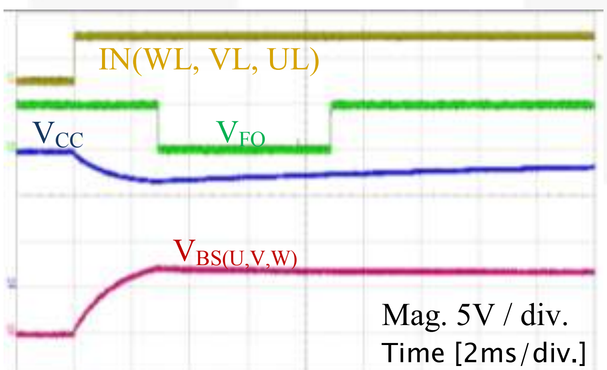
Figure 33. Timing Chart of Initial Bootstrap Charging



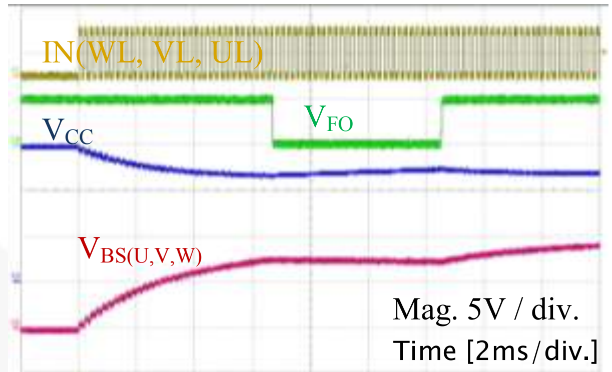
(a) Low-Side Turn-On, C_{BS}=33 µF



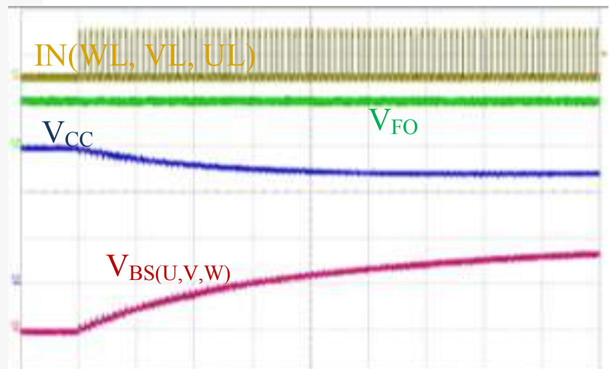
(b) Single Low-Side Turn-On, C_{BS}=100 µF



(c) All Low-Side Turn-On, C_{BS}=100µF



(d) 50% PWM Low-Side Turn-On, C_{BS}=100 µF



(e) 25% PWM Low-Side Turn-On, C_{BS}=100 µF

Figure 34. Recommended Initial Bootstrap Capacitors Charging Sequence (Reference Condition: V_{CC}=15 V, V_{CC} Capacitor=220 µF, R_{BS}=20 Ω)

5.6.3 Selection of Bootstrap Capacitor Considering Operation Conditions

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} \tag{3}$$

where:
Δt: maximum on pulse width of high-side IGBT
ΔV_{BS}: the allowable discharge voltage of the C_{BS} (voltage ripple)
I_{Leak}: maximum discharge current of the C_{BS}.

The leakage current comes mainly from the following mechanisms:

- Gate charge for turning the high-side IGBT on
- Quiescent current to the high-side circuit in HVIC
- Level-shift charge required by level-shifters in HVIC
- Leakage current in the bootstrap diode
- C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)
- Bootstrap diode reverse recovery charge

Practically, 4.5 mA of I_{Leak} is recommended for the Auto SPM® products (see datasheet I_{PBS} value). By considering dispersion and reliability, the capacitance is generally selected to be 2~3 times the calculated one. The C_{BS} is only charged when the high-side IGBT is off and the $V_{S(x)}$ voltage is pulled down to ground.

The on-time of the low-side IGBT must be sufficient for the charge drawn from the C_{BS} capacitor to be fully replenished. This creates an inherent minimum on-time of the low-side IGBT (or off-time of the high-side IGBT). Below is an example calculation of minimum bootstrap capacitance. Note that this value can change depending on the switching frequency, selected capacitor, V_{BS} voltage, and control method. *Figure 35* extends the calculation to a range of switching frequencies.

Based on switching frequency and recommended ΔV_{BS}

- I_{Leak}: circuit current = 4.5 mA (recommended value)
- ΔV_{BS}: discharged voltage = 0.1 V (recommended value)
- Δt: maximum on pulse width of high-side IGBT = 0.1 ms (depends on application)

$$C_{BS\_min} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} = \frac{4.5\text{mA} \times 0.1\text{ms}}{0.1\text{V}} = 4.5 \times 10^{-6} \tag{4}$$

→ More than 2 times → 10~22 μF

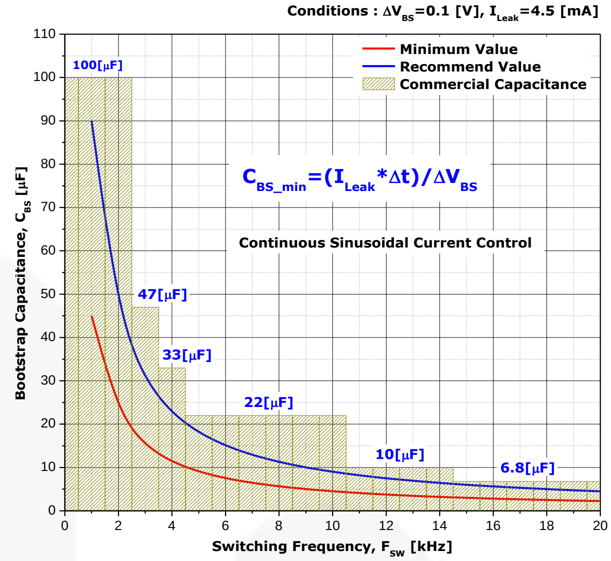


Figure 35. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

To avoid unexpected under-voltage protection and to keep V_{BS} within recommended value, bootstrap capacitance should be selected based on the operating conditions. Bootstrap voltage ripple is influenced by the bootstrap resistor, load condition, output frequency, and switching frequency. Check the voltage ripple during the maximum load condition in the system. *Figure 36* shows an example of $V_{B(x)}$-$V_{S(x)}$ ripple voltage during operation.

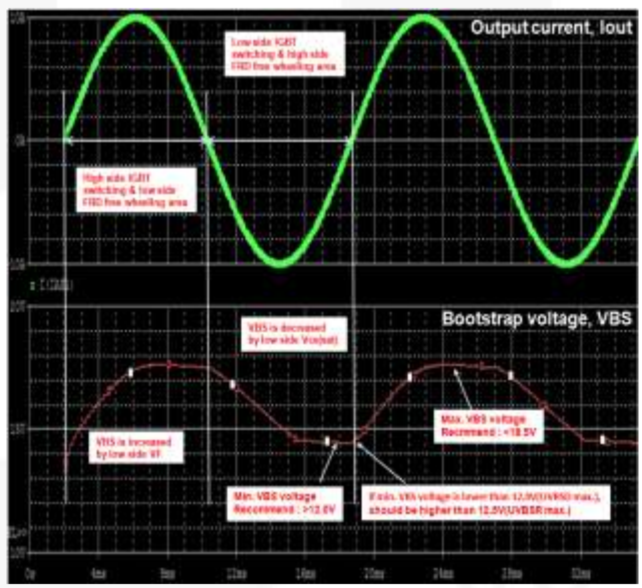


Figure 36. Bootstrap Ripple Voltage During Operation

5.6.4 Selection of Bootstrap Diode

When a high side IGBT or diode conducts, the bootstrap diode (D_{BS}) supports the entire bus voltage. A withstand voltage of at least 600 V and automotive grade is recommended. It is important that the diode should be a fast recovery device (recovery time < 100 ns) to minimize the amount of charge that is fed back from the bootstrap capacitor into the V_{CC} supply. Similarly, the high voltage reverse leakage current is important if the capacitor has to store a charge for long periods of time.

5.6.5 Selection of Bootstrap Resistor

A resistor R_{BS} must be added in series with the bootstrap diode to slow down the dV_{BS}/dt and to limit inrush current at initial C_{BS} charging. It also determines the time to charge the bootstrap capacitor. That is, if the minimum ON pulse width of low-side IGBT or the minimum OFF pulse width of high-side IGBT is t_O, the bootstrap capacitor has to be charged ΔV during this period. Therefore, the value of bootstrap resistance can be calculated by the following equation.

$$R_{BS} = \frac{(V_{DD} - V_{BS}) \times t_O}{C_{BS} \times \Delta V_{BS}} \tag{5}$$

For the selection of R_{BS}, pulse power rating should be considered for initial charging of bootstrap capacitor. To use a large bootstrap capacitor, high pulse power rating is required for the bootstrap resistor. An example of resistor pulse power rating is shown in *Figure 38*.

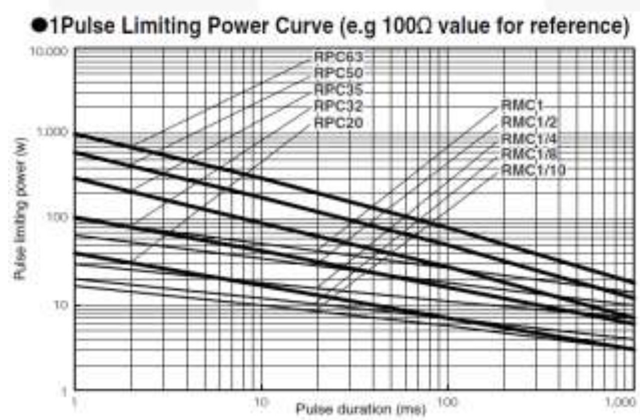


Figure 38. Example of Pulse Power Curve of Resistor (from Kamaya Ohm)

5.7 Thermal Sensing Unit (TSU)

The junction temperature of power devices should not exceed the maximum junction temperature. Even though there is some margin between the $T_{J\text{-}MAX}$ specified on the datasheet and the $T_{J\text{-}MAX}$ at which power devices are destroyed, attention should be paid to ensure the junction temperature stays well below the $T_{J\text{-}MAX}$. The Thermal Sensing Unit (TSU) helps to ensure device safety by providing feedback of the module temperature.

The TSU uses the temperature dependency of transistor V_{BE}, which decreases 2 mV for each 1ºC change in temperature. The sensed value reflects the temperature of the LVIC, as shown in *Figure 39*. The relationship between V_{TS} voltage output and LVIC temperature is shown in *Figure 40*.

The TSU does not have any self-protection function therefore it should be used appropriately based on application requirement. Also, there is a time lag from IGBT temperature to LVIC temperature. The TSU will not respond quickly to a transient high-temperature event such as IGBT shoot-through. Despite this limitation, it is a useful feature to enhance system reliability.

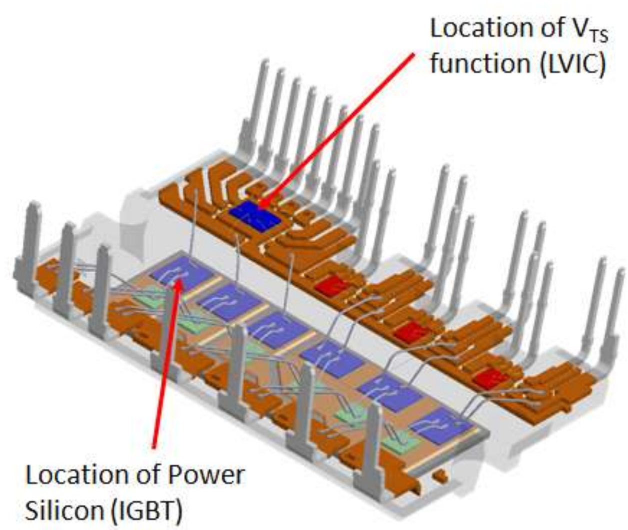


Figure 39. Location of V_{TS} Function (LVIC)

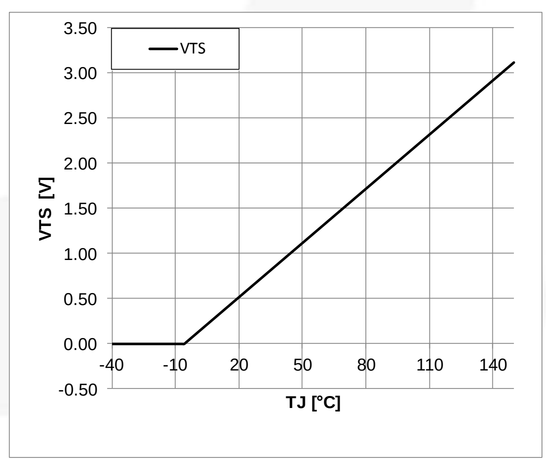


Figure 40. LVIC Temperature vs. V_{TS}

Figure 41 shows the equivalent circuit diagram of the TSU IC with a typical application diagram. The output voltage is clamped to 5.2 V by an internal Zener diode. In case the maximum input range of the MCU Analog to Digital converter is below 5.2 V, an external Zener diode should be inserted between the A/D input pin and the analog ground pin of MCU. An amplifier can be used to change the range of voltage input to the A/D converter to have better resolution of the temperature. It is recommended to add a ceramic capacitor of 1000 pF between V_{TS} and COM to make the V_{TS} output more stable.

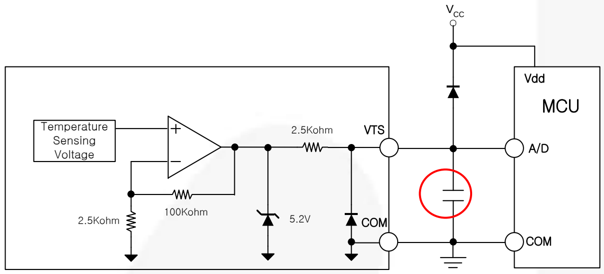


Figure 41. Internal Block Diagram and Interface of TSU

Figure 42 shows the sourcing capability of the V_{TS} pin at 25ºC and the test method used. V_{TS} voltage decreases as the sourcing current increases. Therefore, the load connected to V_{TS} pin should be minimized to maintain the accurate voltage output level without degradation. The relationship between V_{TS} voltage and LVIC temperature can be expressed as the following equations:

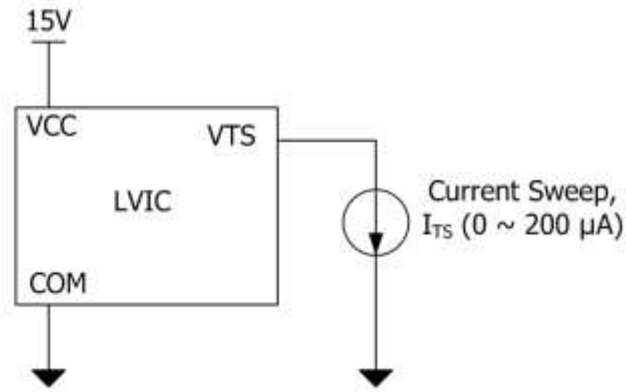
$$V_{TS,min} = 0.02*T_{LVIC} + 0.119 - 0.091 \text{ [V]} \tag{6}$$

$$V_{TS,typ} = 0.02*T_{LVIC} + 0.119 \text{ [V]} \tag{7}$$

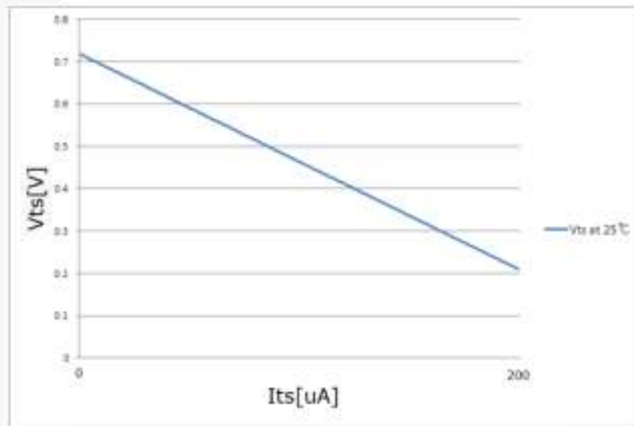
$$V_{TS,max} = 0.02*T_{LVIC} + 0.119 + 0.126 \text{ [V]} \tag{8}$$

In case of FAM65V05DF1, the maximum variation of V_{TS} is {-0.091 V, +0.126 V}. This is due to process variation which is approximately equivalent to ±5ºC. If the ambient temperature information is available, for example from an NTC, V_{TS} can be measured to adjust the offset before the motor starts to operate.

As temperature decreases below 0ºC, V_{TS} decreases linearly until it reaches zero volts. If the temperature of LVIC increases above 150ºC, which is above the maximum operating temperature, V_{TS} would increase to 5.2 V until it gets clamped by the internal Zener diode.



(a) Test Methods.



(b) Test Result

Figure 42. Load Variation of V_{TS}

6 Printed Circuit Board (PCB) Design

6.1 General Application Circuit Example

Figure 43 shows a general application circuitry of interface schematic with control signals connected directly to a MCU.

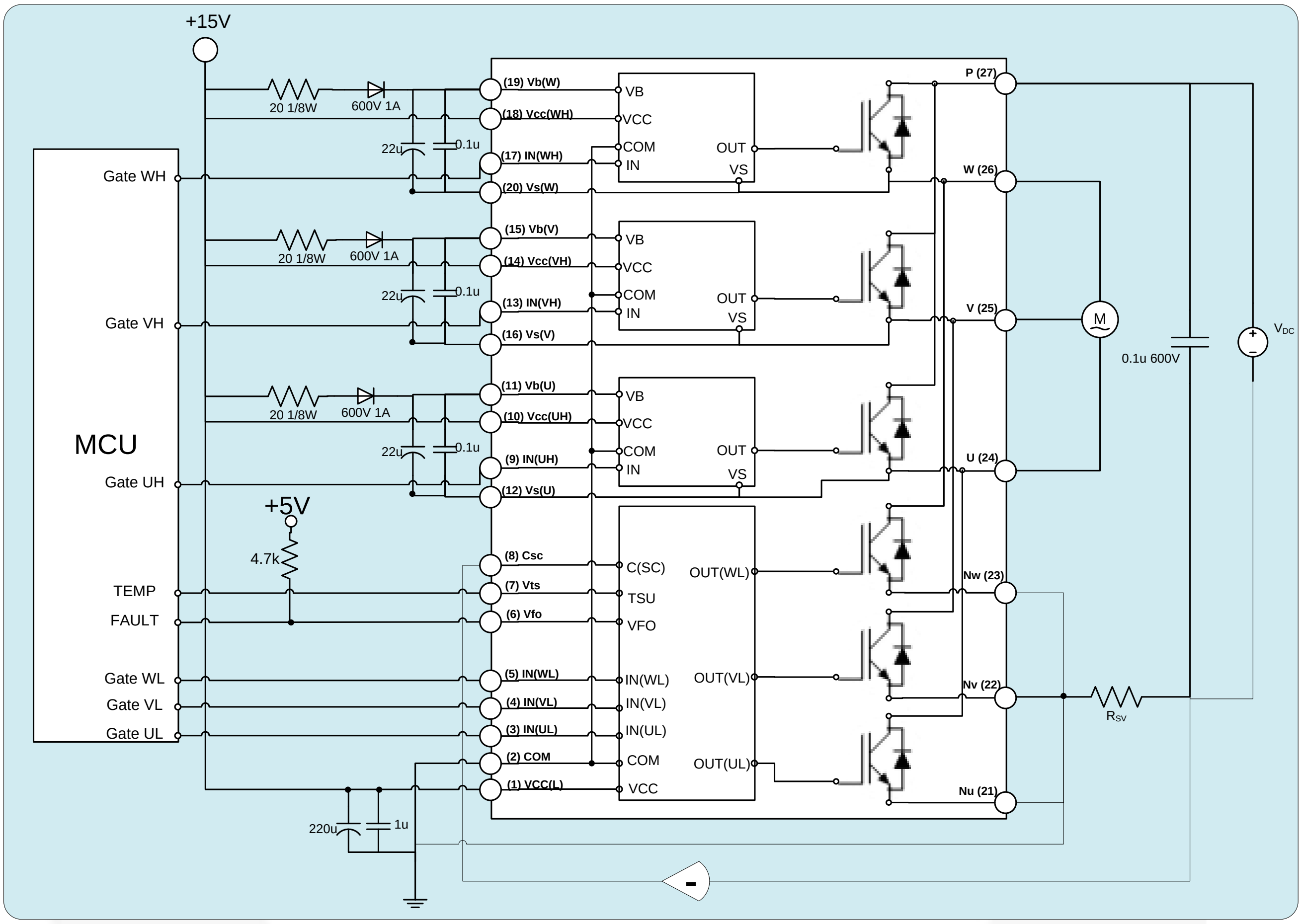


Figure 43. General Application Circuitry for Auto SPM® Module

6.2 PCB Layout Guidance

Figure 44 provides suggestions regarding PCB layout for the FAM65V05DF1.

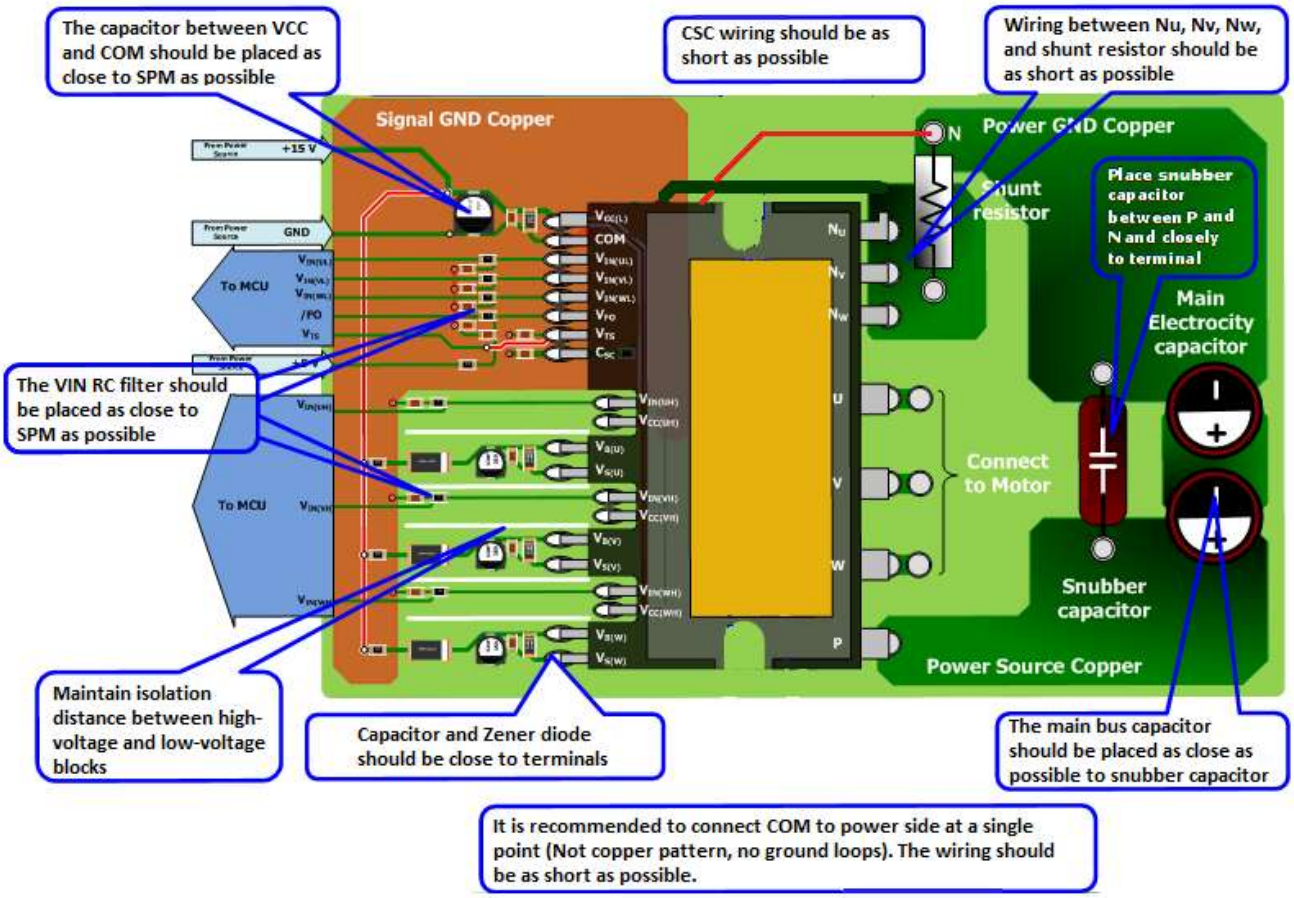
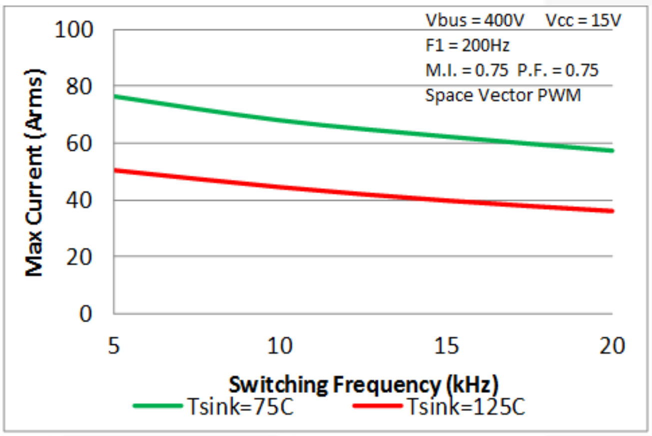


Figure 44. Printed Circuit Board Layout Guidance for FAM65V05DF1

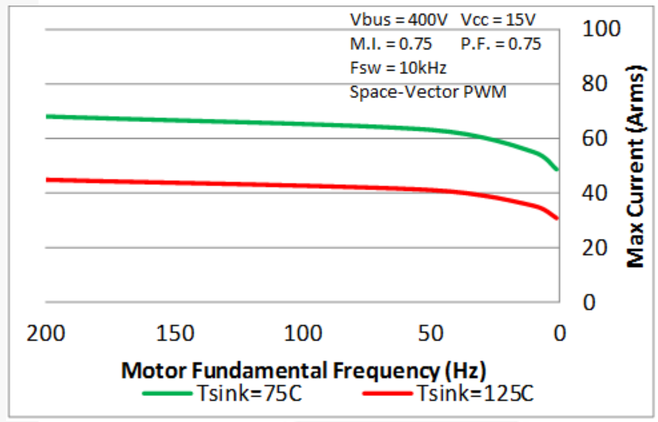
7 Maximum Application Current

The basic requirement for maximum load current is that the junction temperature of each device stays below the maximum of 175°C. For motor applications this is a function of many different operating parameters, such as: battery voltage, heat-sink temperature, thermal interface material, modulation index, PCB layout, motor power factor, and motor speed. It is important to use good PCB layout and cooling system design in order to achieve the best performance.

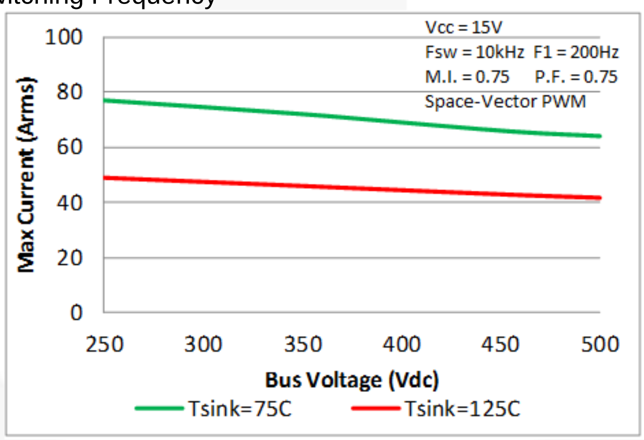
Figure 45 shows examples of how the maximum current changes with different operating parameters. The thermal system was defined by setting the heat-sink to a constant temperature, with 50 µm of thermal interface material between the heat-sink and module (typical 2 W/mK material). The junction temperature was calculated by using the cross-coupled thermal model of a typical package, including an additional 2% solder void in the center of each die.



(a) Variation with Switching Frequency



(b) Variation with Fundamental Frequency

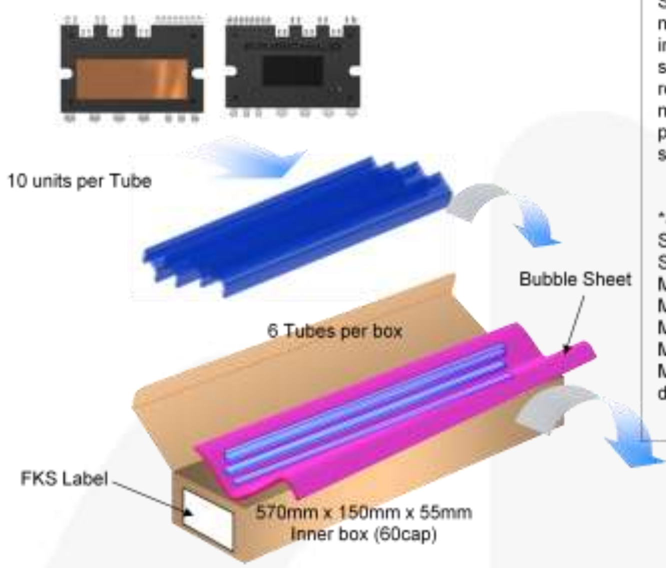


(c) Variation with Bus Voltage

Figure 45. Max. Current vs. Application Conditions

8 Packing Information

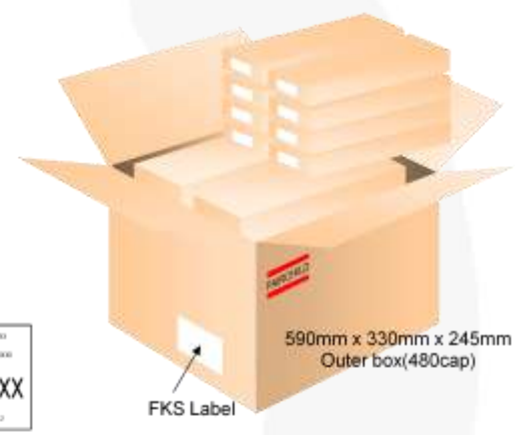
SPMCA-027 Tube Packing Configuration: Figure 1.0



Packaging Description:

SPMCA-027 parts are shipped normally in tube. The tube is made of PVC plastic treated with anti-static agent. These tubes in standard option are placed inside a dissipative plastic bubble sheet, barcode labeled, and placed inside a box made of recyclable corrugated paper. One box contains six tubes maximum (see fig. 1.0). And one or several of these boxes are placed inside a labeled shipping box which comes in different sizes depending on the number of parts shipped.

*SPMCC-027(PKG-MOD27BA),SPMCD-027(PKG-MOD27BA), SPMCE-027(PKG-MOD27BB),SPMCF-027(PKG-MODBD), SPMCG-027(PKG-MOD27BC),SPMEA-027(PKG-MOD27BA),SPMEC-027(PKG-MOD27BA), SPMGA-027(PKG-MOD27BA), SPMGC-027(PKG-MOD27BA), SPMHA-027(PKG-MOD27BA), SPMHC-027(PKG-MOD27BA), SPMIA-027(PKG-MOD27BA), SPMIC-027(PKG-MOD27BA),SPMMA-027(PKG-MOD26BC), SPMMB-027(PKG-MOD26BD) also use packing data.



SPMCA-027 Packaging Information: Figure 2.0

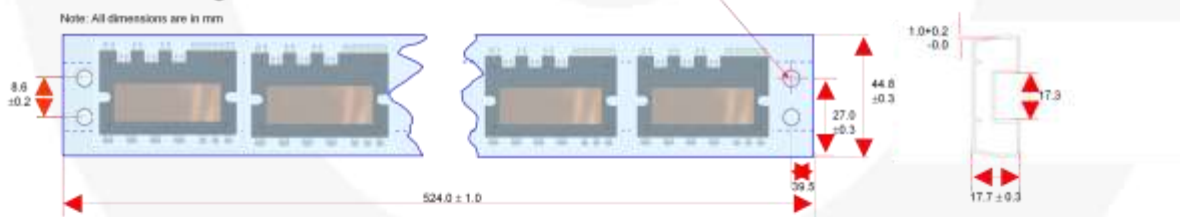
SPMCA-027 Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	10
Inner Box Dimension (mm)	570x150x55
Max qty per Box	60
Outer Box Dimension (mm)	590x330x245
Max qty per Box	480
Weight per unit (gm)	-
Note/Comments	

Inner Box Barcode Label Sample

Outer Box Barcode Label Sample

SPMCA-027 Tube Information: Figure 3.0

Note: All dimensions are in mm



NOTES:

A : ALL DIMENSION ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED

B : DRAWING FIEL NAME : PKG-MOD27BAREV1

Figure 46. **Packing Information**

Related Resources

FAM65V05DF1 – Product Datasheet

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
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