Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Table of Contents

AN-9112

Smart Power Module Motion SPM® 8 Series Application Note

ON Semiconductor®

www.onsemi.com

APPLICATION NOTE

1 Introduction

This application note supports the Motion SPM® 8 series. It should be used in conjunction with the Motion SPM 8 series datasheets, Fairchild's Motion SPM evaluation board user guides, and application notes which can be found on the web pages of which links are listed in *Section 9 Related Resources*.

1.1 Design Concept

The Motion SPM 8 series was developed to provide a minimized package and low power consumption with improved reliability. This is achieved by applying a new 600 V gate-driving High-Voltage Integrated Circuit (HVIC), a new Insulated-Gate Bipolar Transistor (IGBT) of advanced silicon technology. Motion SPM 8 series achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are inverterized motor drives for low power motor drives, such as fans, pumps, refrigerators, washing machines, etc.

The temperature sensing function is implemented in drive IC to enhance the system reliability. The temperature of the drive IC is provided for monitoring the module temperature and necessary protections against over-temperature situations. Most customers want to know the exact temperature of power chips because temperature affects the quality, reliability, and longevity of the products. The temperature sensing function of the Motion SPM 8 series helps to measure internal temperature in module effectively and easily. In addition, a bootstrap circuit is integrated in the driver for driving high side IGBTs.

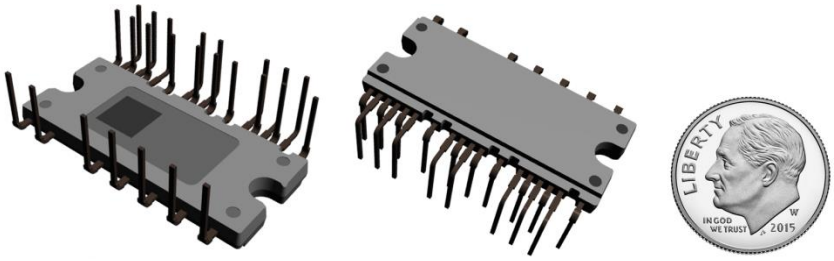


Figure 1. External View and Internal Structure of Motion SPM 8 Series

Table 1. Product Line-up and Target Application

Fairchild Device	IGBT Rating	Motor Rating(1)	Target Application	Isolation Voltage
FNB80460Tx	4 A / 600 V	0.3 kW / 220 V_{AC}	HVAC, Pumps, Home Appliances, Low-Power Industrial Inverter	V_{ISO} = 1500 V_{RMS} (Sine 60 Hz, 1-min between All Shorted Pins and Heat Sink)
FNB80560Tx	5 A / 600 V	0.4 kW / 220 V_{AC}		
FNB81060Tx	10 A / 600 V	0.75 kW / 220 V_{AC}		

Notes:

1. These motor ratings are simulation results under the following conditions: V_{AC} = 220 V, V_{DD} = 15 V, T_C = 100°C, T_J = 150°C, PF=0.8, MI=0.9, Motor efficiency=0.75, overload 150% for 1min.
   These motor ratings are general ratings, so may change by conditions.
2. An online loss and temperature simulation tool, Motion Control Design Tool (*https://www.fairchildsemi.com/design/design-tools/motion-control-design-tool/*), is recommended for choosing the right SPM product for the application.

1.2 Ordering Information

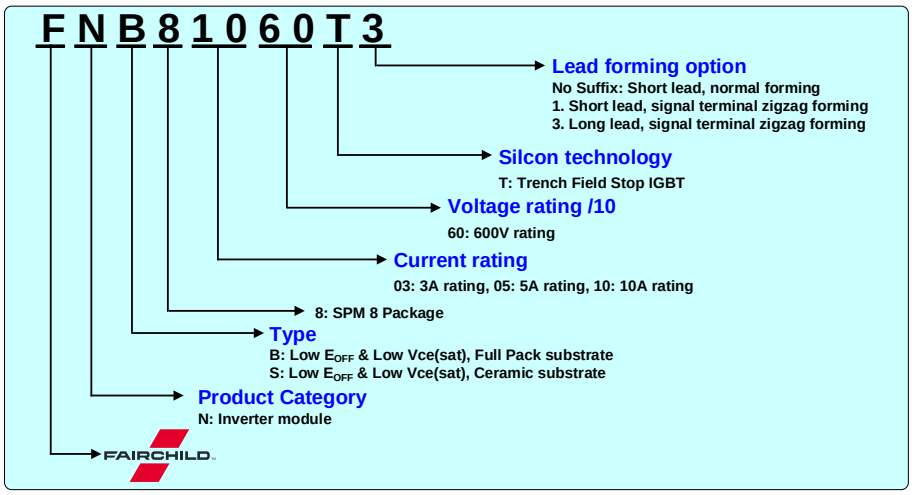


Figure 2. Ordering Information

1.3 Features and Integrated Functions

- Full Mold Package
  - 1500 Vrms Isolation Voltage from Pins to Heat Sink
- Integrated Components:
  - Three Half Bridge Gate Drive ICs for High and Low Side IGBTs Control
  - Six IGBTs / Diodes
- Single DC Supply can be used with internal Bootstrap Circuit
- Features and Functions
  - Low-Loss, Short-Circuit Rated IGBTs
  - High-Voltage Level-Shift Circuit
  - Input Interface: Active HIGH
  - Works with 3.3 / 5 V Controller Outputs
  - High-Side Supply Voltage Under-Voltage Lockout without Fault Signal
  - Low-Side Supply Voltage Under-Voltage Lockout with Fault Signal
  - Short-Circuit and Over-Current Protection By Detecting Sense Current from External Resistor
  - Temperature Sensing
  - Shut Down Function
  - Inter-Lock Function
  - Soft Turn-off to Prevent Excessive Surge Voltage
  - Open Emitter Configuration for Current Sensing of Each Phase

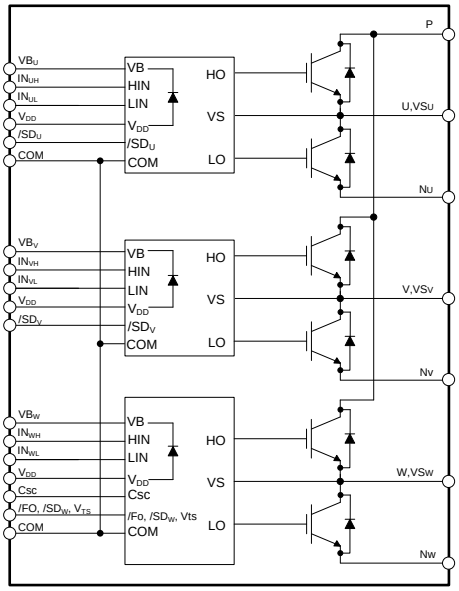


Figure 3. Internal Equivalent Circuit, Input / Output Pins

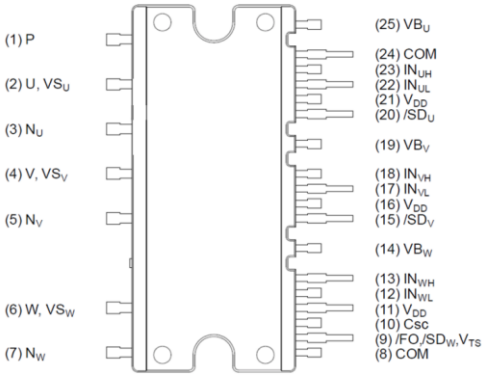


Figure 4. Package Top-View and Pin Assignment (FNB8xx60Tx)

2 Product Synopsis

This section discusses pin descriptions, electrical specifications, characteristics, and packaging.

Table 2. Pin Description

Pin Number	Name	Description
1	P	Positive DC Link Input
2	U,VS_U	Output for U Phase
3	N_U	Negative DC Link Input for U Phase
4	V,VS_V	Output for V Phase
5	N_V	Negative DC Link Input for V Phase
6	W,VS_W	Output for W Phase
7	N_W	Negative DC Link Input for W Phase
8	COM	Common Supply Ground
9	/FO, $/SD_W$, V_{TS}	Fault Output, Shut Down Input for W Phase, Temperature Output of Drive IC
10	C_{SC}	Shut Down Input for Over-Current & Short-Circuit Protection
11	V_{DD}	Common Bias Voltage for IC and IGBTs Driving
12	IN_{WL}	Signal Input for Low-Side W Phase
13	IN_{WH}	Signal Input for High-Side W Phase
14	VB_W	High-Side Bias Voltage for W Phase IGBT Driving
15	$/SD_V$	Shut Down Input for V Phase
16	V_{DD}	Common Bias Voltage for IC and IGBTs Driving
17	IN_{VL}	Signal Input for Low-Side V Phase
18	IN_{VH}	Signal Input for High-Side V Phase
19	VB_V	High-Side Bias Voltage for V Phase IGBT Driving
20	$/SD_U$	Shut Down Input for U Phase
21	V_{DD}	Common Bias Voltage for IC and IGBTs Driving
22	IN_{UL}	Signal Input for Low-Side U Phase
23	IN_{UH}	Signal Input for High-Side U Phase
24	COM	Common Supply Ground
25	VB_U	High-Side Bias Voltage for U Phase IGBT Driving

2.1 Detailed Pin Definition & Notification

- High-side bias voltage pins for driving the IGBT / high-side bias voltage ground pins for driving the IGBTs:
  - ▶ Pins: VB_U-U,VS_U, VB_V-V,VS_V, VB_W-W,VS_W
  - These are drive power supply pins for providing gate drive power to the high-side IGBTs. The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side IGBTs. Each bootstrap capacitor is charged from the V_{DD} supply during ON state of the corresponding low-side IGBT and low-side diode. To prevent malfunctions caused by noise and ripple in the supply voltage, a low-ESR, low-ESL filter capacitor should be mounted very close to these pins.
- Bias voltage pins for gate drive IC:
  - ▶ Pins: V_{DD}
  - This is a control supply pin for the built-in gate drive IC. To prevent malfunctions caused by noise and ripple in the supply voltage, a low-ESR, low-ESL filter capacitor should be mounted very close to this pin.
- Low-side common supply ground pin:
  - ▶ Pins: COM
  - This is a supply ground pin for the built-in gate drive IC. Important! To avoid noise influences, the main power circuit current should not be allowed to flow through this pin.
- Signal input pins:
  - ▶ Pins: IN_{UH}, IN_{UL}, IN_{VH}, IN_{VL}, IN_{WH}, IN_{WL}
  - These pins control the operation of the built-in IGBTs. They are activated by voltage input signals. The terminals are internally connected to a Schmitt-trigger circuit composed of 3.3 / 5 V-class CMOS. The signal logic of these pins is active high. The IGBT associated with each of these pins is turned ON when a sufficient logic voltage is applied to these pins. The wiring of each input should be as short as possible to protect the Motion SPM® 8 series against noise influences. To prevent signal oscillations, an RC coupling as illustrated in Figure 25 is recommended.
- Over-current and short-circuit detection input pin:
  - ▶ Pins: C_{SC}
  - The current detecting resistor should be connected between the C_{SC} and COM pins to detect over-current and short-circuit current *(refer to Figure 17)*. The shunt resistor should be selected to meet the detection levels matched for the specific application. An RC filter should be connected to the C_{SC} pin to eliminate noise. The connection length between the shunt resistor and C_{SC} pin should be minimized.
- Fault output / Shut down input for W phase / Temperature output:
  - ▶ Pin: /FO, /SD_W, V_{TS}
  - This is a multi function pin of fault output, shut down input and temperature output of W Phase drive IC. Firstly, this is the fault output alarm pin. An active LOW output is given on this pin for a fault state condition in the motion SPM 8 series. The alarm conditions are: Short-Circuit Current Protection (SCP), and low-side bias Under-Voltage Lockout (UVLO). The output from /FO, SD_W, V_{TS} pin is open drain configured. The signal line of /FO, SD_W, V_{TS} pin should be pulled to the 5 V logic power supply with approximately 10 kΩ resistance.

    Secondly, this is the shut down input pin for W phase. An active LOW input can be given on this pin for shutdown of Motion SPM 8 series by external control.

    Thirdly, this pin provides the temperature output of drive IC. Output voltage is determined by pull up voltage, pull up resistance and the temperature of drive IC. Thus, this pin can be used as a replacement of the thermistor.
- Shut down input for U and V phase:
  - ▶ Pin: /SD_U, /SD_V
  - These are shut down input pins for U and V phase. An active LOW input can be given on this pin for shutdown of Motion SPM 8 series by external control. These pins should be connected to Pin 9 (/FO, /SDW, VTS) as short as possible for stable operation and all phase shut down under the fault situation.
- Positive DC-link pin:
  - ▶ Pin: P
  - This is the DC-link positive power supply pin of the inverter. It is internally connected to the collectors of the high-side IGBTs. To suppress surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (tip: a metal film capacitor is typically used).
- Negative DC-link pins:
  - ▶ Pins: N_U, N_V, N_W
  - These are the DC-link negative power supply pins (power ground) of the inverter. These pins are connected to the low-side IGBT emitters of the each phase.
- Inverter power output pins:
  - ▶ Pins: U,VS_U ,V,VS_V ,W,VS_W
  - Inverter output pins for connecting to the inverter load (e.g. motor).

2.2 Absolute Maximum Ratings

T_J = 25°C, unless otherwise specified.

Table 3. Inverter

Symbol	Parameter	Conditions		Rating	Unit
V_{PN}	Supply Voltage	Applied between P - N_U, N_V, N_W		450	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P - N_U, N_V, N_W		500	V
V_{CES}	Collector - Emitter Voltage			600	V
±I_C	Each IGBT Collector Current	T_C=25°C, T_J≤150°C	FNB80460Tx	4	A
			FNB80560Tx	5	
			FNB81060Tx	10	
±I_{CP}	Each IGBT Collector Current (Peak)	T_C=25°C, T_J≤150°C, Under 1 ms Pulse Width	FNB80460Tx	6	A
			FNB80560Tx	10	
			FNB81060Tx	20	
T_J	Operating Junction Temperature(3)			-40~150	°C

Note:

3. The maximum junction temperature rating of the power chips integrated within the Motion SPM® 8 series is 150°C.

Table 4. Control Part

Symbol	Parameter	Conditions	Rating	Unit
V_{DD}	Control Supply Voltage	Applied between V_{DD} - COM	20	V
V_{BS}	High-Side Control Bias Voltage	Applied between VB_x - VS_x	20	V
V_{IN}	Input Signal Voltage	Applied between IN_{xH}, IN_{xL} - COM	-0.3~V_{DD}+0.3	V
V_{FS}	Fault Supply Voltage	Applied between /FO, /SD_W, V_{TS} - COM	-0.3~V_{DD}+0.3	V
I_{FO}	Fault Current	Sink Current at /FO, /SD_W, V_{TS} Pin	2	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC} - COM	-0.3~V_{DD}+0.3	V

Table 5. Total System

Symbol	Parameter	Conditions	Rating	Unit
$V_{PN(PROT)}$	Self Protection Supply Voltage Limit (Short-Circuit Protection Capability)	V_{DD}, V_{BS}=13.5~16.5 V, T_J=150°C, Non-Repetitive, < 2 µs	400	V
T_{STG}	Storage Temperature		-40~125	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1-Minute,	1500	V_{rms}

Table 6. Thermal Resistance

Symbol	Parameter	Conditions		Rating	Unit
$R_{th(j-c)Q}$	Junction-to-Case Thermal Resistance	Inverter IGBT Part (per Module)	FNB80460Tx	3.65	°C/W
			FNB80560Tx	3.60	
			FNB81060Tx	3.40	
$R_{th(j-c)F}$		Inverter FWDi Part (per Module)	FNB80360Tx	4.13	
			FNB80560Tx	4.03	
			FNB81060Tx	3.86	

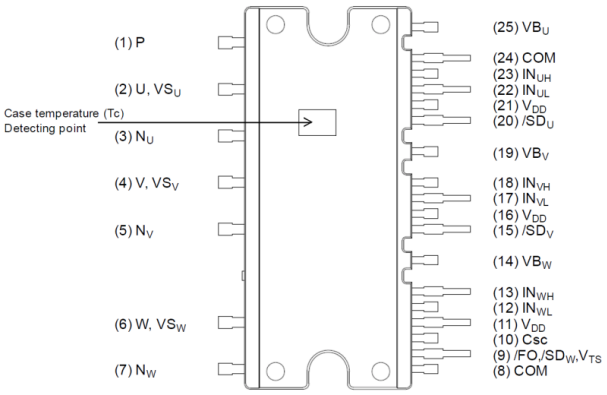


Figure 5. Case Temperature (T_C) Detecting Point (FNx8xx60Tx)

Table 7. Recommended Operating Conditions (Based on FNB81060Tx)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply Voltage	Applied between P - N_U, N_V, N_W		300	400	V
V_{DD}	Control Supply Voltage	Applied between V_{DD} - COM	14.0	15.0	16.5	V
V_{BS}	High-Side Bias Voltage	Applied between $V_{B(x)}$ – x, $V_{S(x)}$	13.0	15.0	18.5	V
dV_{DD}/dt, dV_{BS}/dt	Control Supply Variation		-1		+1	V/μs
t_{dead}	Blanking Time for Preventing Arm-Short	For Each Input Signal	0.5			μs
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W - COM (Including Surge Voltage)	-4		4	V
$P_{WIN(ON)}$	Minimum Input Pulse Width[4]		0.7			μs
$P_{WIN(OFF)}$			0.7			

Note:
4. This product may not make response if the input pulse width is less than the recommended value.

2.3 Electrical Characteristics

T_J = 25°C, unless otherwise specified.

Table 8. Inverter Part (Based on FNB81060Tx)

Symbol		Parameter	Conditions		Min.	Typ.	Max.	Unit
$V_{CE(SAT)}$		Collector - Emitter Saturation Voltage	V_{DD}, V_{BS} = 15 V, V_{IN}=5 V, I_C = 8 A	T_J=25°C		1.50	2.10	V
				T_J=150°C		1.80		
V_F		FWD Forward Voltage	V_{IN} = 0 V, I_F = 8 A	T_J=25°C		1.90	2.50	
				T_J=150°C		1.8		
HS	t_{ON}	Switching Times	V_{PN} = 400 V, V_{DD} = 15 V, V_{BS} = 15 V, I_C = 10 A T_J = 25, V_{IN} = 0 V ↔5 V, Inductive Load[5]		0.25	0.75	1.25	μs
	$t_{C(ON)}$					0.15	0.40	
	t_{OFF}					0.50	1.0	
	$t_{C(OFF)}$					0.10	0.40	
	t_{rr}					0.1		
LS	t_{ON}	Switching Times	V_{PN} = 400 V, V_{DD} = 15 V, V_{BS} = 15 V, I_C = 10 A T_J = 25, V_{IN} = 0 V ↔5 V, Inductive Load[5]		0.25	0.75	1.25	
	$t_{C(ON)}$					0.15	0.45	
	t_{OFF}					0.50	1.0	
	$t_{C(OFF)}$					0.10	0.40	
	t_{rr}					0.1		
I_{CES}		Collector - Emitter Leakage Current	V_{CE} = V_{CES}				1	mA

Note:
5. t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching times of the IGBT itself under the given gate driving condition internally. *For the detailed information, see Figure 6 and Figure 7*.

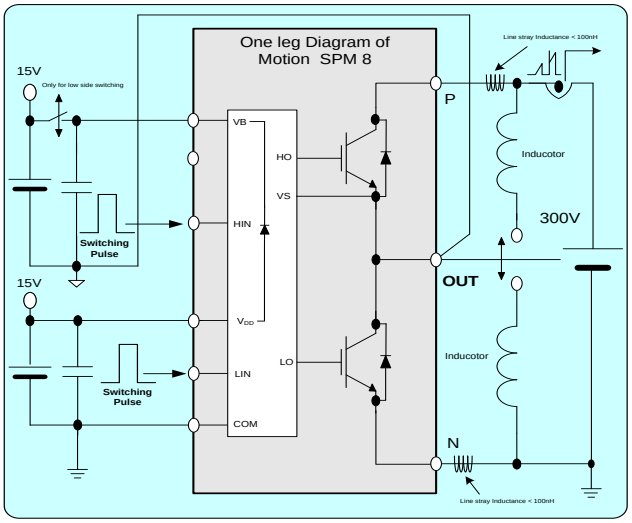


Figure 6. Switching Evaluation Circuit

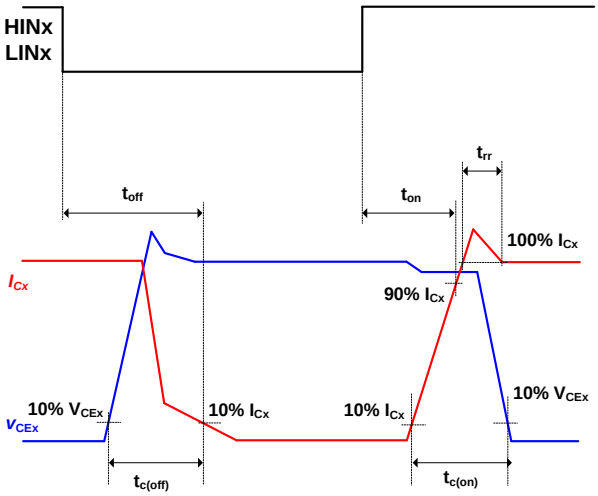


Figure 7. Switching Time Definition

Table 9. Control Part (Based on FNB81060Tx)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{QDD}	Quiescent V_{DD} Supply Current	V_{DD} = 15 V, IN_{xH}, IN_{xL} = 0 V	V_{DD} - COM			1.7	mA
I_{PDD}	Operating V_{DD} Supply Current	V_{DD} = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for High Side	V_{DD} - COM			2.2	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS} = 15 V, IN_{xH} = 0 V	Applied between VB_X –x,VS_x			100	µA
I_{PBS}	Operating V_{BS} Supply Current	V_{DD}, V_{BS} = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for High Side	Applied between VB_X –x,VS_x			600	µA
V_{FOH}	Fault Output Voltage	V_{DD} = 15 V, V_{SC} = 0 V, /FO Circuit: 10 kΩ to 5 V Pull-up		4.5			V
V_{FOL}		V_{DD} = 15 V, V_{SC} = 1 V, /FO Circuit: 10 kΩ to 5 V Pull-up				0.5	
$V_{SC(ref)}$	Short-Circuit Trip Level	V_{DD} = 15 V[6]	C_{SC} - COM	0.46	0.49	0.52	V
UV_{DDD}	Supply Circuit, Under-Voltage Protection	Detection Level		10.0	11.5	13.0	V
UV_{DDR}		Reset Level		10.5	12.0	13.5	
UV_{BSD}		Detection Level		9.5	11.0	12.5	
UV_{BSR}		Reset Level		10.0	11.5	13.0	
I_{FO_T}	HVIC Temperature Sensing Current	V_{DD} = 15 V, V_{BS} = 15 V, T_{HVIC} = 25°C			82.5		µA
V_{FO_T}	HVIC Temperature Sensing Voltage	V_{DD} = 15 V, V_{BS} = 15 V, T_{HVIC} = 25°C, 10 kΩ to 5 V Pull-up			4.18		V
t_{FOD}	Fault-Out Pulse Width			40			µs
V_{FSDR}	Shut Down Reset Level	Applied between /FO - COM				2.4	V
V_{FSDD}	Shut Down Detection Level			0.8			
$V_{IN(ON)}$	ON Threshold Voltage	Applied between IN_{xH}, IN_{xL} - COM				2.4	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.8			

Note:

6. Short-circuit current protection function is for all six IGBTs if the /FO, $/SD_W$, V_{TS} pin is connected to $/SD_x$ pins.

3 Package

Since heat dissipation is an important factor in limiting the power module's current capability, the heat dissipation characteristics of a package are important in determining the performance. A trade-off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to good package technology lies in the optimization of package size while maintaining outstanding heat dissipation. In Motion SPM® 8 series, technology was developed with full pack substrate while keeping the thickness small between lead frame and module case. Power chips are attached directly to the lead frame. Figure 8 shows the cross sections and isolation distances of the Motion SPM 8 series.

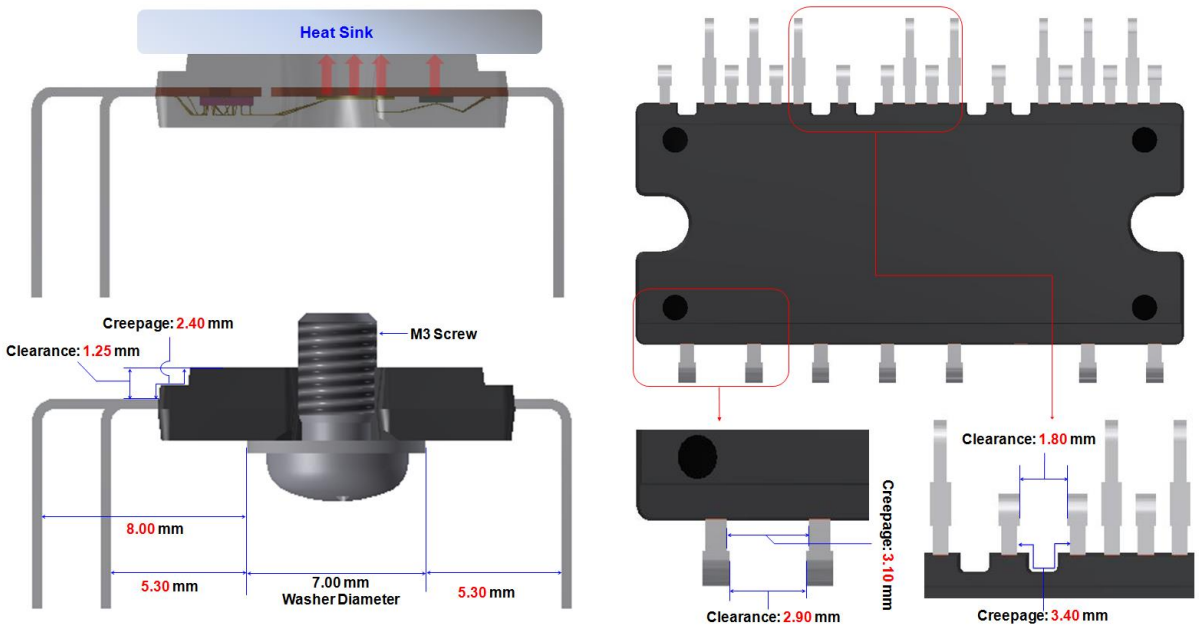


Figure 8. Vertical Structure for Heat Dissipation and Distance for Isolation from Pin to Pin and from Pins to Heat Sink and Washer

Table 10. Mechanical Characteristics and Ratings

Parameter	Conditions		Value			Unit
			Min.	Typ.	Max.	
Device Flatness	*See Figure 9*		-50		100	µm
Mounting Torque	Mounting Screw: M3	Recommended 0.7 N·m	0.6	0.7	0.8	N·m
		Recommended 7.1 kg·cm	5.9	6.9	7.9	kg·cm
Weight				5.0		g

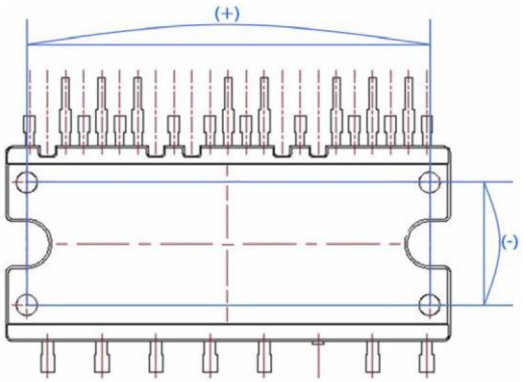


Figure 9. Flatness Measurement Position

3.1 Detailed Package Outline Drawings

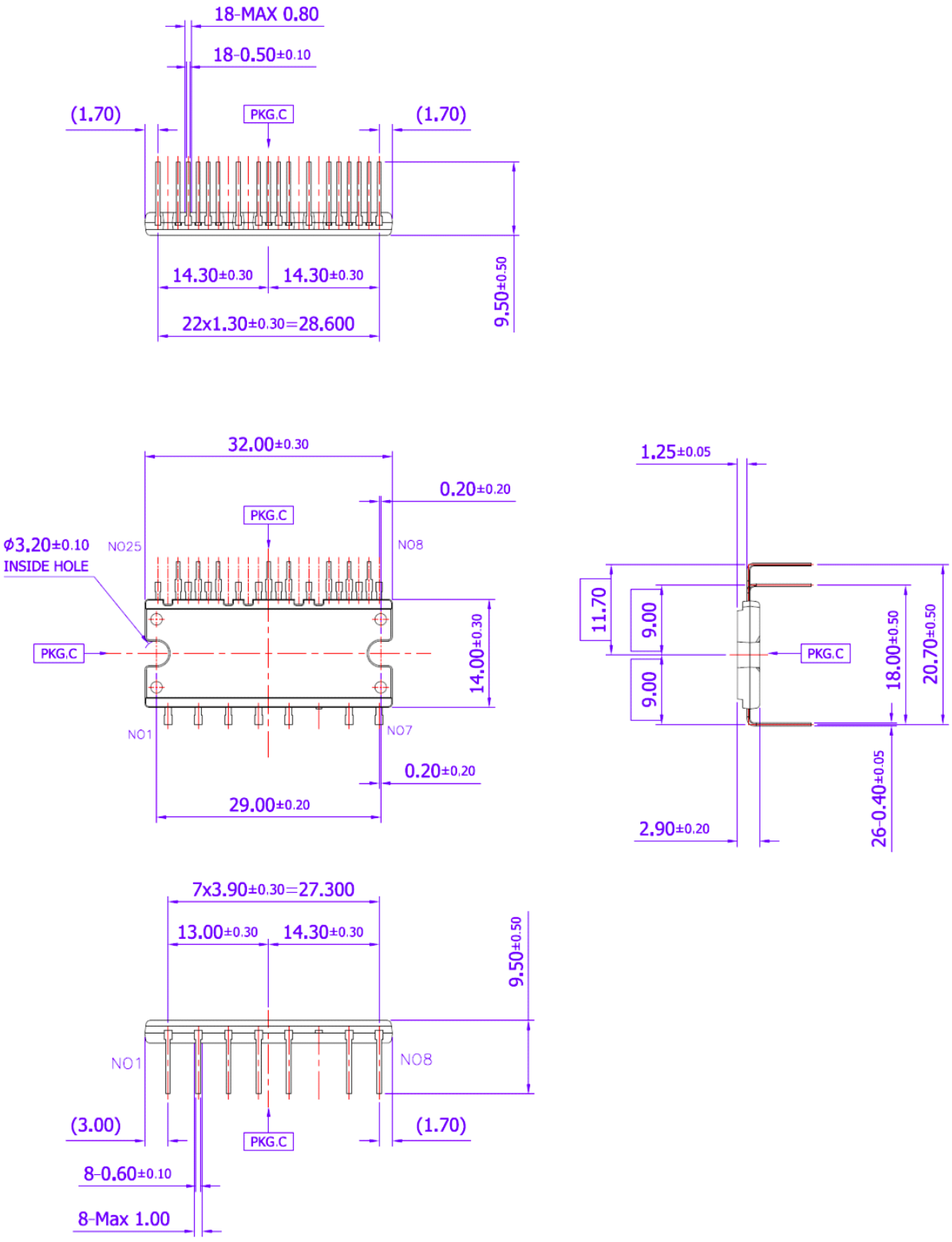
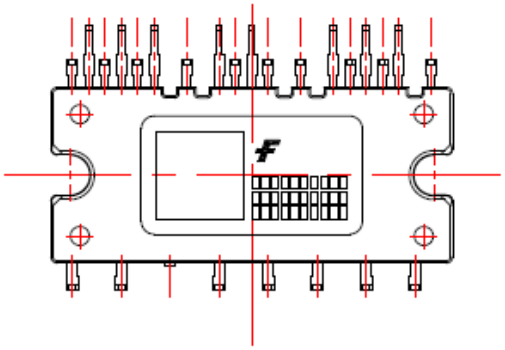


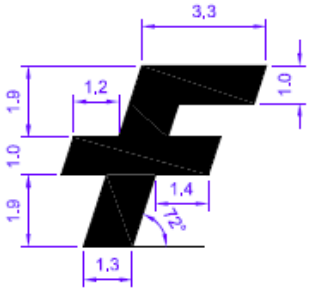
Figure 10. FNB8xx60T3, Long Lead

3.2 Marking Information

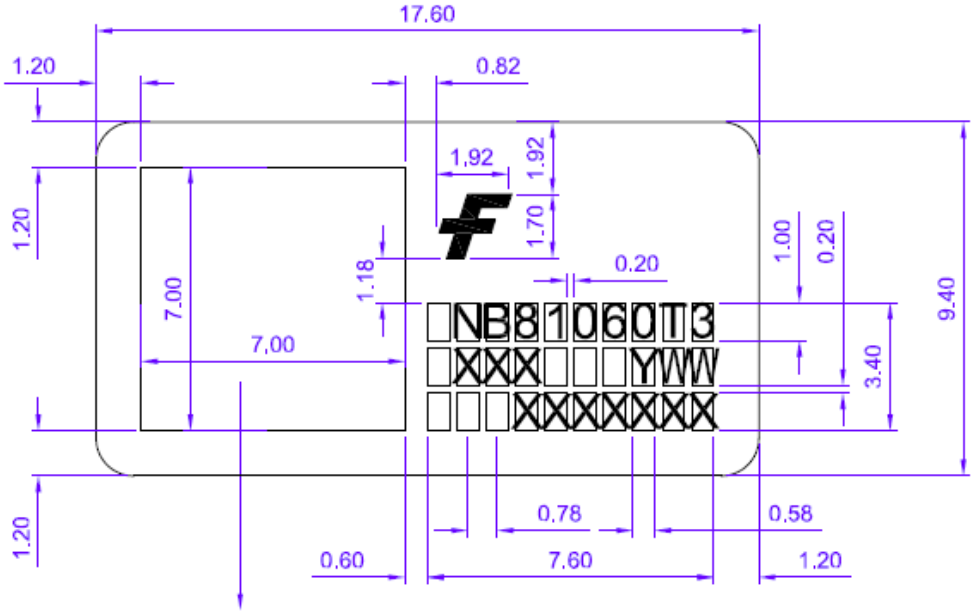
* MARKING LAY-OUT



FAIRCHILD SEMICONDUCTOR LOGO
DIMENSIONAL PROPORTION



* MARKING DIMENSION



Data Matrix Code. 2D data:
NB81060T3 XXX YWW A 0000001

Part number
Lot No.
7 digit serial number
Machine ID(One character A~Z)
Date code

Y	Alphabet
2010	A
2011	B
2012	C
2013	D
2014	E
2015	F
2016	G
2017	H
2018	J
2019	K
2020	A

* NOTE

1. F : FAIRCHILD LOGO
2. XXX : LAST 3 DIGITS OF LOT NO(OPTION CODE)
3. YWW : WORK WEEK CODE ("Y" REFERS TO THE RIGHT ALPHABET CHARACTER TABLE)
4. XXXXXXX : SERIAL NUMBER

Figure 11. Marking Information

4 Operating Sequence for Protections

4.1 Inter-lock Function

Motion SPM® 8 series provides an inter-lock function with fixed dead time to prevent leg short-circuit by the wrong input signal from the controller. Operating timing diagram is shown in Figure 12.

Driver output correspond to the advanced input signal, a later input signal of the same phase is ignored during overlapped time and then the output signal is delayed by integrated fixed dead time as shown in Figure 12.

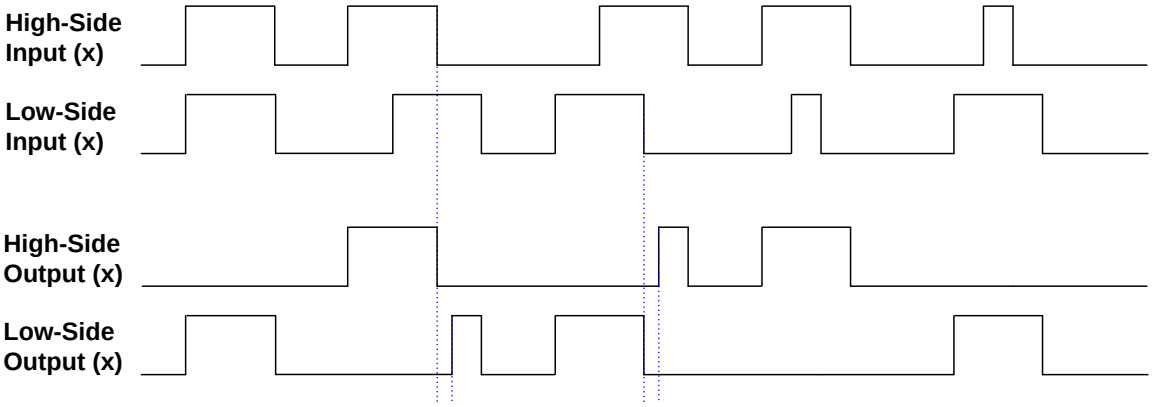


Figure 12. Integrated Gate Drive IC Input / Output Timing Diagram by Inter Lock Function

4.2 Over-Current & Short-Circuit Protection (OCP/SCP)

Motion SPM 8 series use an external shunt resistor (R_{SC}) for the over-current detection as shown in Figure 13. Drive IC has a built-in over-current protection function. This protection function senses the voltage to the C_{SC} pin. If this voltage exceeds the $V_{SC(ref)}$ (the threshold voltage trip level of protection function) specified in the device datasheets($V_{SC(ref)}$, typ. is 0.5 V), a fault signal is activated to low and the all six IGBTs are turned off. Typically the maximum short-circuit current magnitude is gate-voltage dependent: higher gate voltage (V_{DD} & V_{BS}) results in larger short-circuit current. To avoid potential problems, the maximum short-circuit trip level is set below 2 times the nominal rated collector current. The drive IC short-circuit current protection-timing chart is shown in Figure 14.

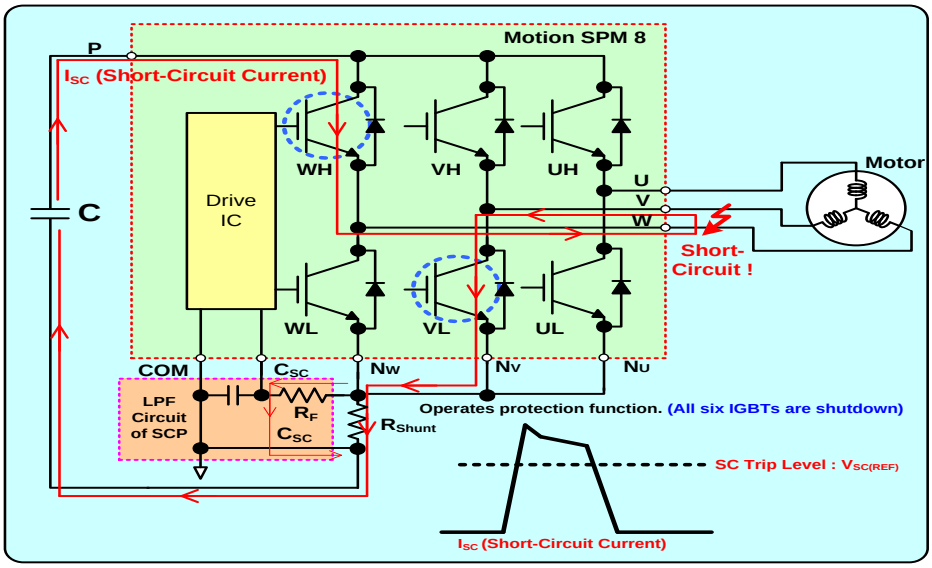


Figure 13. Operation of Short-Circuit Current Protection

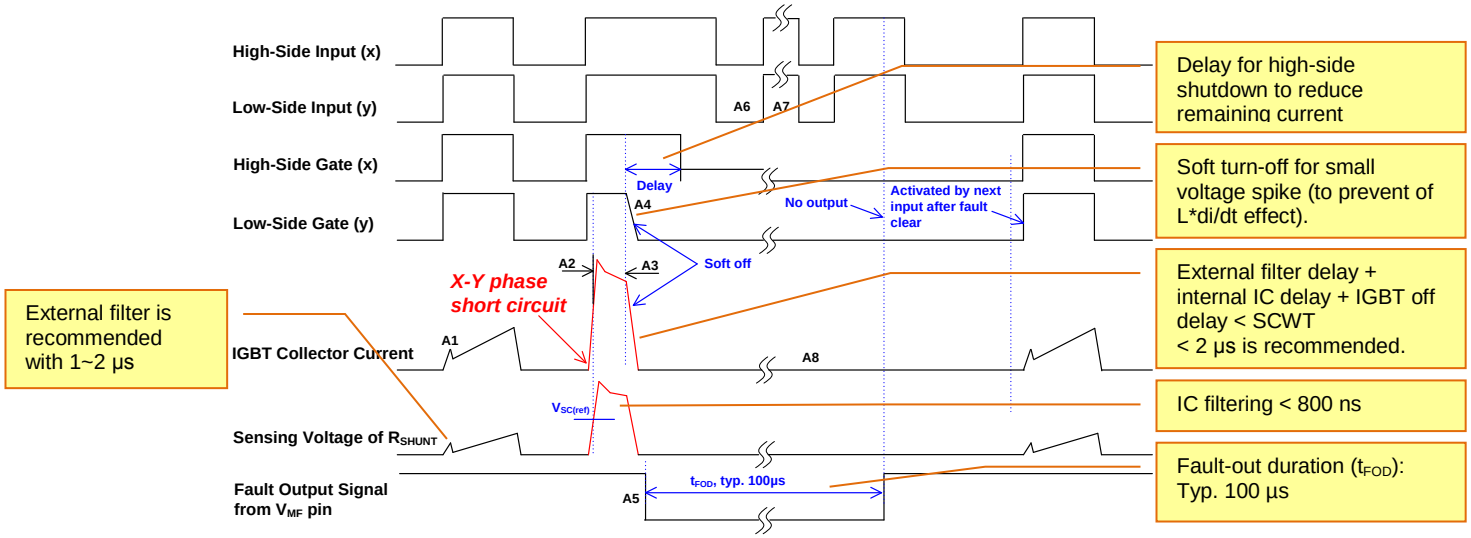


Figure 14. Timing Chart of Short-Circuit Current Protection Function

Notes:

7. A1-normal operation: IGBT on and carrying current.
8. A2-short circuit current detection (SC trigger).
9. A3-hard IGBT gate interrupt.
10. A4-IGBT turns OFF by soft-off function.
11. A5-fault output timer operation start with internal delay (Typ. 2.0 µs), tFOD=Typ. 100 µs.
12. A6-input “L”: IGBT OFF state.
13. A7-input “H”: IGBT ON state, but during the active period of fault output the IGBT doesn’t turn ON.
14. A8-IGBT keeps OFF state.

4.3 Under-Voltage Lockout Protection

The gate drive IC has an Under-Voltage Lockout protection (UVLO) function to protect the IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 15. The gate drive IC has an under-voltage lockout function to protect the high-side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 16. A fault-out alarm from /FO pin is not given for low at high-side bias conditions.

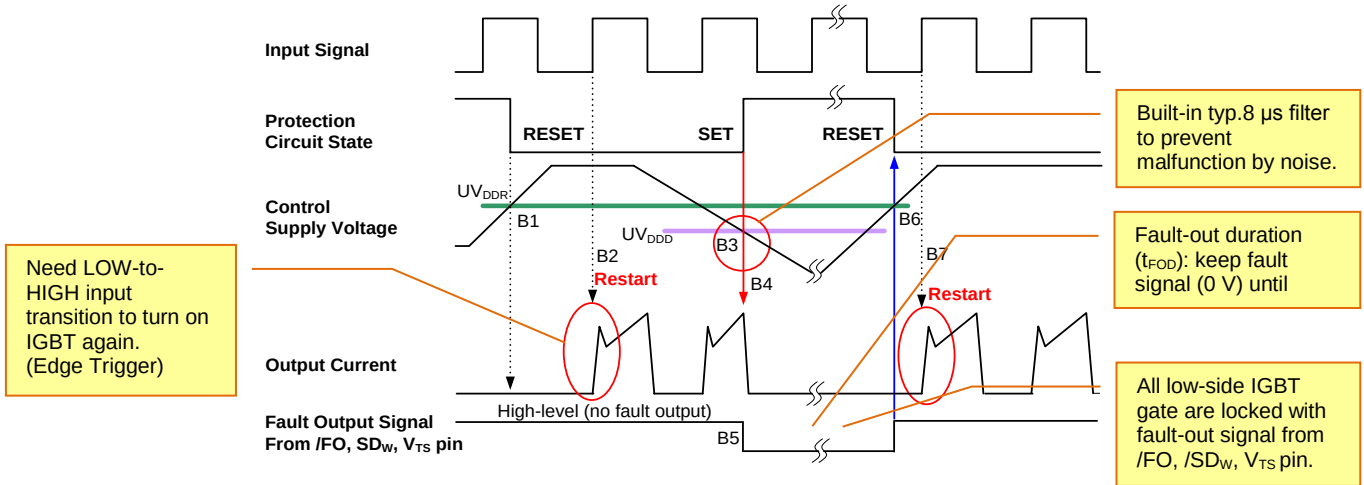


Figure 15. Timing Chart of Low-Side Under-Voltage Protection Function

Notes:

15. B1-control supply voltage rise: after the voltage rises UV_{DDR}, the circuits starts to operate when the next input is applied.
16. B2-normal operation: IGBT ON and carrying current.
17. B3-under-voltage detection (UV_{DDD}).
18. B4-IGBT OFF in spite of control input is alive.
19. B5-fault output signal from /FO, /SD_W, VTS pin starts.
20. B6-under-voltage reset (UV_{DDR}).
21. B7-normal operation: IGBT ON and carrying current.

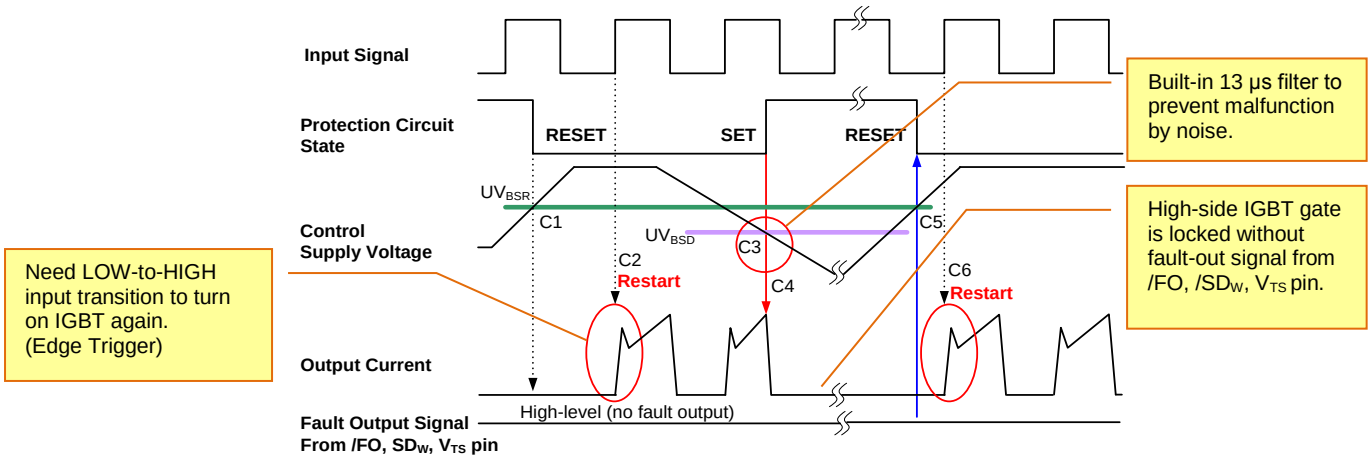


Figure 16. Timing Chart of High-Side Under-Voltage Protection Function

Notes:

22. C1-control supply voltage rises: after the voltage reaches UV_{BSR}, the circuit starts when the next input is applied.
23. C2-normal operation: IGBT ON and carrying current.
24. C3-under-voltage detection (UV_{BSD}).
25. C4-IGBT OFF in spite of control input is alive, but there is no fault output signal from /FO, $/SD_W$, VTS pin.
26. C5-under-voltage reset (UV_{BSR}).
27. C6-normal operation: IGBT ON and carrying current.

5 Key Parameter Design Guidance

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of Motion SPM® 8 series.

5.1 Shunt Resistor Selection at N-Terminal for Current Sensing & Protection

The external RC time constant from the N-terminal shunt resistor to CSC must be lower than 2 µs when overload condition is detected for a stable shutdown.

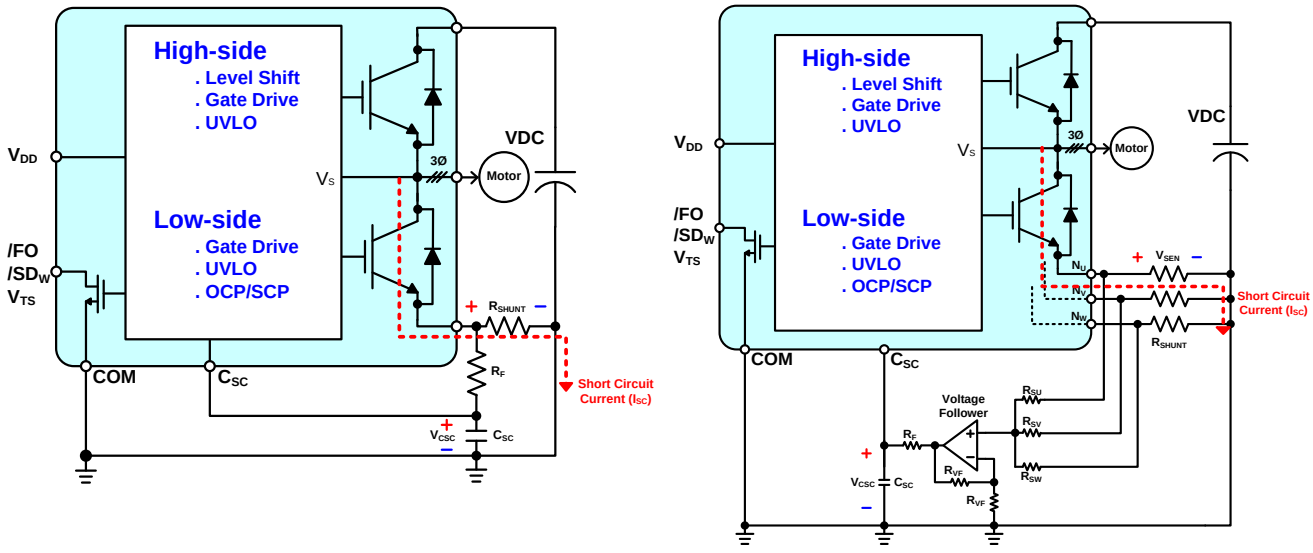


Figure 17. Recommended Circuitry for Over-Current & Short-Circuit Protection

Table 11. OCP & SCP Level ($V_{SC(ref)}$) Specification

Conditions	Min.	Typ.	Max.	Unit
Specification at T_J=25°C, V_{DD}=15 V	0.46	0.49	0.52	V

Table 12. Operating Over Current Range (R_{SHUNT}=37 mΩ (Min.), 39 mΩ (Typ.), 41 mΩ (Max.)) *(see the equations below)*

Conditions	Min.	Typ.	Max.	Unit
Operating OC Level at T_J=25°C	11	13	15	A

In case of one shunt, the value of shunt resistor is calculated by the following equations.

Maximum current trip level (depends on user selection):

$$I_{OC(max)} = 1.5 \times I_{C(max)}$$

Over-current trip reference voltage (depends on datasheet):

$$V_{SC(ref)} = min.\ 0.46\ V,\ typ.\ 0.49\ V,\ max.\ 0.52\ V$$

Shunt resistance:

$$I_{OC(max)} = V_{SC(max)} / R_{SHUNT(min)} \rightarrow R_{SHUNT(min)} = V_{SC(max)} / I_{SC(max)}$$

If the deviation of the shunt resistor is limited below ± 5%:

$$R_{SHUNT(typ)} = R_{SHUNT(min)} / 0.95,$$

$$R_{SHUNT(max)} = R_{SHUNT(typ)} \times 1.05$$

Actual over-current trip current level becomes:

$$I_{OC(typ)} = V_{SC(typ)} / R_{SHUNT(typ)},\ I_{OC(min)} = V_{SC(min)} / R_{SHUNT(max)}$$

Inverter output power:

$$P_{OUT} = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times V_{DC\_Link} \times I_{RMS} \times PF$$

where:

MI = Modulation Index;

V_{DC_Link} *= DC link voltage;*

I_{RMS} *= Maximum load current of inverter; and*

PF = Power Factor

Average DC current:

$$I_{DC\_AVG} = V_{DC\_Link} / (P_{out} \times Eff)$$

where:

Eff = Inverter efficiency

The power rating of shunt resistor is calculated by the following equation:

$$P_{SHUNT} = (I^2_{DC\_AVG} \times R_{SHUNT} \times Margin) / Derating\ Ratio$$

where:

R_{SHUNT}*=Shunt resistor typical value at* T_C*=25*°C

Derating Ratio=Derating ratio of shunt resistor at T_{SHUNT}*=100*°C

(From datasheet of shunt resistor); and

Margin = Safety margin (determined by user)

✓ **Shunt Resistor Calculation Examples**

➢ Calculation Conditions:

- DUT: FNB81060Tx
- Tolerance of shunt resistor: ±5%
- Over-current trip reference voltage:

  $V_{SC(min)}$=0.46 V, $V_{SC(typ)}$=0.49 V, $V_{SC(max)}$=0.52 V
- Maximum load current of inverter (I_{RMS}): 5 A_{rms}
- Maximum peak load current of inverter ($I_{C(max)}$): 10 A
- Modulation Index (MI): 0.9
- DC Link Voltage (V_{DC_Link}): 300 V
- Power Factor (PF): 0.8
- Inverter Efficiency (Eff): 0.95
- Shunt resistor value at T_C = 25°C (R_{SHUNT}): 39 mΩ
- Derating ration of shunt resistor at T_{SHUNT} = 100°C: 70%
- Safety margin: 20%

➢ Calculation results:

- $I_{OC(max)}$: 1.5 × $I_{C(max)}$ = 1.5 x 10 A = 15 A
- $R_{SHUNT(min)}$: $V_{SC(max)}$ / $I_{SC(max)}$=0.52 V / 15 A=35 mΩ
- $R_{SHUNT(typ)}$: $R_{SHUNT(min)}$ / 0.95 = 35 mΩ / 0.95 = 37 mΩ
- $R_{SHUNT(max)}$: $R_{SHUNT(typ)}$ x 1.05 = 37 mΩ x 1.05 = 39 mΩ
- $I_{OC(min)}$: $V_{SC(min)}$ / $R_{SHUNT(max)}$ = 0.46 V / 39 mΩ = 11.7 A
- $I_{OC(typ)}$: $V_{SC(typ)}$ / $R_{SHUNT(typ)}$ = 0.49 V / 37 mΩ = 13.2 A
- $P_{OUT} = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times V_{DC\_Link} \times I_{RMS} \times PF = \frac{\sqrt{3}}{\sqrt{2}} \times 0.9 \times 300 \times 5 \times 0.8$ = 1323 W
- I_{DC_AVG} = (P_{OUT}/Eff) / V_{DC_Link} = 4.64 A
- P_{SHUNT} = ($I^2_{DC\_AVG}$ × R_{SHUNT} × Margin) / Derating Ratio = (4.64^2 × 0.041 × 1.2) / 0.7 = 1.44 W (Therefore, the proper power rating of shunt resistor is over 1.5 W)

5.2 Time Constant of Internal Delay

An RC filter prevents unexpected malfunction by noise-related signal like reverse recovery current of FWDi. The RC time constant is determined by the applied noise time and the Short-Circuit Current Withstanding Time (SCWT) of Motion SPM® 8 series. When the R_{SHUNT} voltage exceeds the OCP level, this is applied to the C_{SC} pin via the RC filter. The RC filter delay (T1) is the time required for the C_{SC} pin voltage to rise to the referenced OCP level. The gate drive IC has an internal filter time (logic filter time for noise elimination: T2). Consider this filter time when designing the RC filter of V_{CSC}.

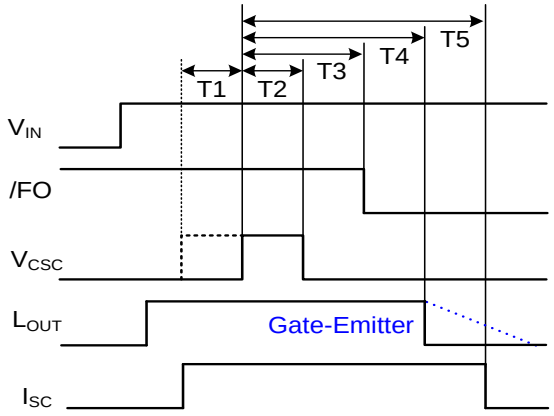


Figure 18. Timing Diagram

Notes:

28. V_{IN}: Voltage of input signal.
29. L_{OUT}: V_{GE} of low-side IGBT.
30. V_{CSC}: Voltage of C_{SC} pin.
31. I_{SC}: Short-circuit current.
32. /FO: Voltage of /FO, $/SD_W$, V_{TS} pin.
33. T1: filtering time of RC filter of V_{CSC}.
34. T2: filtering time of C_{SC}. If V_{CSC} width is less than T2, SCP does not operate.
35. T3: delay from C_{SC} triggering to gate-voltage down.
36. T4: delay from C_{SC} triggering to fault-out signal.
37. T5: delay from C_{SC} triggering to short-circuit current.

Table 13. Time Table on Short-Circuit Conditions: V_{CSC} to L_{OUT}, I_{SC}, /FO

Device Under Test	Typ. at T_J=25°C	Max. at T_J=25°C
FNB81060Tx	T2 = 0.8 μs	Considering ±20% Dispersion, T4=1.6 μs
	T3 = 0.9 μs	
	T4 = 1.45 μs	
	T5 = 1.6 μs	

Notes:

38. To guarantee safe short-circuit protection under all operating conditions, C_{SC} should be triggered within 0.8 μs after short-circuit occurs. (Recommendation: SCWT < 2.0 μs, Conditions: V_{DC}=400 V, V_{DD}=16.5 V, T_J=150°C).
39. It is recommended that delay from short-circuit to C_{SC} triggering should be minimized.

5.3 Soft Turn-Off

A soft turn-off function protects the low-side IGBTs from over-voltage of V_{PN} (supply voltage) by "hard off at over-current or short-circuit mode," which is when IGBTs are turned off by an input signal before the SCP function under short-circuit condition. In this case, V_{PN} rapidly rises by fast and large di/dt of I_C (over-current or short-circuit current). This kind of rapid rise of V_{PN} can cause destruction of IGBT by over-voltage. Soft-off function prevents IGBT rapid turning off by slow discharging of V_{GE} (gate-to-emitter voltage of IGBT).

An internal block diagram of the low-side and operation sequence of the soft turn-off functions are shown in Figure 19 and Figure 20. This function operates by two internal protection functions (UVLO and OCP/SCP). When the IGBT is turned off in normal conditions, gate drive IC turns off the IGBT immediately by turn-off gate signal ($IN_{(XL)}$) via gate driver block. Pre-driver turn-on output buffer of gate driver block, path ①. When the IGBT is turned off by a protection function, the gate driver is disabled by the protection function signal via output of protection circuit (disable output buffer, high-Z) and output of the protection circuit turn-on switch of the soft-off function. V_{GE} (IGBT gate-emitter voltage) is discharged slowly via circuit of soft-off (path ②).

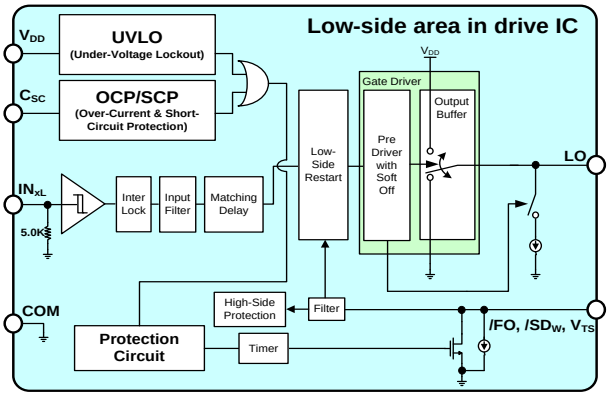


Figure 19. Internal Block Diagram of Gate Drive IC

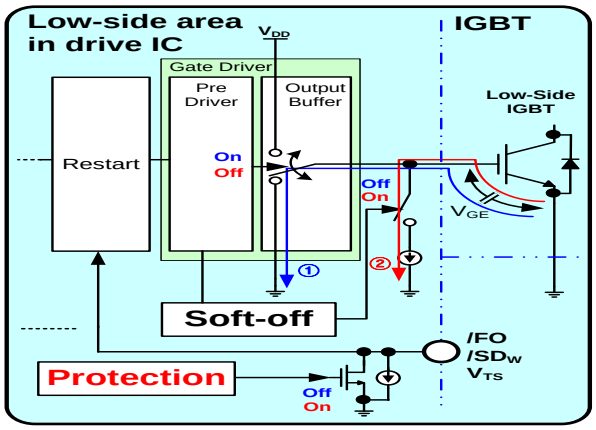


Figure 20. Operating Sequence of Soft Turn-Off

5.4 Multi-function Pin (/FO, /SDW, VTS)

Pin 9 (/FO, /SDW, VTS) terminal provides multi functions which are fault-out, shut down input and temperature monitoring. Firstly, this terminal provides temperature monitoring function for temperature of internal drive IC. As shown in Figure 21, this terminal can be connected to ADC and fault detection terminals of micro controller. This circuit is very simple, and IGBTs can be shut down by the micro controller. For example, when R1 is 10 kΩ, then voltage of this terminal is 1.76 V Typ. at V_{ctr} = 5 V if drive IC T_J is about 110°C as shown in Figure 22. User can control target voltage simply by change R1 value.

It is noted that /SDU and /SDV pins should be connected to /FO, /SDW, VTS pin as short as possible for stable operation and all phase shut down under the fault situation.

Table 14. Maximum Ratings of /FO, /SDW, VTS Part

Symbol	Item	Condition	Rating	Unit
VFS	Fault Supply Voltage	Applied between /FO, /SDW, VTS - COM	-0.3 ~ VDD+0.3	V
IFO	Fault Current	Sink Current at /FO, /SDW, VTS Pin	2	mA

Table 15. Electric Characteristics

Symbol	Item	Conditions	Min.	Max.	Unit
VFOH	Fault Voltage	VDD=15 V, VSC=0, /FO Circuit: 10 kΩ to 5 V Pull-Up	4.5		V
VFOL		VDD=15 V, VSC=1 V, /FO Circuit: 10 kΩ to 5 V Pull-Up		0.5	V
IFT	HVIC Temperature Sensing Current	VDD=15 V, THVIC=25°C	68	95	μA
VFT	HVIC Temperature Sensing Voltage	VDD=15 V, THVIC=25°C, 10 kΩ to 5 V Pull-Up	4.05	4.32	V
VFSDR	Shut Down Reset Level	Applied between /FO, SDW, VTS - COM		2.4	V
VFSDD	Shut Down Detection Level		0.8		V

Figure 23 and Figure 24 describe timing diagram of fault-out and shut down input functions. Temperature of drive IC in Motion SPM® 8 series is calculated by below equation.

$$T_{HVIC} = ((Vctr - /FO) - 20\mu A \times R1) / (R1 \times 2.76\mu A)$$

It is noted that above equation is based on 'current = zero' in fault input area of controller. If leakage current exists at fault input of the controller, '20 μA' in the above equation should be changed to '20 μA + leakage current'.

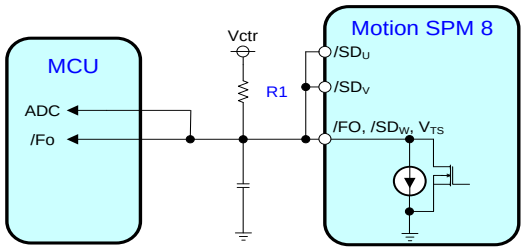


Figure 21. Proposed Circuit for Protection

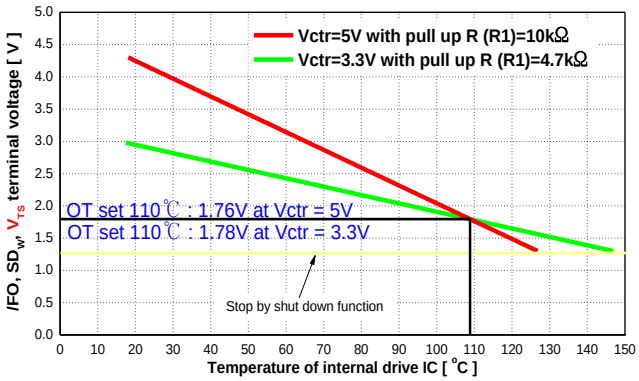


Figure 22. Voltage of /FO, SDW, VTS Terminal according to Internal Drive IC Temperature

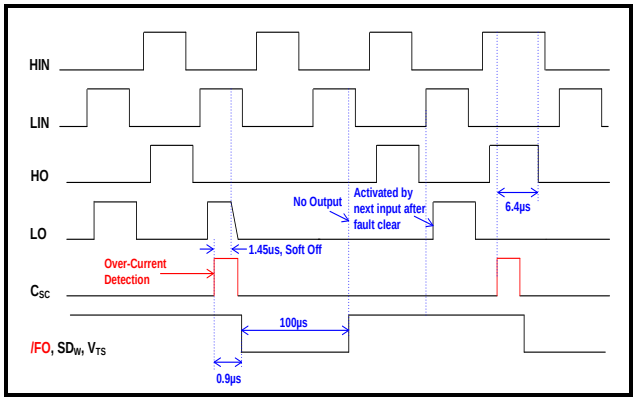


Figure 23. Fault-Out Function of /FO, SDW, VTS Terminal

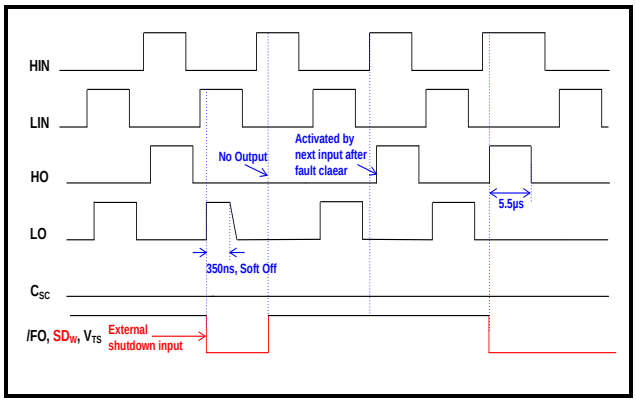


Figure 24. Shutdown Function of /FO, SDW, VTS Terminal

5.5 Circuit of Input Signal (IN_{xH}, IN_{xL})

Figure 25 shows the I/O interface circuit between the MCU and Motion SPM® 8 series. Because the Motion SPM 8 series input logic is active high and there are built-in pull-down resistors, external pull-down resistors are not needed.

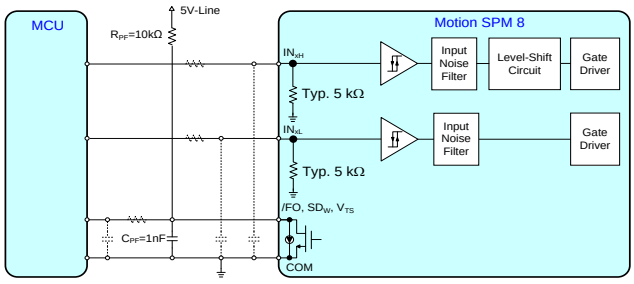


Figure 25. Recommended CPU I/O Interface Circuit

The input and fault output maximum rated voltages are shown in Table 16. Since the fault output is open drain, its rating is V_{DD} +0.3 V, 15 V supply interface is possible. However, it is recommended that the fault output be configured with the 5 V logic supplies, which is the same as the input signals. It is also recommended that the de-coupling capacitors be placed at both the MCU and Motion.

To avoid unexpected operation by fault signal, it is recommended to connect bypass capacitor to ends of the signal line for /FO, SD_W, V_{TS} pin and MCU as close as possible to each device. The RC coupling at each input (parts shown dotted in Figure 25) can be changed depending on the PWM control scheme used in the application and the wiring impedance of the PCB layout.

The input signal section of the Motion SPM 8 series integrates 5 kΩ (typical) pull-down resistors. Therefore, when using an external filtering resistor between the MCU output and the Motion SPM 8 series input, attention should be given to the signal voltage drop at the Motion SPM 8 series input terminals to satisfy the turn-on threshold voltage requirement. For instance, R=100 Ω and C=1 nF can be used for the parts shown dotted in Figure 25.

Table 16. Maximum Ratings of Input Pins

Symbol	Item	Condition	Rating	Unit
V_{IN}	Input Signal Voltage	Applied between IN_{xH}, IN_{xL}-COM	-0.3 ~ V_{DD} +0.3	V

Table 17. Input Threshold Voltage Ratings (V_{DD}=15 V, T_J=25°C)

Symbol	Item	Condition	Min.	Max.	Unit
$V_{IN(ON)}$	Turn-On Threshold Voltage	IN_{xH},IN_{xL} - COM		2.4	V
$V_{IN(OFF)}$	Turn-Off Threshold Voltage		0.8		V

5.6 Bootstrap Circuit Design

5.6.1 Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between VB (U, V, W) and VS (U, V, W), provides the supply to the HVIC within the Motion SPM 8 series. This supply must be in the range of 13.0 V~18.5 V to ensure that the HVIC can fully drive the high-side IGBT. The under-voltage lockout protection for V_{BS} ensures that the HVIC does not drive the high-side IGBT if the V_{BS} voltage drops below a specific voltage (*refer to the datasheet of Motion SPM 8 series*). This function prevents the IGBT from operating in a high-dissipation mode.

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here (refer to Figure 26). This method has the advantage of being simple and inexpensive. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. SPM 8 provides integrated bootstrap circuitry in driver. The bootstrap supply is formed by a combination of an integrated bootstrap diode and the current flow path of the bootstrap circuit is shown in Figure 26. When V_S is pulled down to ground (low-side IGBT turn-on or low-side FRD freewheeling), the bootstrap capacitor (C_{BS}) is charged through the integrated bootstrap diode from the V_{DD} supply.

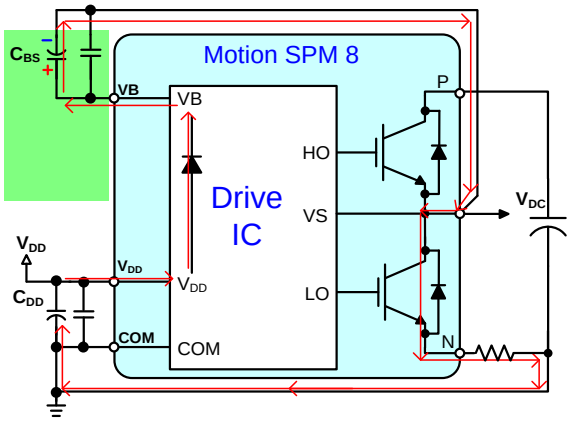


Figure 26. Current Path of Bootstrap Circuit for the Supply Voltage (V_{BS}) of a HVIC when Low-Side IGBT Turns On

5.6.2 Selection of Bootstrap Capacitor Considering Initial Charging

Figure 27 shows an example of initial bootstrap charging sequence. Once V_{DD} is established, V_{BS} needs to be charged by turning on the low-side IGBTs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency. Therefore, it is desired to maintain this structure without creating complementary high-side PWM signals.

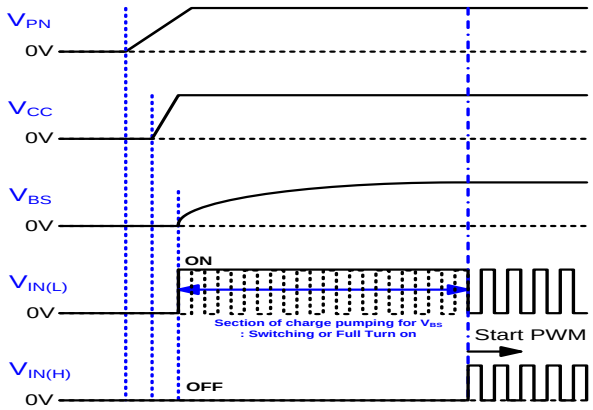


Figure 27. Timing Chart of Initial Bootstrap Charging

Adequate on-time of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated by:

$$t_{charge} = C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln \frac{V_{DD}}{V_{DD} - V_{BS(target)} - V_{F\_TH} - V_{CE\_TH}} \quad (1)$$

where:

C_{BS} = Capacitance of bootstrap capacitor

R_{BS} = Resistance of integrated bootstrap diode

V_{F_TH} = Threshold voltage of integrated bootstrap diode

$V_{BS(target)}$ =Target charged value of the V_{BS}

V_{CE_TH} = Collector-Emitter threshold voltage of the low-side IGBT

δ = Low side duty ratio of PWM.

Enough on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is initially required before normal operation of PWM starts for the Motion SPM® 8 series. I-V characteristics of integrated bootstrap diode is shown in Figure 28 and recommended C_{BS} initial charging time (t_{charge}) is shown in Figure 29.

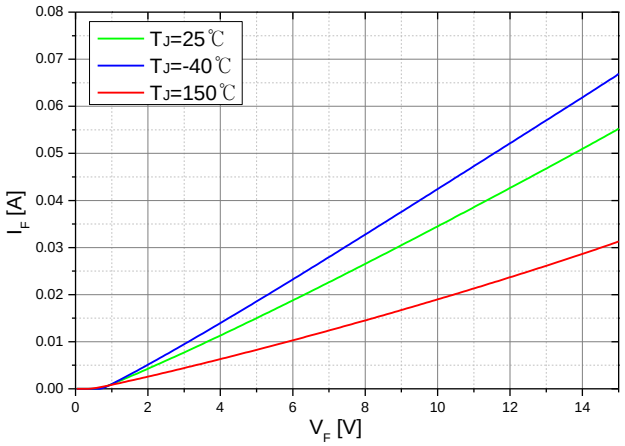


Figure 28. Built-In Bootstrap Diode I-V Characteristic

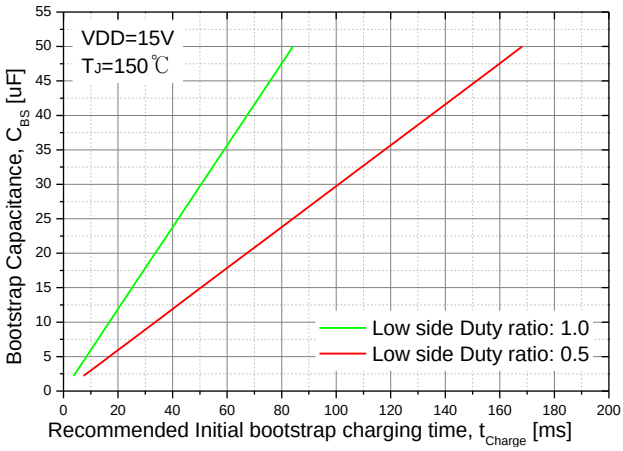


Figure 29. Recommended t_{charge} by C_{BS} and Duty Ratio

5.6.3 Selection of Bootstrap Capacitor Considering Operating

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{IBS_{TOT} \times \Delta t}{\Delta V_{BS}} \quad (2)$$

where:
Δt: maximum on pulse width of high-side IGBT;
ΔV_{BS}: the allowable discharge voltage of the C_{BS} (voltage ripple); and
IBS_{TOT}: maximum discharge current of the C_{BS}.

Mainly via the following mechanisms:

- Gate charge for turning the high-side IGBT on
- Quiescent current to the high-side circuit in HVIC
- Level-shift charge required by level-shifters in HVIC
- Leakage current in the bootstrap diode
- C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)
- Bootstrap diode reverse recovery charge

Practically, I_{PBS}*1.2 is recommended as IBS_{TOT} for the Motion SPM® 8 series. By considering dispersion and reliability, the capacitance is generally selected to be 2~3 times the calculated one. The C_{BS} is only charged when the high-side IGBT is off and the $VS_{(U,V,W)}$ voltage is pulled down to ground.

The on-time of the low-side IGBT must be sufficient for the charge drawn from the C_{BS} capacitor to be fully replenished. This creates an inherent minimum on-time of the low-side IGBT (or off-time of the high-side IGBT).

Calculation Examples of Bootstrap Capacitance A;

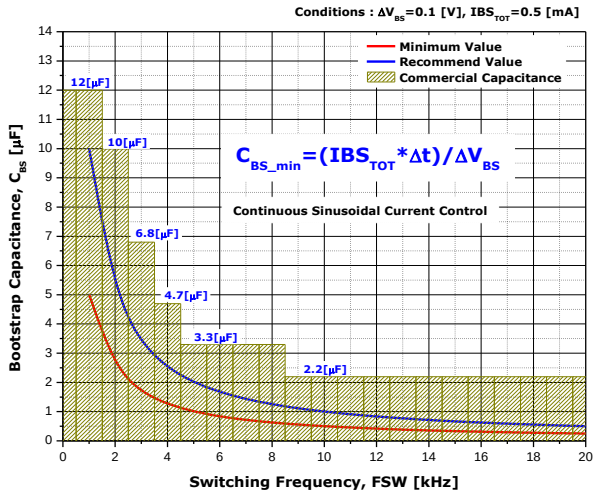


Figure 30. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Based on switching frequency and recommended ΔV_{BS}

- IBS_{TOT}: circuit current = 0.5 mA (recommended value)
- ΔV_{BS}: discharged voltage = 1 V (recommended value)
- Δt: maximum on pulse width of high-side IGBT = 2 ms (depends on application)

$$C_{BS\_min} = \frac{IBS_{TOT} \times \Delta t}{\Delta V_{BS}} = \frac{0.5mA \times 2ms}{1V} = 1.0 \times 10^{-6} \quad (3)$$

→ More than 2 times → 2 μF.

Note:
40. The capacitance value can be changed according to the switching frequency, the capacitor selected, and the recommended V_{BS} voltage of 13.0~18.5 V (from datasheet). The above result is just a calculation example. This value can be changed according to the actual control method and lifetime of the component.

Calculation Examples of Bootstrap Capacitance B;

The appropriate value for bootstrap capacitors should be selected based on operating conditions, UVBS function, and allowable recommended VB_x-VS_x

To avoid unexpected under-voltage protection and to keep V_{BS} within recommended value, bootstrap capacitance should be selected based on the operating conditions. Bootstrap voltage ripple is influenced by bootstrap resistor, load condition, output frequency, and switching frequency. Check the bootstrap voltage under the maximum load condition in the system. Figure 31 shows example of VB_x - VS_x ripple voltage during operation.

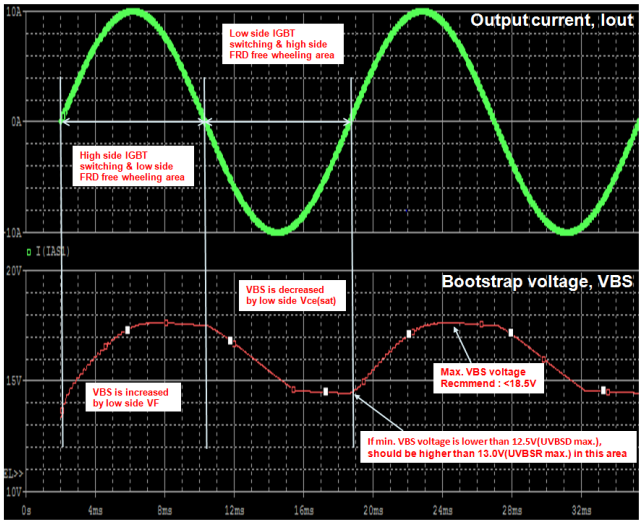


Figure 31. Recommendation of Bootstrap Ripple Voltage during Operation

6 Print Circuit Board (PCB) Design

6.1 General Application Circuit Example

Figure 32 shows a general application circuitry of interface schematic with control signals connected directly to a MCU. Figure 33 shows guidance of PCB layout for Motion SPM® 8 series.

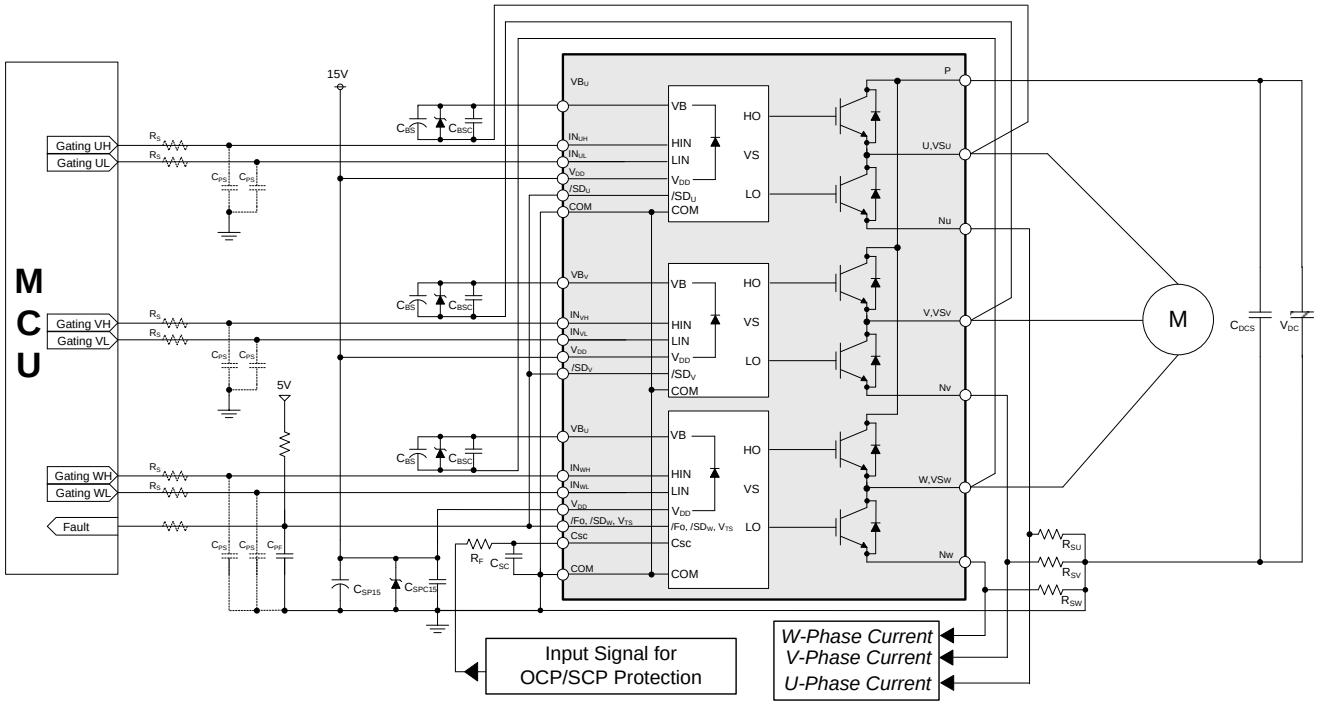


Figure 32. General Application Circuitry for Motion SPM 8 Series

6.2 PCB Layout Guidance

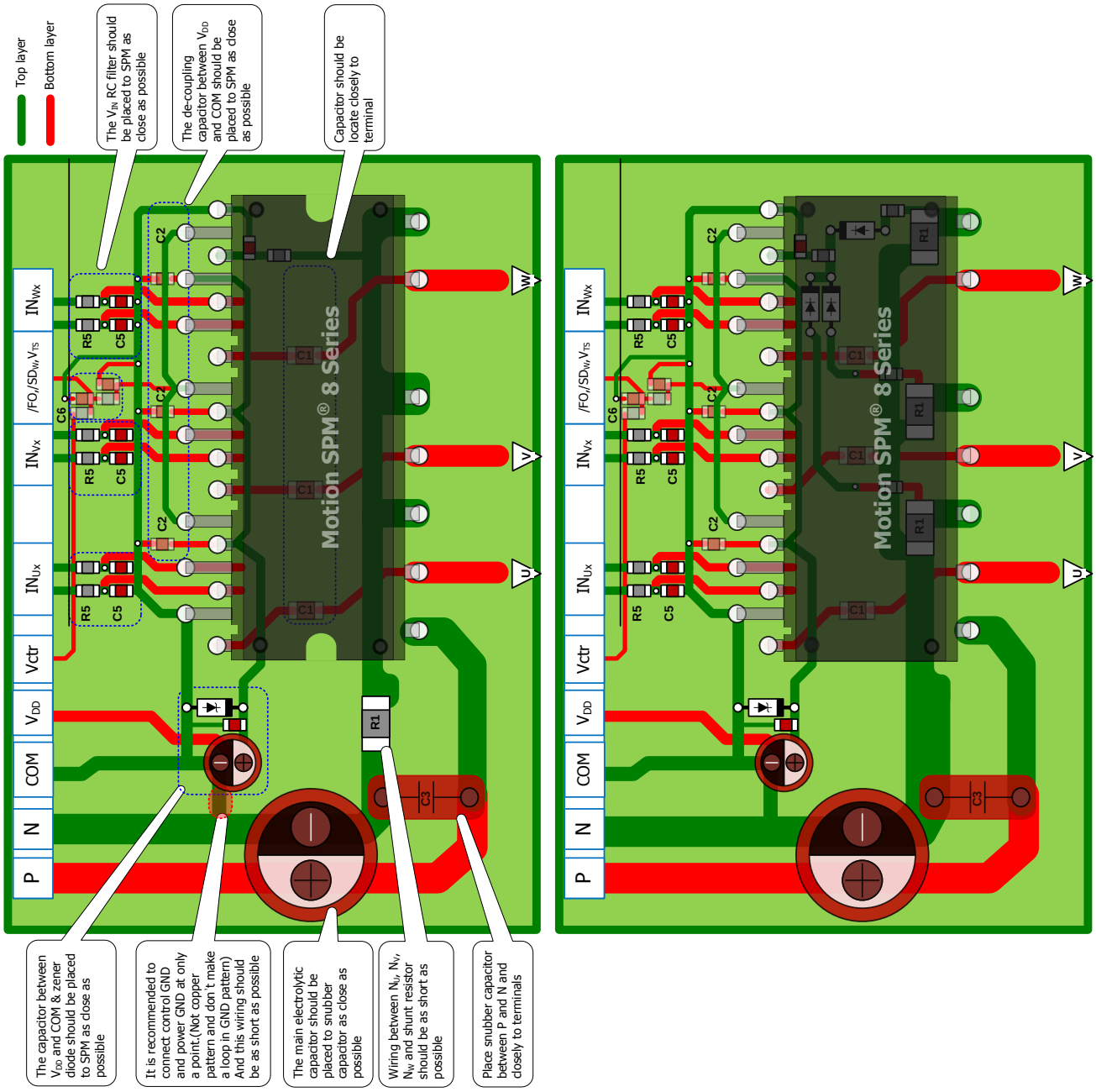
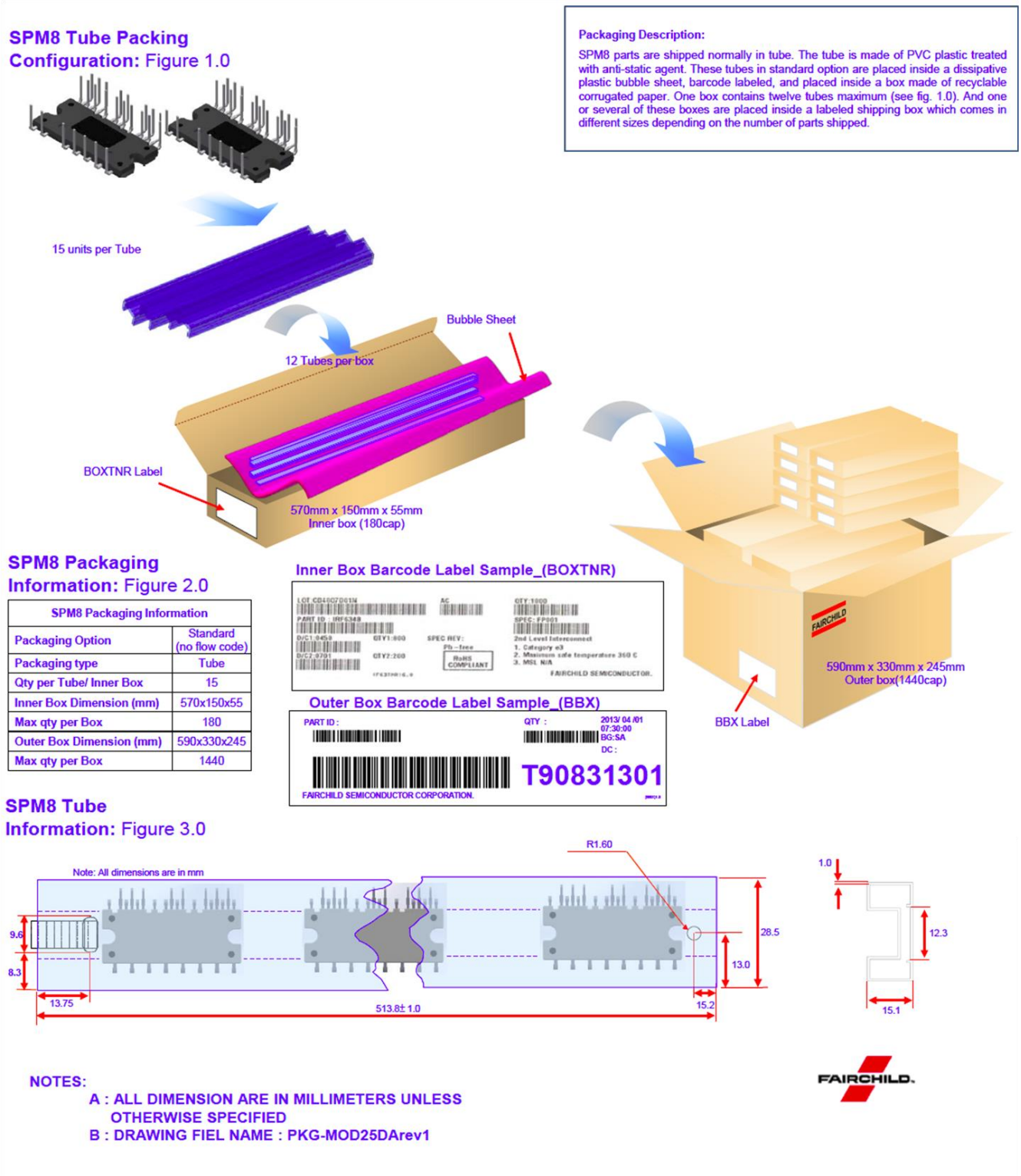


Figure 33. Print Circuit Board (PCB) Layout Guidance for Motion SPM® 8 Series (Left: One Shunt Usage, Right: Three Shunt Usage)

7 Packing Information



SPM8 Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Tube
Qty per Tube/ Inner Box	15
Inner Box Dimension (mm)	570x150x55
Max qty per Box	180
Outer Box Dimension (mm)	590x330x245
Max qty per Box	1440

Figure 34. Packing Information

8 Related Resources

FNB81060T3 Product Information

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative