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AN-5061

µSerDes™ Layout Guidelines

Summary

Fairchild's µSerDes™ devices can be used to minimize the cost and complexity associated with the design of parallel interface connections. Since these devices are capable of reducing a parallel data path to a serialized differential pair, the number of signals needed across the interface media is diminished. This reduction in signal count translates to a cost savings through decreased layer counts and size. This guide addresses some questions that might arise with the design and layout of µSerDes devices.

The serial I/O information is transmitted at a high serial rate. Care must be taken implementing this serial I/O flex cable. The following best practices should be used when developing the flex cabling:

- All four differential serial wires should be the same length
- No noisy signals over or near differential serial wires
- One ground plane or ground wire over the differential serial wires
- No test points on the differential serial wires
- Provide a separate RF ground for phones that have a metal housing
- Differential serial wires should be a minimum of 2cm from antenna
- Impedance measured from customer flex:
  - Best: 80-120ohm
  - Typical: 70-130ohm

Differential Pair Design

The µSerDes devices have been designed so that a 180-degree rotation of either device results in a straight-forward alignment of the serial clock and data lines. This arrangement is intended to make the layout of the differential trace routes as clean as possible. Typical bi-directional mode connections are shown in Figure 1.

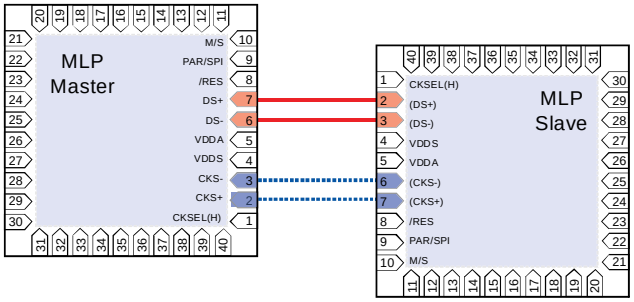

Figure 1. FIN324C Serial Port Alignment

The positive and negative signals of the differential pair must have the same length. The difference in trace length should not exceed 20mils, approximately 3ps in skew.

When designing with µSerDes devices, it is necessary to keep the lengths of the serial data pairs equivalent to the lengths of the serial clock pairs. The amount of mismatch allowed is based on the frequency of operation. The lower the frequency, the greater the allowable mismatch.

Do not route signals (differential or parallel) over any type of plane split, which results in a significant impedance discontinuity and increased loop area of return currents.

Differential pairs should be routed on the same layer and the number of vias on the differential lines should be minimized.

It is not necessary to round corners of a differential trace route: 45-degree corners are sufficient.

The main consideration with differential pairs should be electrical balance. Any discontinuity (ex. vias, pads, stubs, layer transitions, and crosstalk) introduced to one side of the differential pair should be introduced equally to the other side. Minimize discontinuities as much as possible.

Whether or not the differential traces are tightly or loosely coupled is application specific. Priority should be given to the matching of lengths between the positive and negative pairs over the trace to trace configuration.

If close coupling of the differential pairs is desired, the main consideration is to keep (S<H) and (X>5H) (see Figure 2). The important factor is that industry-standard equations are used to determine the proper dimensions to maintain a design goal or constant 100Ω differential impedance.

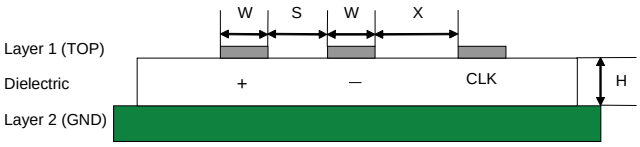

Figure 2. Differential Pair Coupling

External termination of the differential pair is not necessary because the µSerDes devices have internal termination.

When operating in unidirectional mode of the FIN12 and FIN24, the CKSO outputs of the deserializer and the CKSI inputs of the serializer are not needed. To minimize power consumption, the CKSO outputs should be allowed to float and no termination resistor should be connected. The status of the CKSI inputs is dependent on the specific device being used. All versions of µSerDes devices can have the CKSI inputs either floating or grounded. Both the (+) and (-) CKSI signals should be tied to the same potential whether floating or grounded.

Flex Cable

When working with flex cable as an interface media between the serializer and deserializer, it is important to minimize any discontinuities that may affect the signal integrity of the serial clock and data lines. The objective is to maintain a differential impedance of 100Ω throughout the serial link. Since there are various pitches of Flat Flex Cable (FFC), with and without GND shielding, there are specific signal configurations that should be followed to create the desired 100Ω impedance. For instance, when working with a 1mm pitch, unshielded flex cable, it is recommended to route with a GND-SIG1-SIG2-GND arrangement, where SIG1 and SIG2 are the positive and negative signals of the differential pair. MERITEC® developed the paper "Impedance Tests of Meritec's Laminated Flat Cable and Teflon Ribbon Cable (FRC)" that outlines the impedance of several types of flex cable with various combinations of signal configurations. The paper can be reviewed at: http://www.meritec.com/pdf/FFCImpTest187.pdf

Parallel Clock and Data Routing

The primary consideration with clock and I/O data is to route them in a manner that reduces capacitive and inductive crosstalk, while maintaining equivalent length (within system timing tolerances).

Inductive crosstalk can be reduced by at least maintaining an (X>5H) edge to edge separation between all traces (see Figure 2). This is a minimum recommendation and any distance X greater than 5H results in an even greater decrease in coupling.

Limit the length of parallel trace routes. Longer parallel lengths increase the mutual inductance and the crosstalk.

Capacitive crosstalk can be reduced by routing traces on adjacent signal layers at right angles.

To reduce the radiated emissions, as well as the susceptibility to EMI, route clock traces on stripline layers.

Where termination is necessary, it is better to use smaller surface mount components (ex. 0603 package) for lower lead inductance and pad capacitance.

If operating as a serializer in PLL-bypass mode of FIN12 or FIN24, the CKREF signal should be connected to GND and a free-running bit clock connected to the CKSI differential inputs. Refer to the datasheet for more information on PLL-bypass mode.

When operating in unidirectional mode of FIN12 or FIN24, the deserializer CKREF and STROBE signals should be connected to GND.

Unused data inputs should either be connected to ground or V_{DDP} for the FIN12 or FIN24. To minimize dynamic power due to data transitions, it is recommended that the unused signals be grouped together and tied to the same polarity. Unused output signals should be allowed to float.

Control I/O

The DIRI input pin is used to control the direction of data flow through certain µSerDes devices (FIN24, FIN12). If DIRI=0, the device is a deserializer; if DIRI=1, the device is a serializer. DIRO is an output pin that generates the complementary state of DIRI. The DIRO pin can be used in bi-directional applications where the system drives the DIRI pin of the master device and the DIRO pin of the master device can be connected to the DIRI pin of the slave device. The DIRO pin should be left floating if not used.

The functionality of S1 and S2 control pins is dependent on the µSerDes device being used. For example, the S1 and S2 pins control the direction of DP[21:24] data signals for the FIN24 device. For the FIN24A device, the S1 and S2 pins are used to define the frequency range of the CKREF input clock. Driving S1 and S2 low results in a power down and reset of the device.

Notes:

1. CKREF input frequency of the FIN24 device is internally set for operation between 10 and 30MHz.
2. The DP[21:22] input pins of the FIN24A serializer device are always outputs on the corresponding DP[23:24] pins of the deserializer device.)

Power Supply

The recommended configuration of the decoupling capacitors is shown in Figure 3. It may be necessary to change the specific capacitor values and quantities based on the frequency of operation and the number of parallel I/O.

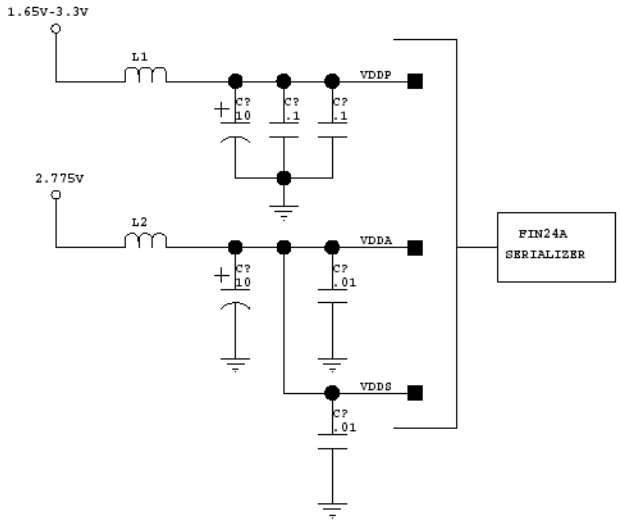

Figure 3. Recommended Supply Decoupling

When placing capacitors, try to reduce any significant amount of lead length (inductance) from the IC to the capacitor. It is often better to connect capacitor and IC pins directly into power planes with vias as close as possible to the IC pin.

It is suggested to use ferrite beads for components L1 and L2 to provide filtering for the V_{DD} power supplies. A chip bead suppresses unwanted noise on the DC power supply by creating a series impedance that varies as a function of frequency. When choosing a ferrite, it is important to:

- determine the noise frequency to be suppressed
- determine the maximum current the device draws.

Since the impedance of ferrites is generally specified at 100MHz, review the impedance versus frequency characteristics. The larger the impedance at the desired suppression frequency, the greater the effect for noise reduction. The bead should be chosen so that its DC current rating is higher than the maximum current of the device supply. It is also important to choose a ferrite with low DC resistance. TDK's ACC series of ferrite beads provides a range of frequency characteristics and DC resistances from .03Ω - .05Ω.

Create interplane capacitance by sandwiching power and GND planes with a thin dielectric. Dielectric thicknesses that are 4mils or less produce an effective high-frequency bypass capacitor (see Figure 4).

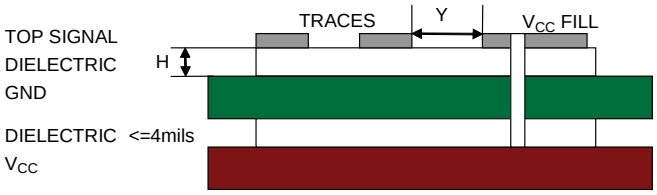

Figure 4. Decoupling Capacitor Configuration

Where possible, try to fill unused areas of signal planes with copper to provide an additional plane area. Using multiple vias to apply the appropriate voltage to the plane can increase the size of the interplane capacitance.

When filling signal planes with copper, it is important to remember to relieve the copper fill back at least five times the distance from the trace to the nearest return plane (Y=5H). The trace impedance is compromised if this is not designed properly.

When working with the MLP package, there are a few additional considerations; such as via, soldermask, and solder paste stencil design. The MLP package has a die attach paddle on the bottom that provides both heat conduction and a ground reference to the device. To take full advantage of the enhanced thermal and electrical characteristics of this package, it is recommended to review the "Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages" application note by AMKOR Technology. This paper is available at: http://www.amkor.com/products/notes_papers/MLFAppNote.pdf

Related Datasheets

FIN12AC
FIN12AC
FIN24AC
FIN24C
FIN224AC
FIN224C
FIN324C

Resources

For questions not addressed here, visit Fairchild's website at http://www.fairchildsemi.com/products/interface/userdes.html or contact Fairchild via email interface@fairchildsemi.com.

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