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LVDS Fundamentals

Introduction

With the recent developments in the communications market, the demand for throughput is becoming increasingly more crucial. Although older differential technologies provide significant signal integrity benefits compared to single-ended technologies, many of them consume much more power at lower throughput than LVDS.

The LVDS standard was created to address applications in the data communications, telecommunications, server, peripheral, and computer markets where high-speed data transfer is necessary. LVDS offers a low cost, high speed, low power solution when compared to the standards of the past.

What is LVDS?

LVDS is defined in the TIA/EIA-644 standard. It is a low voltage, low power, differential technology used primarily for point-to-point and multi-drop cable driving applications. The standard was developed under the Data Transmission Interface committee TR30.2. It specifies a maximum data rate of 655 Mbps although some of today's applications are pushing well above this specification for a serial data stream.

Compared to other differential cable driving standards like RS422 and RS485, LVDS has the lowest differential swing with a typical voltage swing of 350 mV with a typical offset voltage of 1.25V above ground. See Figure 1.

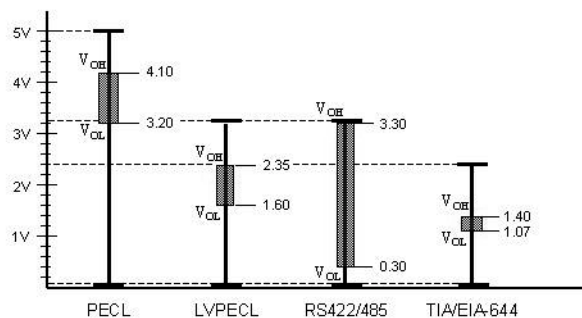


FIGURE 1. Signal Level Comparison

LVDS features a low swing differential constant current source configuration which supports fast switching speeds and low power consumption. Figure 2 shows this configuration. This allows for other features not found in single

ended technologies such as Common Mode Rejection and Failsafe, which will be discussed later in this application note.

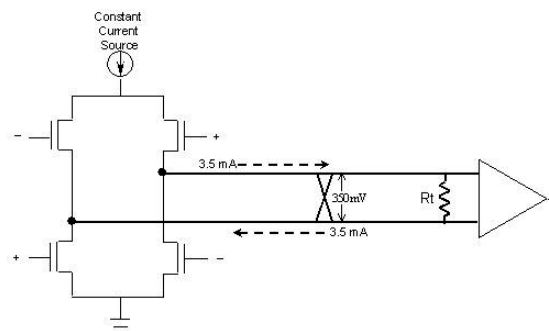


FIGURE 2. Driver/Receiver Schematic

Differential Signaling

Differential signaling offers many advantages over single ended technologies. LVDS signaling centers around 1.25V with a 350 mV swing and is not dependent on power supply voltage. Not only does this result in a faster, more stable signal, it also makes migration to lower power supply voltages much easier.

Another advantage to differential technology is that the balanced differential lines have tightly coupled equal but polar opposite signals which reduce EMI. The magnetic fields radiated by each of the conductors are drawn toward each other and cancel much of the magnetic fields.

Common Mode

Differential signaling also offers common mode rejection. The receiver ignores any noise that is coupled equally on to the differential signals and only considers the difference between the two signals. The receiver has a common mode voltage range of 0.05V to 2.35V. LVDS receivers will

operate with as much as a $\pm 1V$ ground shift between the driver and receiver. This is shown graphically in Figure 3.

Low swing differential signaling can also improve signal integrity concerns at higher speeds. As throughput demands increase throughout the information industry, higher frequencies and wider bit widths cause transmission line reflections and crosstalk. As system loading increases, the characteristic impedance of a system can change and cause impedance mismatches which will, in turn, send reflective signals across the transmission line. These reflections can cause bit errors or increase settling times making timing budgets more difficult as speeds increase. Differential signaling technologies like LVDS solve this by accepting common mode noise on the differential line. Additionally, lower swing differential technologies reduce reflections by having small voltage swings which limit the energy supplied to the transmission line.

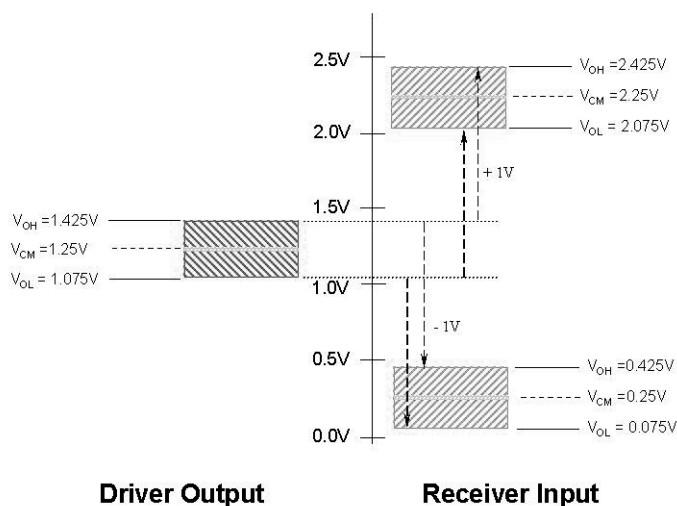


FIGURE 3. Common Mode Noise Range

Failsafe

Failsafe is a feature offered in LVDS that will help system reliability by preventing errors. Failsafe guarantees that the outputs are in a known state (HIGH) when the receiver inputs are under certain fault conditions. Without the failsafe feature, any external noise above receiver thresholds could trigger the output to an unknown state.

According to the TIA/EIA-644 standard, when the receiver inputs are open, not connected to the generator, or if the generator is powered off, the failsafe feature will drive the outputs high. If the receiver inputs are shorted, the outputs will be in failsafe mode (HIGH State). The standard also states that the receiver outputs will also go in to a failsafe if the differential inputs remain within the threshold region for an abnormal period of time.

This protection feature has many benefits for a system designer. For instance, some applications may dictate that not all of the LVDS receiver inputs are used. With the fail-

safe feature, the receiver outputs will always be in a known state as long as the inputs are not receiving a valid signal.

Termination

Termination of LVDS is necessary at the receiver input to generate the Output Differential Voltage (V_{OD}). The TIA/EIA-644 specification stipulates an internal termination resistor value between 90Ω and 132Ω . Fairchild recommends a termination resistor value between 90Ω and 110Ω depending on the characteristic impedance of the cable.

Termination of LVDS is much easier than most other technologies. ECL and PECL both use a 220Ω pull-down resistor on each driver output as well as a 100Ω resistor across the driver outputs. GTLP, due to the open drain configuration, must have a termination resistor (usually 50Ω double terminated) to a 1.5V pull-up voltage in order to generate a GTLP signal. (See Figure 4)

Differential Signaling (Continued)

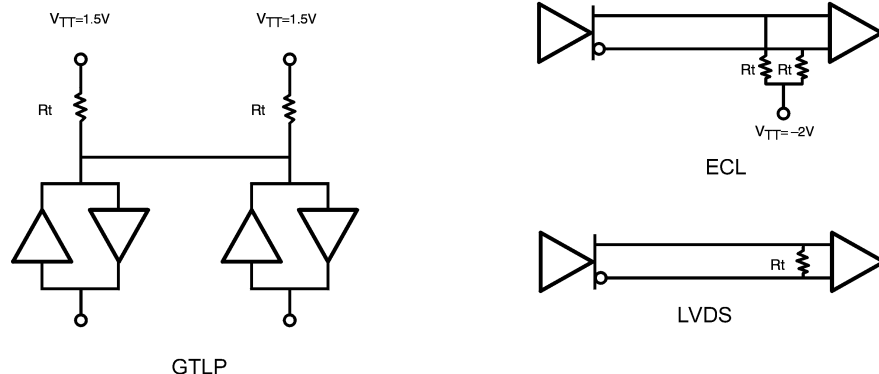


FIGURE 4. Termination

In a point-to-point system configuration, the termination resistor should be placed within 2 cm of the receiver. For a multi-drop configuration, the termination resistor should also be located within 2 cm of the last receiver.

Fast Switching Speeds

Typical slew rates for LVDS are under 1 ns when measured from 10% to 90% of the edge. When edge rates approach less than half the time of the distance to the load, the load can no longer be thought of as a lumped load and transmission line effects must be considered. Because LVDS is most often used in driving cables and in backplanes, transmission line effects are a concern for the system designer.

One of the largest contributors to bit error in medium to long cable and bus driving systems is reflections. Reflections are caused by mismatches in line impedance which cause inductive and capacitive ripples in the signal which, in turn, reduce the drivers ability to provide a clean signal to the receiver. For this reason, it is essential for the impedance of all cables, connectors, busses, and termination resistors to be closely matched. The LVDS common mode rejection feature helps to minimize reflections caused by mismatched transmission lines.

Jitter

There are many ways that digital jitter can effect a system operation. A transmission channel typically passes signals at a specific bit rate or within a range of bit rates. Jitter has the effect of shortening some bits, while lengthening others. This shortening of bits can increase the signal speed and cause dropped bits in the transmission. Additionally, excessive jitter can cause dropped bits due to the system's internal timing correction system not having the ability to track the signal.

Jitter can be defined as a type of line distortion caused by a random variation in a signal's reference timing position. The deviation can either be leading or lagging the ideal

position. Jitter is usually expressed in picoseconds (ps), as a percent (%), or as a unit interval fraction (UI) and can be caused by a number of factors including reflections, noise and crosstalk.

Jitter is divided into three basic categories: Deterministic jitter, random jitter, and frequency dependent jitter. Deterministic jitter is typically a result of phase changes which are correlated to specific events like data path bandwidth limitations. Random jitter is often caused by thermal noise and other random variables that are not necessarily related to specific events. Frequency-dependent-jitter is typically caused by things such as power supply noise and crosstalk.

Jitter is most easily shown by the use of an eye pattern. Figure 5 shows an example of an eye pattern. The size of the eye opening determines the quality of the signal, and jitter can be measured at the switch point. The eye pattern is useful for much more than to measure jitter. It is also beneficial for measuring Intersymbol Interference (ISI) - signal attenuation caused by such things as high frequency overlapping and dispersion - crosstalk, skew, and reflections.

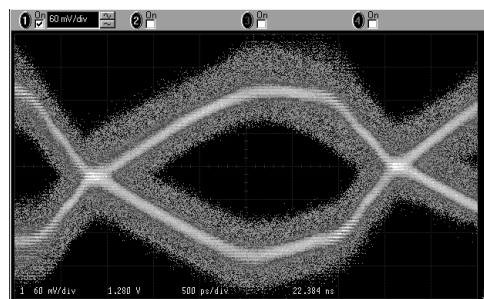


FIGURE 5. Eye Pattern at Driver Outputs

Point-to-Point Configuration

LVDS drivers and receivers perform optimally when used in systems designed as point-to-point configured systems. The transmission line must be terminated at the receiver with a termination resistor between 90Ω and 110Ω (100Ω is the recommended typical resistor value) placed as close to the receiver inputs as possible. Most twisted pair cables are designed to about 100Ω impedance, so a 100Ω termination resistor is recommended to avoid transmission line

mismatches, which will result in reflections and other discontinuities. Figure 6 shows an example of a typical point-to-point configuration using LVDS.

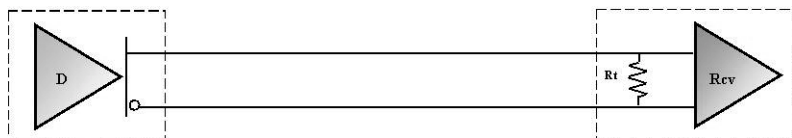


FIGURE 6. Typical Point-to-Point Configuration

Multi-Drop Configuration

LVDS can also be used in a multi-drop design typically found in backplanes as well as box-to-box applications providing the media transmission distance is short. In a typical

multi-drop system, the termination resistor must be located at the receiver that is located at the far end of the bus. This is illustrated in Figure 7.

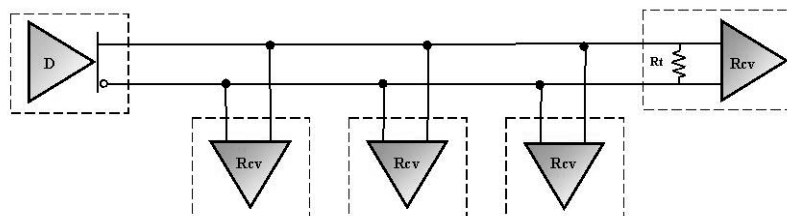


FIGURE 7. Typical Multi-Drop Configuration

When flight time from the driver to the receivers is crucial, the system can be designed to drive from the center to the bus. Termination resistors are needed at each end of the bus in order to prevent reflections. Although this arrangement is preferred when high frequencies dictate short signal propagation across the transmission line, the

termination resistors are seen by the driver as two parallel resistors and therefore the driver must provide twice the current to drive the bus. Figure 8 illustrates a multi-drop configuration with the driver at both the end of the bus and the center of the bus.

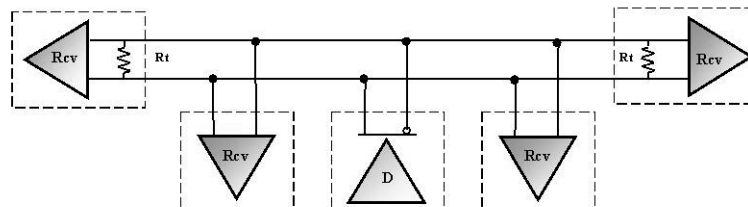


FIGURE 8. Center Driven Multi-Drop Configuration

Multi-Point Configuration

Although LVDS, as defined in the RS644 standard, does not have the dynamic current drive to support a multi-point bus system, there is a high drive LVDS available which has a higher drive compared to the 3.5 mA drive of standard LVDS. Fairchild Semiconductor works on a committee that is addressing a new specification for high drive LVDS, or M-LVDS (Multi-point Low Voltage Differential Signaling).

In a multi-point system, the driver can be located at any point along the bus. For this reason, much like the multi-drop center driven bus previously discussed, a termination resistor is required at each end of the bus. This also means that the driver sees the two resistors in parallel and must supply twice the current to the bus. The 11 mA dynamic drive is provided on the high drive version of LVDS to address a multi-point configuration. Figure 9 gives a typical example of a multi-point system.

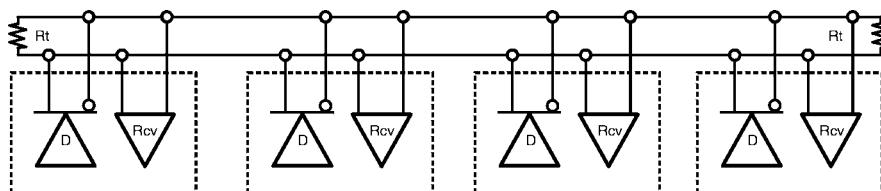


FIGURE 9. Multi-Point Configuration

Conclusion

Demands for throughputs are growing exponentially and are now exceeding several gigabits per second. Transmission of data across long media lengths demands high speed, low noise solutions. System designers are also always conscious of achieving high throughput while still conserving power. LVDS, with its low swing, differential, current driver solution, will continue to solve throughput requirements for future generations of systems.

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