

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

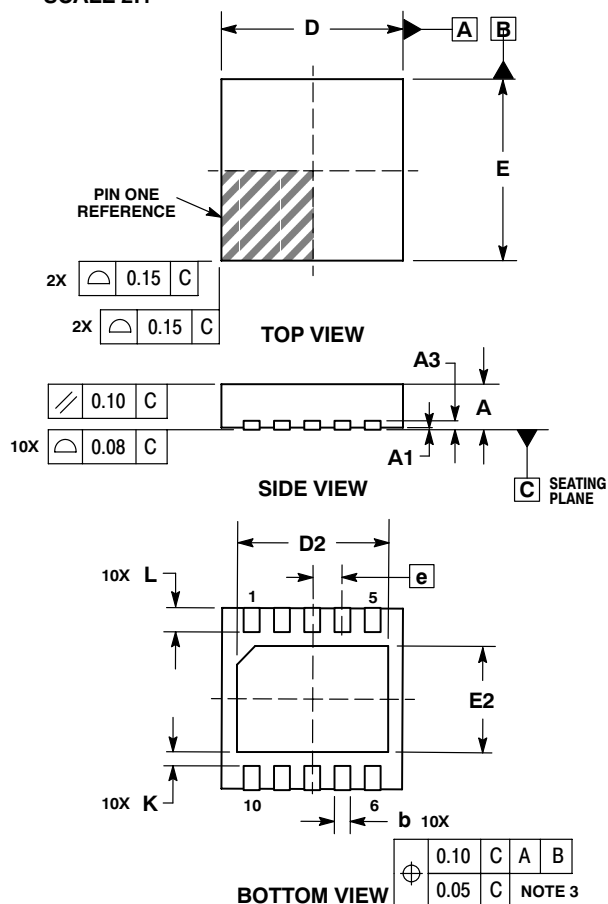
ON



WDFN10, 3x3, 0.5P  
CASE 522AA-01  
ISSUE A

SCALE 2:1

DATE 02 JUL 2007

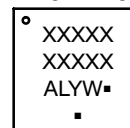


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN         | NOM  | MAX  |
| A   | 0.70        | 0.75 | 0.80 |
| A1  | 0.00        | 0.03 | 0.05 |
| A3  | 0.20 REF    |      |      |
| b   | 0.18        | 0.24 | 0.30 |
| D   | 3.00 BSC    |      |      |
| D2  | 2.45        | 2.50 | 2.55 |
| E   | 3.00 BSC    |      |      |
| E2  | 1.75        | 1.80 | 1.85 |
| e   | 0.50 BSC    |      |      |
| K   | 0.19 TYP    |      |      |
| L   | 0.35        | 0.40 | 0.45 |

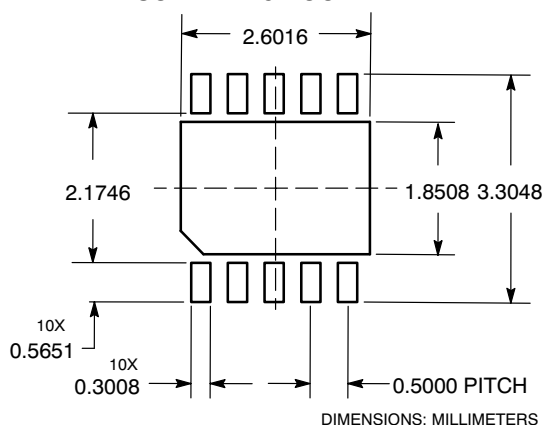
## GENERIC MARKING DIAGRAM\*



- A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.


## SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                  |                           |  |
|------------------|---------------------------|--|
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| STATUS:          | ON SEMICONDUCTOR STANDARD |  |
| NEW STANDARD:    |                           |  |
| DESCRIPTION:     | WDFN10 3X3, 0.5P          | PAGE 1 OF 2  |

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