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AN-6100

Design Guideline for Travel Adapter Applications Using FAN6230A

1. Introduction

The FAN6230A is a secondary-side synchronous rectifier (SR) controller used to drive an SR MOSFET to improve converter efficiency. FAN6230A is able to operate under both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) while maintaining accurate SR control. FAN6230A integrates a shunt regulator and an internal charge pump circuit for low Bill of Material (BOM) count and small form factor. The output voltage of the converter is used for providing bias to the secondary side, FAN6230A controller. Due to the charge pump circuit inside, FAN6230A can operate from lower converter output voltage in Constant Current (CC) mode. It also has an internal cable drop compensation function for precise constant output voltage regulation at the end of the cable. The gain for the cable drop compensation is programmed externally for both high and low line input conditions. A typical application circuit is illustrated in Figure 1.

FAN6230A is compatible with variable-frequency as well as fixed-frequency PWM controllers, and its maximum operating frequency is 200 kHz. In order to improve no-load power consumption, a green mode function is utilized. In green mode operation, FAN6230A stops switching to reduce the operating current to less than 500 µA thus minimizing switching losses.

SR turn-off is determined by the FAN6230A Linear Predict Control (LPC) algorithm which uses the principle of volt-sec balance. Detecting the drain voltage of the SR MOSFET instead of the drain current using SR MOSFET $R_{DS(ON)}$ offers additional flexibility with regards to MOSFET selection. As a result, power consumption on the SR MOSFET is significantly reduced.

This article describes a design procedure and a design example using the FAN6230A in a flyback converter for travel adapter applications. A guideline for the Printed Circuit Board (PCB) design along with several design trouble shooting notes are also described.

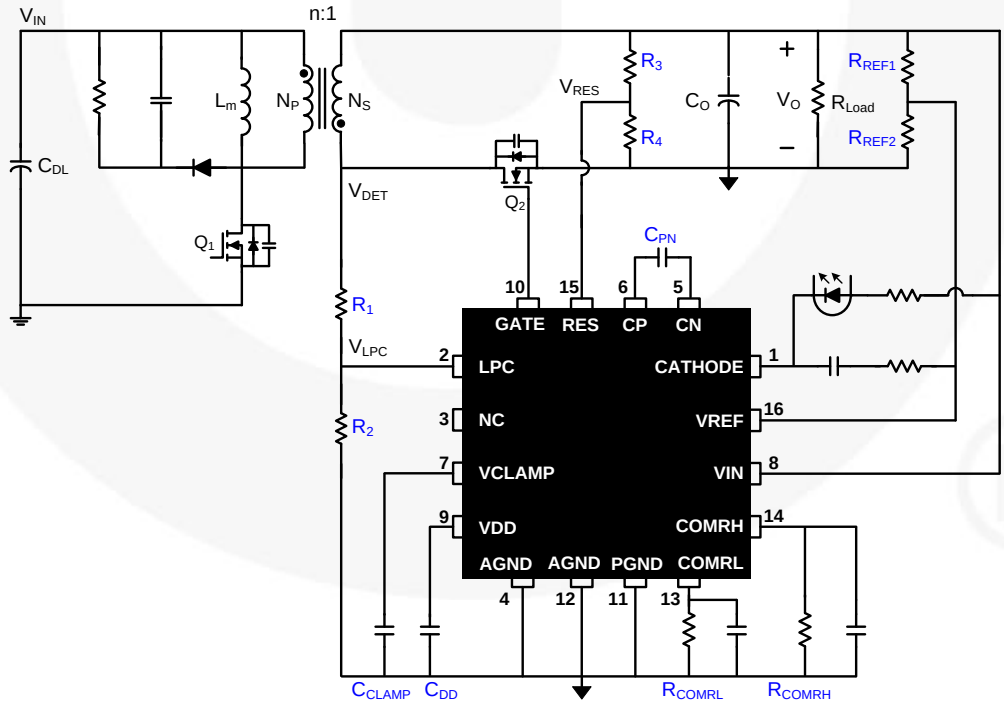

Figure 1. Typical Application Circuit for Flyback Converter with FAN6230A

2. Operation Principle

1. Power On and Off Sequence

During initial power on, the charge pump circuit is enabled when the VIN pin voltage exceeds approximately 1 V, resulting in V_{DD} being twice of VIN. When V_{DD} = 3.35 V (i.e. VIN = 1.675 V), all internal blocks in the FAN6230A are biased and ready for operation, except for SR switching. The SR gate signal will be generated 32 ms after V_{DD} = 3.35 V. If VIN becomes more than 2.6 V, the internal clamping circuit clamps VIN at 2.6 V and V_{DD} at 5.2 V.

The charge pump circuit is disabled when VIN is higher than 8 V (hysteresis 1 V) and the clamping circuit clamps VIN at 5.5 V, resulting in V_{DD} = 5.5 V.

During power off or when VIN decreases below 7 V, the clamping voltage is changed to 2.6 V and the charge pump circuit is again enabled clamping V_{DD} to 5.2 V. The SR controller remains active as long as V_{DD} is greater than 3 V.

Figure 2 shows the waveforms described above.

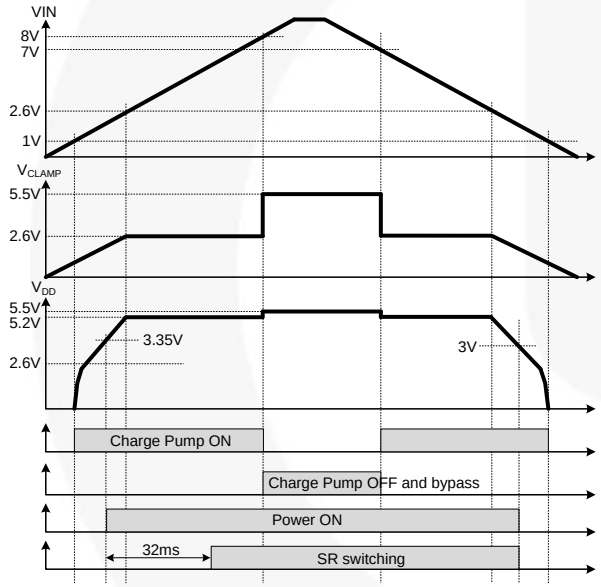

Figure 2. Power On and Off Sequence

2. Linear Predict Control for DCM Operation

As mentioned previously, SR MOSFET turn-off is determined by the Linear Predict Control (LPC) algorithm. As such, the average voltage applied to the inductor must be zero over a switching period during steady-state operation. Thus the product of the charging voltage and charging time is equal to the product of the discharging voltage and discharging time. AS shown in Figure 3 the transformer current (magnetizing inductor current) always ramps up from zero when a new switching cycle starts. Similarly, the current ramps back down to zero before the next switching cycle starts. Since the slope of the magnetizing current is determined by the voltage applied across the magnetizing inductance, the volt-sec balance equation shows when the magnetizing current returns to its initial condition after one switching cycle, as follows:

$$\frac{V_{IN}}{L_m} t_{ON,PWM} = \frac{nV_O}{L_m} t_{L,DIS} \quad (1)$$

where V_{IN} is the input voltage applied to the primary side of the transformer, V_O is the output voltage of the converter (=VIN for FAN6230A), L_m is the magnetizing inductance of the transformer, n is the turns ratio of the transformer, $t_{ON,PWM}$ is the primary switch turn-on time, and $t_{L,DIS}$ is the discharge time of L_m.

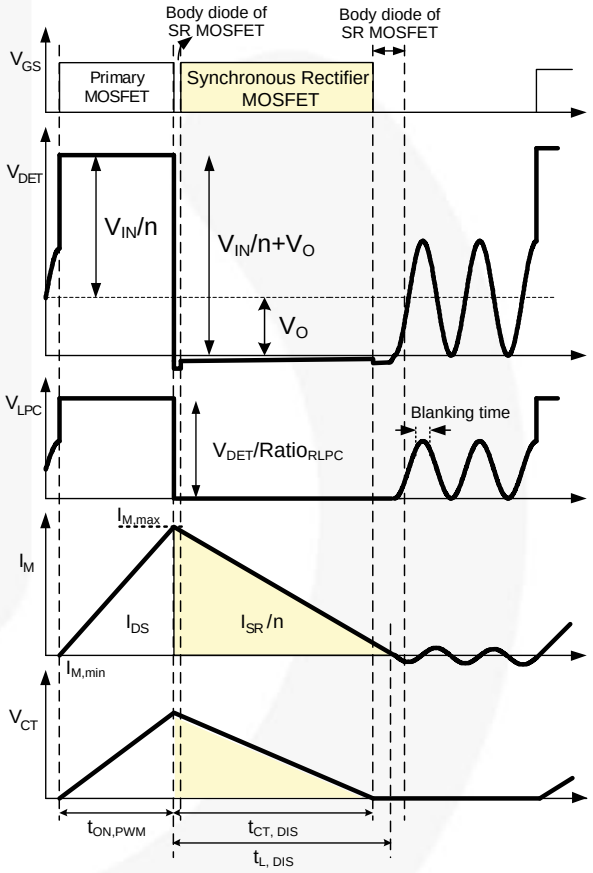

Figure 3. Operation of LPC in DCM Flyback

Figure 3 shows the typical LPC waveforms during DCM operation, where I_{DS} is the primary MOSFET current, I_{SR} is the SR MOSFET current, and I_M is the magnetizing current of L_m. The discharge time of the internal timing capacitor is less than the discharge time of L_m ($t_{CT,DIS} < t_{L,DIS}$) to guarantee the SR gate is turned off before the SR current reaches zero.

The LPC circuit generates a replica (V_{CT}) of the flyback transformer magnetizing current using an internal timing capacitor (C_T), as shown in Figure 4. V_{LPC} is obtained by dividing V_{DET} which is equal to $V_{IN}/n+V_O$. V_{RES} is proportional to V_O, while i_{CHR} is proportional to V_{DET} and i_{DISCHR} is proportional to V_{RES}. Thus C_T is charged by i_{CHR}-i_{DISCHR} which is proportional to V_{IN} and discharged by

i_{DISCHR} which is proportional to V_O, resulting in the waveform of V_{CT} being similar to the waveform of I_M.

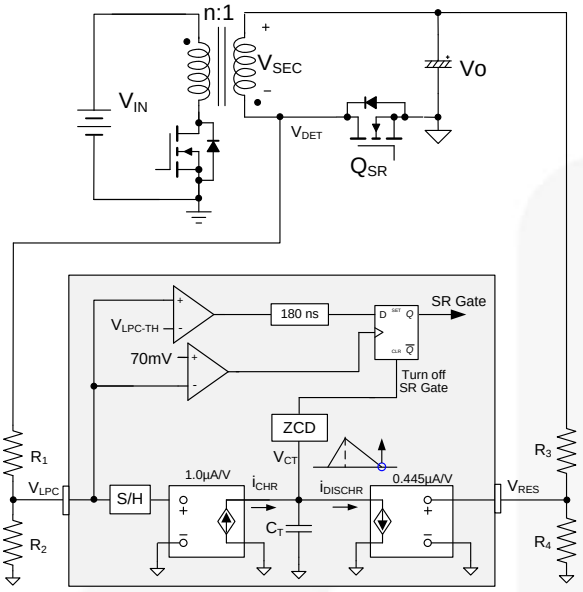

Figure 4. Simplified LPC internal block

3. Causal Function for Transient Mode

Even though the linear predict method anticipates the SR current zero crossing instant very effectively in DCM operation, it has limitations during transient CCM operation. This is because the magnetizing current does not return to its initial condition at the end of the switching cycle, as illustrated in Figure 5. Thus, the LPC results in late termination of the SR gate, which can cause shoot-through since both primary side and secondary side MOSFETs are on at the same. To guarantee reliable SR control over all operating modes, a second SR control method called Causal Predict Control (CPC) is also employed in the FAN6230A.

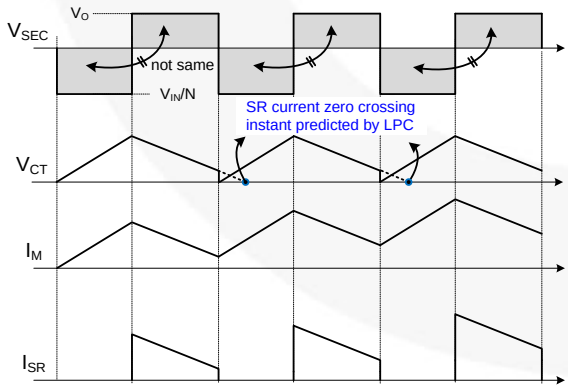

Figure 5. Magnetizing Current Waveform during Transient in CCM

CPC anticipates the SR current zero crossing instant based on the switching period of the previous switching cycle as illustrated in Figure 6. The causal predictive SR control algorithm is based on the assumption that the switching frequency does not change significantly between two consecutive switching cycles.

As can be seen in Figure 6, CPC anticipates the SR current to cross zero later than the actual zero crossing in DCM, while LPC predicts the actual SR current zero crossing instant more precisely. For CCM operation, LPC anticipates the SR current to cross zero later than the actual zero crossing. On the other hand, CPC anticipates the SR current zero crossing instant properly in CCM.

FAN6230A uses the zero crossing anticipation signals from LPC and CPC and whichever signal is introduced first triggers the turn-off of the SR switch.

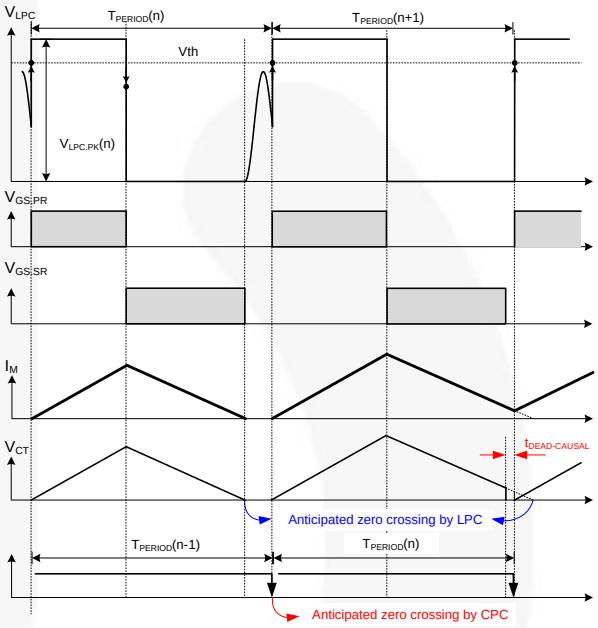

Figure 6. Operation of CPC in Transient CCM

3. Design Considerations

1. Operating Frequency

According to the specification for "linear operation range of the causal function", t_{CAUSAL_LINEAR}, the operating frequency of the FAN6230A is limited from 33 kHz to 200 kHz. In addition, the maximum operating frequency is also determined by the specification of "minimum LPC time to enable the SR gate at high/low line", $t_{LPC\text{-}EN\text{-}H/L}$. If the turn-on time of the primary side MOSFET, $t_{ON,PWM}$ is shorter than $t_{LPC\text{-}EN\text{-}H/L}$, the LPC voltage is not recognized as a valid signal resulting in SR being disabled and efficiency lowered.

2. Allowable Turns Ratio of Transformer

For a flyback converter operating in DCM, the primary side MOSFET drain voltage ($V_{DS.PRI}$) oscillates when the secondary side diode current reaches zero. This oscillation is caused by the resonance between the effective output capacitance of the primary MOSFET and magnetizing

inductance of the transformer. This also causes a similar oscillation on the SR MOSFET drain voltage ($V_{DS.SR}$) as illustrated in Figure 7 and Figure 8, where the peak-to-peak amplitude of the SR drain voltage can be as much as twice the output voltage. As input voltage is decreased, causing the oscillation amplitude ($2\ V_O$) to be larger than the nominal SR drain voltage ($V_{IN}/n+V_O$), the oscillation on the LPC voltage can cause inadvertently shrink the SR gate signal in the next cycle since the oscillation is clamped at the peak. To avoid abnormal operation, it is recommended to design the proper turns ratio of the transformer such that SR gate voltage does not shrink when SR MOSFET voltage of 90% ($0.9\ V_{DS.SR.PK}$) is greater than $2\ V_O$.

Equation (2) shows the maximum allowable turns ratio to avoid the shrink of the SR gate signal.

$$0.9 \cdot \left(\frac{V_{IN\,(\min)}}{n} + V_O \right) > 2V_O$$

$$\Rightarrow n < \frac{V_{IN\,(\min)}}{\left(2V_O / 0.9 - V_O \right)} = \frac{V_{IN\,(\min)}}{1.22V_O} \quad (2)$$

where $V_{IN(min)}$ is the minimum input voltage applied to the primary winding of the transformer, taking into consideration of the ripple on C_{DL}.

It is also required to verify the design of the transformer turns ratio taking into consideration the functionalities of the controller used in the primary side.

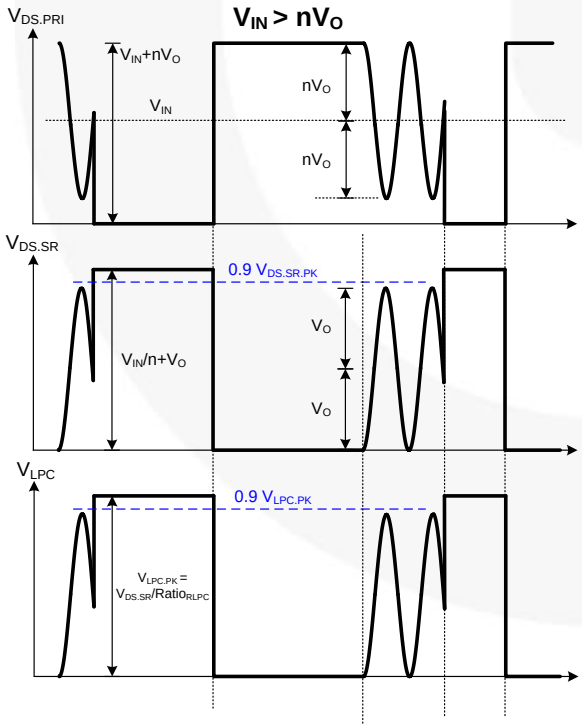

Figure 7. Normal Operation with $V_{IN} > nV_O$

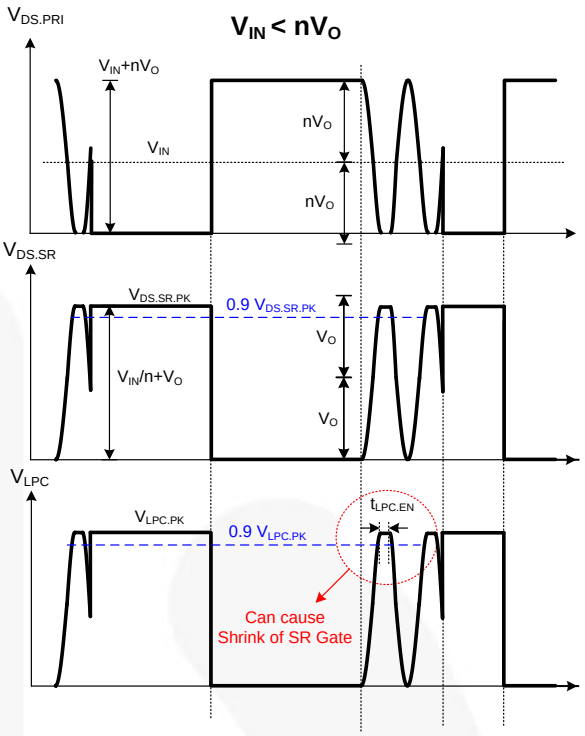

Figure 8. SR Gate Signal Shrink due to the Resonance with $V_{IN} < nV_O$

4. Design Procedure

The FAN6230A is divided into two notable partitions: an SR controller to control the SR MOSFET and a shunt regulator for providing an error signal used to regulate the outputs. The design procedure for the shunt regulator section, i.e. feedback network design procedure is described in the other Fairchild Application Notes such as AN-4137, AN-4150. A design procedure for the SR control and cable drop compensation will be presented in this section.

For the design example, the system specifications are as follows:

- Input voltage range: 90 ~ 264 V_{AC} (50 ~ 60 Hz)
- Nominal output voltage: 5 V
- Minimum output voltage in CC range: 2 V (40% of the rated value)
- Nominal output current in CC Mode: 2.5 A

Figure 9 shows the profile of the output voltage and current for the given example.

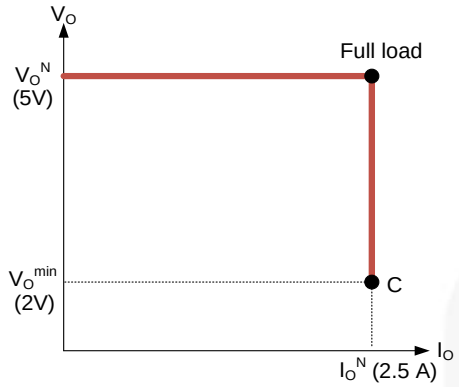

Figure 9. Output Voltage and Current Profile

[STEP-1] Determine V_{DD}, V_{CLAMP}, and V_{PN} (between CN and CP pin) Capacitors

The output voltage of the converter is connected to the VIN pin supplying bias voltage, $V_{DD,}$ to the FAN6230A. If VIN is lower than 8 V, it is clamped at 2.6 V and doubled by the charge pump circuit, which is supplied to the internal bias circuit maintained by an external capacitor. Thus V_{DD} is 5.2 V. If VIN is higher than 8 V, it is clamped at 5.5 V and supplied to the internal bias circuit directly. Considering voltage ripple, 1 µF capacitors are recommended for V_{DD}, V_{CLAMP}, and V_{PN} capacitor values.

[STEP-2] Determine the Resistors on REF Pin

FAN6230A integrates a shunt regulator with low bias current for reducing BOM component count, as illustrated in Figure 10.

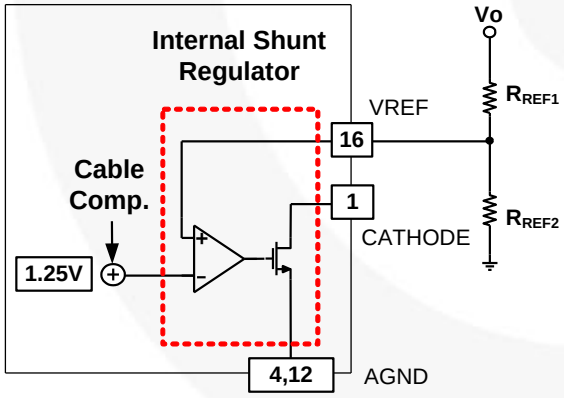

Figure 10. Typical Application Circuit for the Shunt Regulator Section

The output voltage divider R_{REF1} and R_{REF2} should be determined such that the voltage of the VREF pin is 1.25 V, as follows:

$$\frac{R_{REF1}}{R_{REF2}} = \frac{V_O}{1.25} - 1 \qquad (3)$$

Selection of 1% tolerance resistors for better output regulation is recommended. Since the maximum reference input current is 4 µA, R_{REF1} can be as large as approximately 1 MΩ. However, using a lower R_{REF1} value will result in better response time with regards to following the output voltage. The trade-off between response time and power consumption with regards to meeting standby power requirements must be considered when optimizing the design of the R_{REF1} and R_{REF2} divider.

(Design Example)

The VREF resistor is obtained as:

$$\frac{R_{REF1}}{R_{REF2}} = \frac{V_O}{1.25} - 1 = \frac{5}{1.25} - 1 = 3$$

By setting R_{REF2} = 9.09 kΩ, R_{REF1} is obtained as 27.4 kΩ. Then the power consumption on the resistors is as:

$$P_{loss} = \frac{V_O^{\,2}}{R_{REF1} + R_{REF2}} = \frac{5^2}{9.09k + 27.4k} = 0.68mW$$

[STEP-3] Determine the Resistors on LPC and RES Pins

Figure 11 shows the FAN6230A LPC and RES pin circuitry. One voltage divider is used for the LPC pin by dividing the V_{DET} voltage, while a second voltage divider is used for the RES pin by dividing the output voltage. When calculating the four resistors, it is first necessary to determine the range of the ratio of LPC resistors ($Ratio_{RLPC}$ = $(R_1+R_2)/R_2$). Secondly, it is necessary to determine the range of the ratio of RES resistors ($Ratio_{RRES}$ = $(R_3+R_4)/R_4$) considering the detection range of the RES pin. Once $Ratio_{RLPC}$ and the voltage scaled-down ratio, K ($Ratio_{RLPC}/Ratio_{RRES}$), are determined, $Ratio_{RRES}$ is used to calculate the RES divider resistor values. The selection f the four divider resistors begin by choosing the optimal resistance value for R_1 and R_3 according to the sink current for each pin.

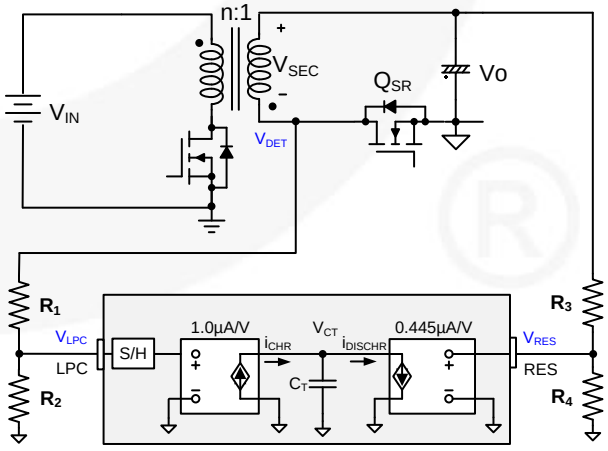

Figure 11. Typical Application Circuit for LPC and RES Pins

1. Determine the range of LPC ratio: There are three conditions to determine the range of the LPC ratio, as depicted in Figure 12.

(1) At minimum input voltage with full load condition, V_{LPC} should be higher than the SR enabled threshold voltage at low line and 5 V output, $V_{LPC-HIGH-L-5V}$, as follows:

$$\frac{V_{DET\_90V_{AC}}(\min)}{Ratio_{RLPC}} > V_{LPC-HIGH-L-5V}(\max) \quad (4)$$

where $V_{DET\_90VAC(min)}$ is the minimum V_{DET} when the input voltage is minimized considering the ripple on the primary side input capacitor C_{DL} depending on the load condition. $V_{DET\_90VAC(min)}$ is described as follows:

$$V_{DET\_90V_{AC}}(\min) = \frac{V_{IN\_90V_{AC}}(\min)}{n} + V_{O(\min)} \quad (5)$$

where V_O is the output voltage, n is the turns ratio of the transformer, and $V_{IN\_90VAC(min)}$ is the minimum input voltage on C_{DL} applied to the primary side of the transformer at 90 V_{AC}. Thus,

$$Ratio_{RLPC} < \frac{\frac{V_{IN\_90V_{AC}}(\min)}{n} + V_{O(\min)}}{V_{LPC-HIGH-L-5V}(\max)} \quad (6)$$

(2) At low line input (115 V_{AC}), V_{LPC} should be less than the high-to-low line threshold voltage on LPC pin at 5 V output, $V_{LINE-L-5V}$, to ensure the operation range at low line, as follows:

$$\frac{V_{DET\_115V_{AC}}(\max)}{Ratio_{RLPC}} < V_{LINE-L-5V}(\min) \quad (7)$$

where

$$V_{DET\_115V_{AC}}(\max) = \frac{\sqrt{2}V_{IN\_115V_{AC}}}{n} + V_{O(\max)} \quad (8)$$

Thus,

$$Ratio_{RLPC} > \frac{\frac{\sqrt{2}V_{IN\_115V_{AC}}}{n} + V_{O(\max)}}{V_{LINE-L-5V}(\min)} \quad (9)$$

(3) In order to avoid that the green mode operation stops and returns to normal operation during no load operation, V_{LPC} should be less than the threshold voltage on LPC rising edge at low line and 5 V output, $V_{LPC-TH-L(min)}$, as follows:

$$\frac{V_{O(\max)}}{Ratio_{RLPC}} < V_{LPC-TH-L-5V}(\min) \quad (10)$$

where $V_{O(max)}$ is the maximum DC output voltage plus the maximum peak ripple voltage. Thus,

$$Ratio_{RLPC} > \frac{V_{O(\max)}}{V_{LPC-TH-L-5V}(\min)} \quad (11)$$

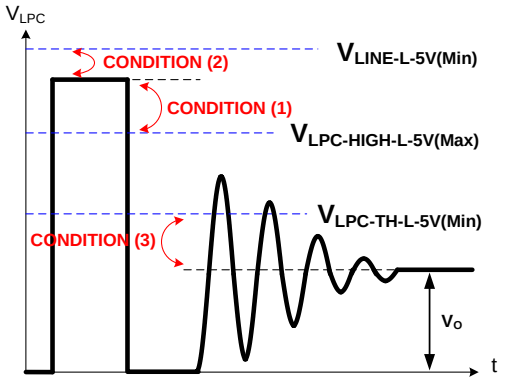

Figure 12. Conditions for Determining $Ratio_{RLPC}$

2. Determine the range of RES ratio: There are two conditions to determine the range of RES ratio for normal operation of FAN6230A, as depicted in Figure 13.

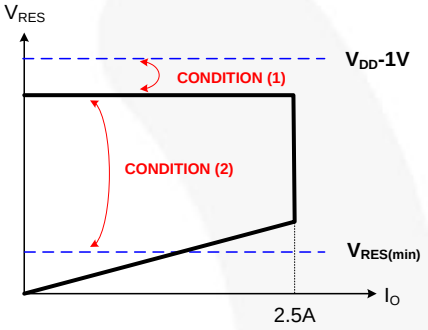

Figure 13. Conditions for determining $Ratio_{RRES}$

(1) To ensure the linear operation range of the RES pin, V_{RES} should be lower than the minimum value of V_{DD} minus 1 V.

$$\frac{V_{O(\max)}}{Ratio_{RRES}} < V_{DD(\min)} - 1V \quad (12)$$

where $V_{DD(min)}$ is the minimum supply voltage. Thus,

$$Ratio_{RRES} > \frac{V_{O(\max)}}{V_{DD(\min)} - 1V} \quad (13)$$

(2) V_{RES} should be higher than the $V_{RES(min)}$ to assure the SR gate signal is enabled normally, as follows:

$$\frac{V_{O(\min)}}{Ratio_{RRES}} > V_{RES}(\min) \quad (14)$$

where $V_{O(min)}$ is the minimum DC output voltage plus the minimum peak ripple voltage. Thus,

$$Ratio_{RRES} < \frac{V_{O(\min)}}{V_{RES}(\min)} \quad (15)$$

Taking an unintentional delay with internal parasitic capacitance into account, R_4 is suggested to be equal or less than 40 kΩ. R_2 is suggested to be less than the 15 kΩ. As shown in Figure 3, when the secondary starts to conduct current, the SR MOSFET drain-to-source voltage, V_{DS}, is

negative. In order to avoid the LPC pin from being damaged by the negative voltage, the LPC pin internally sources current when V_{LPC} is less than 0 V. Therefore, R_2 cannot be too small to clamp negative voltage on the LPC pin. After the resistance of R_2 and R_4 are determined, R_1 and R_3 can be calculated with proper ratio selection.

3. Determine the voltage scaled-down ratio K: The basic idea of the linear predict method is to estimate the instant when the magnetizing current of the transformer goes back to its initial condition after completing one switching cycle by emulating the operation of the magnetizing inductor current. Two voltage-controlled current sources and an internal timing capacitor C_T are used to emulate the charging and discharging of the magnetizing inductance.

The current which charges the internal capacitor C_T while V_{LPC} is high is given by Equation (16) as:

$$i_{CT1} = \frac{\frac{V_{IN}}{n} + V_O}{Ratio_{RLPC}} \times 1 \times 10^{-6} - \frac{V_O}{Ratio_{RRES}} \times 0.445 \times 10^{-6} \quad (16)$$

Whereas, the current discharging the internal capacitor C_T while V_{LPC} is low is given by Equation (17) as:

$$i_{CT2} = \frac{V_O}{Ratio_{RRES}} \times 0.445 \times 10^{-6} \quad (17)$$

The current-sec balance of CT which is equivalent to the volt-sec balance of the magnetizing inductance is as follows:

$$\left(\frac{\frac{V_{IN}}{n} + V_O}{Ratio_{RLPC}} - \frac{0.445 V_O}{Ratio_{RRES}} \right) \times t_{ON,PWM} = \left(\frac{0.445 V_O}{Ratio_{RRES}} \right) \times t_{ON,SR} \quad (18)$$

where $t_{ON,PWM}$ is the turn-on time of the primary side MOSFET and $t_{ON,SR}$ is the turn-on time of the SR MOSFET. By substituting the voltage scaled-down ratio K (=$Ratio_{RLPC}$/$Ratio_{RRES}$) into Equation (18), Equation (19) is obtained as follows:

$$\left(\frac{2.25}{K} \times \left(\frac{V_{IN}}{n} + V_O \right) - V_O \right) \times t_{ON,PWM} = V_O \times t_{ON,SR} \quad (19)$$

By setting K=2.25, the volt-sec balance equation is obtained. Thus, the C_T voltage decreases to zero when the SR current decreases to zero. Considering the tolerance of the resistor dividers and internal circuit tolerances, the coefficient K should be slightly larger than 2.25 to guarantee that the SR gate is turned off before the SR current reaches zero.

(Design Example)

Assume C_{DL} = 24 µF with a charging time ratio over a half line cycle period given as 0.21 (D_{ch}), the output voltage ripple is ± 5%, the voltage drop due to the load cable is 0.21 V, and the estimated efficiency of the converter is 87%. Then $V_{IN\_90VAC(min)}$ can be obtained as follows:

$$V_{IN\_90V_{AC}(min)} = \sqrt{2 \cdot V_{IN\_90V_{AC}}^{\ 2} - \frac{(V_O + 0.4) \times I_O}{\eta} \cdot \frac{1 - D_{ch}}{C_{DL} \cdot f_{L,min}}}$$

$$= \sqrt{2 \cdot 90^2 - \frac{5.21 \times 2.5}{0.87} \cdot \frac{1 - 0.21}{24\mu \cdot 50}} = 79.6V$$

where $f_{L,min}$ is the minimum line frequency. The first condition for the range of $Ratio_{RLPC}$ is obtained using a given transformer turns ratio of 13 as follows:

$$Ratio_{RLPC} < \frac{\frac{V_{IN\_90V_{AC}(min)}}{n} + V_{O(min)}}{V_{LPC-HIGH-L-5V(max)}} = \frac{\frac{79.6}{13} + 4.96}{0.74} = 14.98$$

The second and third conditions for the range of $Ratio_{RLPC}$ are as follows, respectively:

$$Ratio_{RLPC} > \frac{\frac{\sqrt{2} V_{IN\_115V_{AC}}}{n} + V_{O(max)}}{V_{LINE-L-5V(min)}} = \frac{\frac{\sqrt{2} \cdot 115}{n} + 5.46}{1.6} = 11.23$$

$$Ratio_{RLPC} > \frac{V_{O(max)}}{V_{LPC-TH-L-5V(min)}} = \frac{5.46}{0.55} = 9.93$$

Therefore, the range of $Ratio_{RLPC}$ is obtained as follows:

$$11.23 < Ratio_{RLPC} < 14.98$$

The first and second conditions for the range of $Ratio_{RRES}$ are as follows, respectively:

$$Ratio_{RRES} > \frac{V_{O(max)}}{V_{DD(min)} - 1V} = \frac{5.46}{5.2 - 1} = 1.3$$

$$Ratio_{RRES} < \frac{V_{O(min)}}{V_{RES(min)}} = \frac{4.96}{0.4} = 12.4$$

Therefore, the range of $Ratio_{RRES}$ is obtained as follows:

$$1.3 < Ratio_{RRES} < 12.4$$

Based on experimental result, Select K = 2.7 and $Ratio_{RLPC}$ = 12.12, then the $Ratio_{RRES}$ is obtained as follows:

$$Ratio_{RRES} = \frac{Ratio_{RLPC}}{K} = \frac{12.12}{2.7} = 4.4$$

It meets the conditions: higher than 1.3 and lower than 12.4. So $Ratio_{RRES}$ is chosen as 4.4.

Select R_2 = 11 kΩ and R_4 = 32.4 kΩ, then R_1 and R_3 can be calculated as follows, respectively:

$$R_1 = R_2 \times (Ratio_{LPC} - 1) = 122\ k\Omega$$

$$R_3 = R_4 \times (Ratio_{RES} - 1) = 110\ k\Omega$$

[STEP-4] Determine the Compensation Gain for the Cable Drop

While one end of a charging cable is connected to the output terminals of the travel adapter, the phone-side battery is located at the other end of the cable. Even if the output voltage of the converter is regulated exactly at its nominal value, the phone-side voltage at the other end of the cable is lower due to the cable impedance. As such, the more output current, the more voltage drop. In order to compensate for the voltage drop measured across the charging cable, the FAN6230A has a built-in cable compensation circuit which provides regulated constant voltage at the phone side end of the cable, when operating in CV Mode. The voltage drop across the cable is compensated by adjusting the reference voltage of the internal shunt regulator in proportion to the output current as shown in Figure 14.

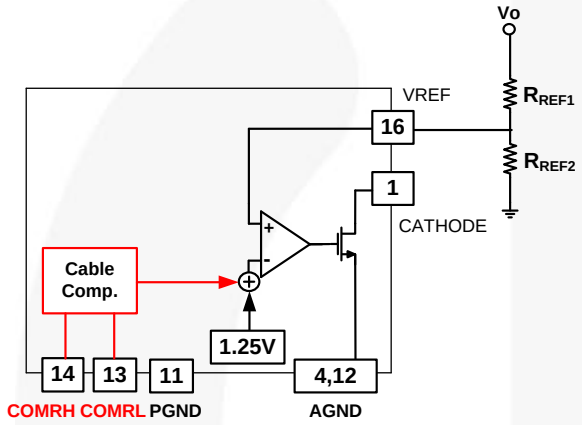

Figure 14. Cable Voltage Drop Compensation

The CATHODE pin of the FAN6230A is typically connected to an opto-coupler to implement feedback to the primary side controller. The cable drop compensation in FAN6230A is programmed by external resistors on COMRH and COMRL pins, whose relationship can be described as follows:

$$V_O = \left(1 + \frac{R_{REF1}}{R_{REF2}}\right) \cdot \left(1.25 + 0.8 \cdot t_{ON,SR} \cdot R_{COMRH} \cdot \frac{t_{ON,SR}}{t_S}\right) \quad (20)$$

$$V_O = \left(1 + \frac{R_{REF1}}{R_{REF2}}\right) \cdot \left(1.25 + 0.8 \cdot t_{ON,SR} \cdot R_{COMRL} \cdot \frac{t_{ON,SR}}{t_S}\right) \quad (21)$$

where R_{COMRH} and R_{COMRL} are the external resistors on the COMRH and COMRL pins, respectively and t_S is the switching frequency of the primary side controller.

It is recommended that a 47 nF bypass capacitor is placed in parallel with the resistors for COMRH/L when the cable drop compensation function is used for positive feedback degradation. Since the output current is estimated based on the conduction time of the SR MOSFET, the cable drop compensation gain should be adjusted if the operating mode (CCM or DCM) changes with line voltage. Thus, FAN6230A has two pins for cable drop compensation gain setting (COMRH and COMRL) for high/low lines, respectively. When the compensation gain doesn't have to be adjusted with line voltage, connect the COMRL pin to V_{DD}. In this case, the cable drop compensation gain for low line and high line is solely determined by the resistor on the COMRH pin. The COMRH and COMRL pins can be also shorted to ground if no cable drop compensation is required.

To make it easy to find the compensation resistance, a graph based on Equations (20) and (21)is illustrated, as shown in Figure 15. The y-axis is the output voltage drop due to the cable which should be compensated and the x-axis is the compensation resistance.

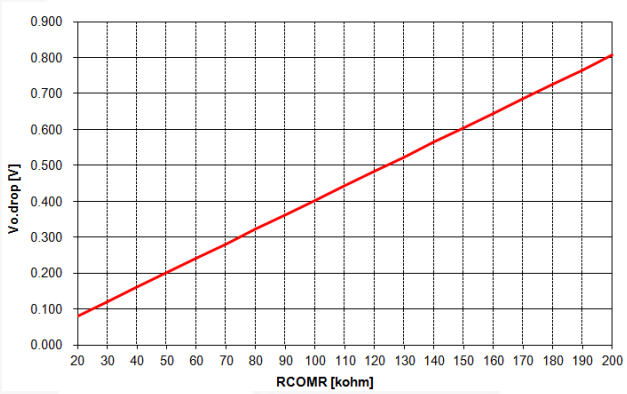

Figure 15. Voltage Drop vs. R_{COMR}

(Design Example)

Assuming a 24 AWG, 1 m cable length is used (0.0842 Ω/m), the voltage drop at maximum output current is obtained as follows:

$$\Delta V_O = R[\Omega/m] \times l[m] \times I_O = 0.0842 \times 1 \times 2.5 = 0.2105\,V$$

According to the graph in Figure 15, R_{COMR} is selected as 51.1 kΩ in parallel with a 47 nF bypass capacitor on both COMRH and COMRL pins.

5. Trouble Shooting Notes

1. Dead-Time Needs To Be Adjusted

If the SR dead-time is too large, it is recommended to decrease R_1 or increase R_2 of LPC pin. Then V_{LPC} is increased and the discharge time of the C_T capacitor ($t_{CT.DIS}$) is prolonged to decrease the dead-time, as shown in Figure 16. However, Equation (7) must still be satisfied when increasing V_{LPC}.

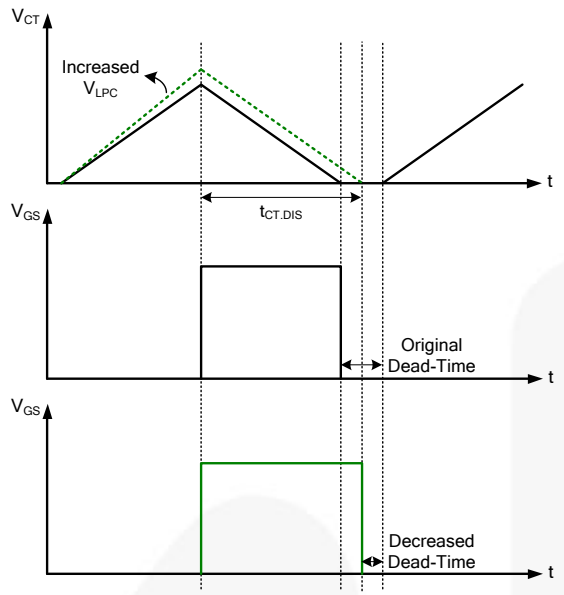

Figure 16. Adjusting SR Dead-Time by increasing V_{LPC}

In contrast, if SR dead-time is too small, it is suggested to decrease R_3 or increase R_4. Then V_{RES} is increased and the discharge time of the C_T capacitor is reduced to increase the dead-time, as shown in Figure 17. However, Equation (12) must still be satisfied when increasing V_{RES}. A dead time of 700 ns at full load is recommended for mass production (MP).

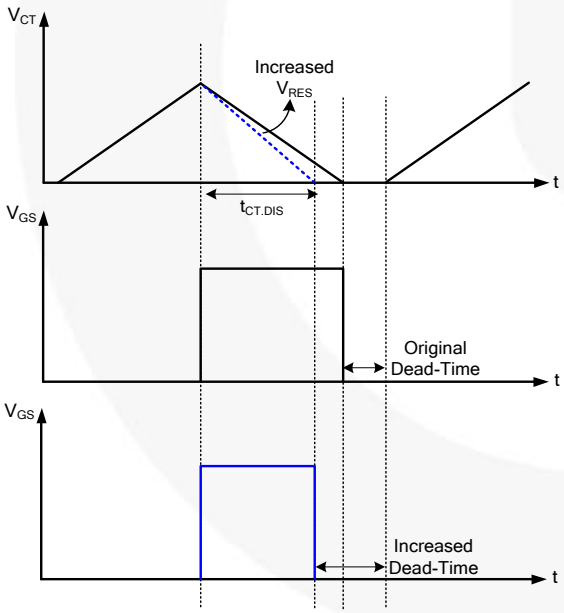

Figure 17. Adjusting SR Dead-Time by decreasing V_{RES}

2. FAN6230A Is Unable To Enter Green Mode

One of the conditions to enter green mode is based on the V_{LPC} period. If the non-switching state remains longer than 330 µs ($t_{GREEN-ON}$) measured between V_{LPC} falling and V_{LPC} rising of the next cycle, the SR circuit enters green mode. If the FAN6230A cannot enter into green mode, it is recommended to verify that the non-switching state lasts longer than $t_{GREEN-ON}$ and V_{LPC} is lower than V_{LPC-TH} under the given operating condition *(see Equation (10))*.

3. SR Does Not Switch

If the FAN6230A is not in green mode and the SR switch does not operate, try the following: First, verify that V_{DD} is at its nominal regulated value. If V_{DD} < 4 V or appears unstable, it is possible that the IC is damaged, try to change C_{DD} or increase the capacitor value to 10 µF. Second, check if V_{LPC} is equal to the $V_{DET}/Ratio_{RLPC}$ and if V_{LPC} might be exceeding $V_{LPC-HIGH-L}$ (Equation (4)). Third, check if V_{RES} is equal to $V_O/Ratio_{RRES}$. Additionally, verify whether there might be an overshoot or undershoot during V_{DET} rising and falling detection. If noise on the RES pin is excessive, due to poor PCB layout, a small capacitor (several tens of pF) can be added in parallel with R4. Fourth, add a resistor (around 20 kΩ) between the GATE pin and PGND of the FAN6230A to protect GATE pin from any negative voltage spikes during turning on.

4. SR Switched for a while and Shuts Down Repetitively

In steady-state, the SR MOSFET switches on and off in a switching cycle, as determined by the LPC or CPC functions. However, since the charging and discharging of inductor current are not always balanced during load and AC line transient, the SR gate signal can be overlapped with the next gate signal of the primary MOSFET. Therefore, FAN6230A has several integrated protection functions such as LPC-voltage falling detect protection, causal period protection, and RES-voltage drop protection that prevent overlapping due to volt-sec imbalance. Once any of these protections are triggered, FAN6230A will terminate SR switching or shrink the pulse width of the SR gate signal immediately and then return to normal operation after the abnormal conditions are cleared. Refer to the FAN6230A datasheet for the detailed descriptions.

6. PCB Layout Guidelines

Printed Circuit Board (PCB) layout and design are very important for CCCV switching mode power supplies where the voltage and current can rapidly change. Applying proper PCB layout techniques minimize excessive Electro-Magnetic Interference (EMI) and prevent the power supply from being disrupted during surge and Electro-Static Discharging (ESD) tests. As shown in Figure 18, C_{DL} and C_O are the input and output capacitors, respectively, T is the isolation transformer, Q_1 is the primary side main MOSFET, and Q_2 is the secondary side SR MOSFET controlled by the FAN6230A. For optimal FAN6230A performance, the following PCB layout design guidelines are recommended:

- The main power flows through the secondary side winding, C_O and Q_2. So it is better to configure the loop, formed by the secondary side winding, C_O and Q_2, as small as possible.
- The power ground ① (for V_{LPC}) should be connected to power ground ② (for V_{RES}) first and then both are together connected to PGND pin (Trace ① → ② → PGND).
- The charge pump output provides driving power to the SR MOSFET, so it is better to make the path from the GATE pin to the gate of the Q_2, and from the Q_2 source to the ground of C_6 as small as possible. The power ground ③, ④ and ⑤ are connected together and then connected to the PGND pin of the FAN6230A (Trace ③ → ④ → ⑤ → PGND).
- Resistor R_{REF1} and R_{REF2} sense the output voltage. The ground of R_{REF2} can be connected to the ground of C_O to achieve optimal voltage regulation. The ground of the R_{REF2} should return to AGND of the IC directly to minimize noise (Trace ⑥ → AGND).
- Resistor R_{COMRH} and R_{COMRL} are used for cable drop compensation. The grounds of both resistors should be connected together first and then connected to the AGND pin of the IC (Trace ⑦ → AGND).
- A Y-CAP should be connected to the C_O ground using a wide trace on the secondary side as indicated by the red wire shown in Figure 18.
- Finally, the AGND and PGND of the IC should be connected together with one single wire as indicated by the orange wire shown in Figure 18. It is important to make the ground traces as wide as possible for lower parasitic inductance and better noise immunity.

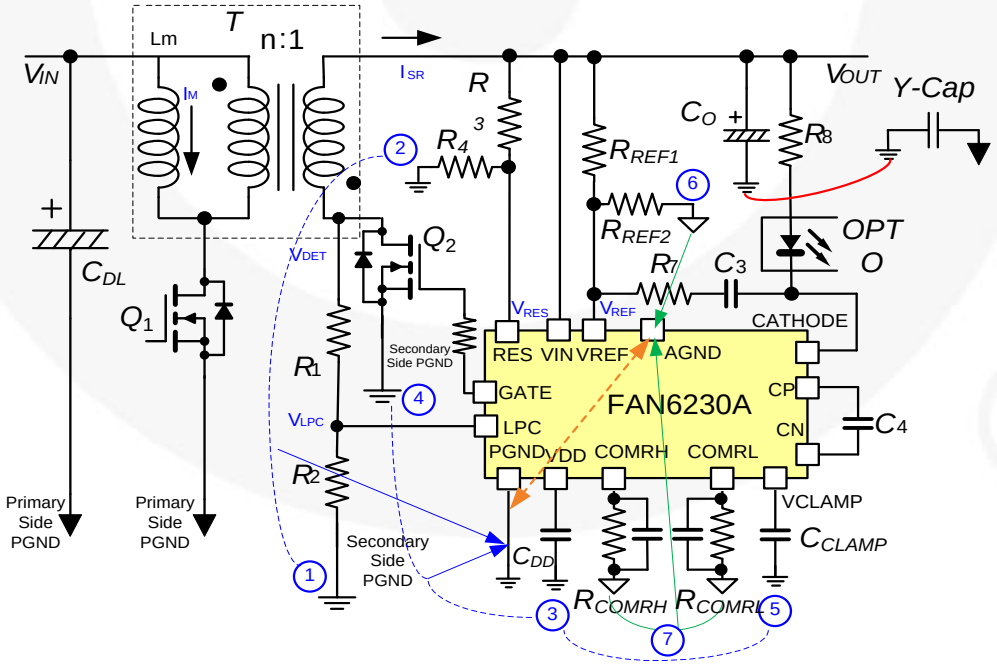

Figure 18. Recommended Layout

7. Schematic of Design Example

This section shows a design schematic for a 12.5 W charger (5 V/2.5 A) using FAN501 and FAN6230A as shown in Figure 19. An EPC1716 core is used for the transformer and the winding structure is shown in Figure 20.

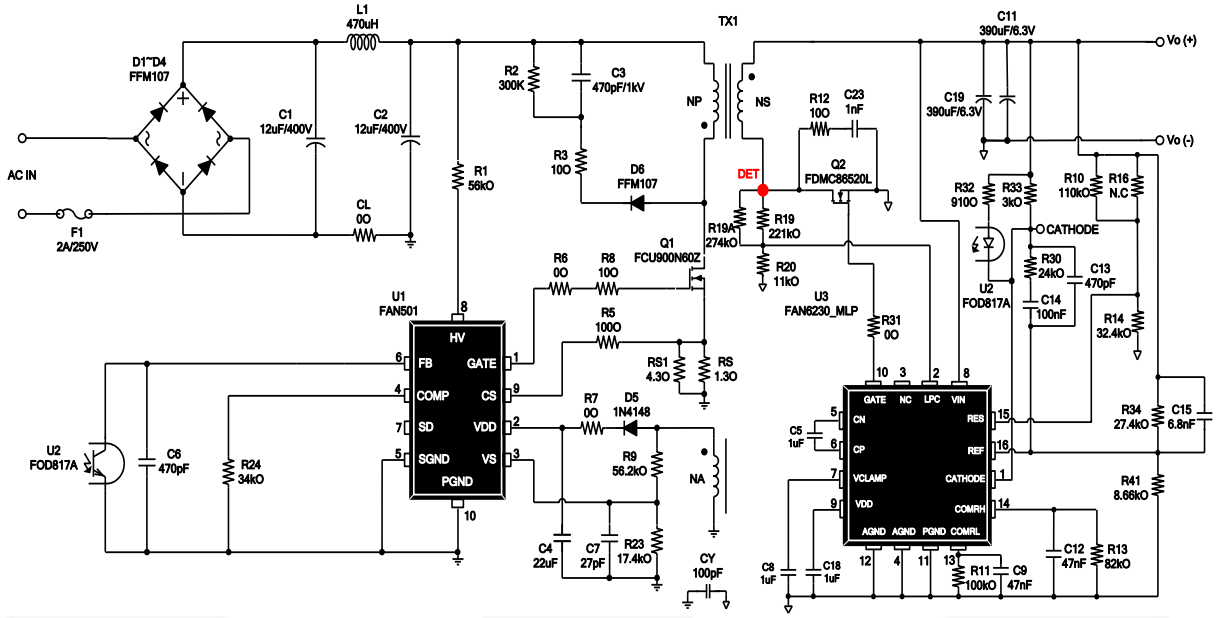

Figure 19. Schematic of the FAN6230A 12.5 W Design Example

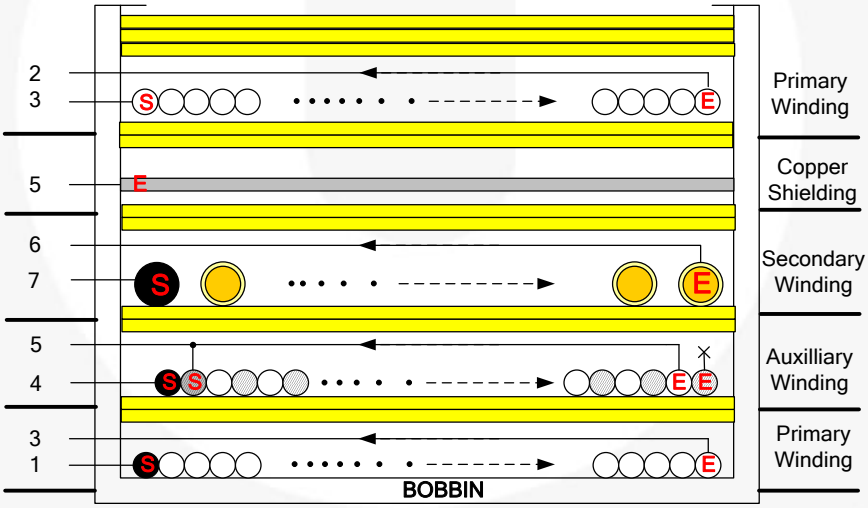

Figure 20. Transformer structure

- Core: EPC-1716 PC95, Bobbin: EPC-1716.
- W1-1 & W1-2 are sandwich winding, four layers in total.
- W2 consists of one layer with a cancellation method. The number of turns for each layer is specified below.
- W3 consists of one layer with triple-insulated wire. The leads of positive and negative; flying leads are 3.5 cm and 2.5 cm, respectively.
- W4 consists of one layer for wire shielding

Winding	Margin Tape (mm)	Terminal (Pin)	Wire Gauge (mm)	Turns (T)	Note
Bobbin					
W1-1	0	1→3	0.27 ψ*1	26	± 5 %, 1 V/1 kV
Insulation Tape 2 T					
W2	0	4→5	0.2 ψ* 2	8	Winding by cancellation
	0	5→X	0.2 ψ* 2	8	
Insulation Tape 2 T					
W3	0	7→6	0.6 ψ*2	4	TEX-E
Insulation Tape 2 T					
W4	0	5→X	Copper Shielding	1	Tight
Insulation Tape 2 T					
W1-2	0	3→2	0.27 ψ* 1	26	± 5%, 1 V/1 KV
				1	
Insulation Tape 3 T					
Copper shielding to Pin 5 (ψ0.25mm)					
Insulation Tape 2 T					

Specification	Terminal(pin)		Remark
Primary-Side Inductance	1 – 2	540 μH ± 5%	80 kHz, 1 V
Primary-Side Effective Leakage	1 – 2	< 30 μH Max.	Short All Other Pins

8. Test Results of Design Example

Figure 21 shows the experimental waveforms under full load condition (2.5 A) and AC low line from a 5 V/12.5 W evaluation board. The SR gate is turned off by causal function control in CCM operation and has a dead time between the primary-side and secondary-side MOSFET.

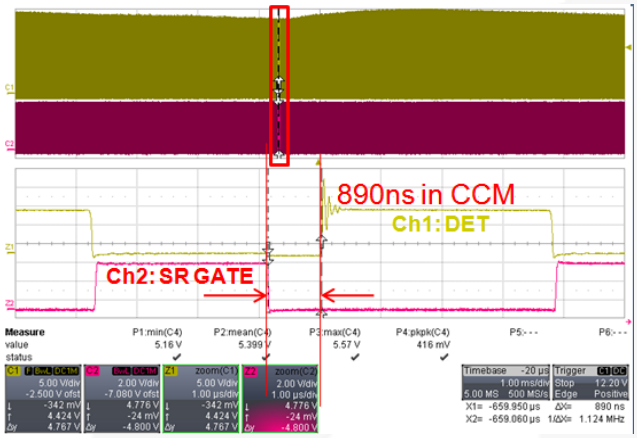

Figure 21. Waveforms at Full Load & Low Line

Figure 22 shows the experimental waveforms under full load condition (2.5 A) and AC high line. LPC turns the SR MOSFET off to prevent overlap with primary MOSFET in DCM operation.

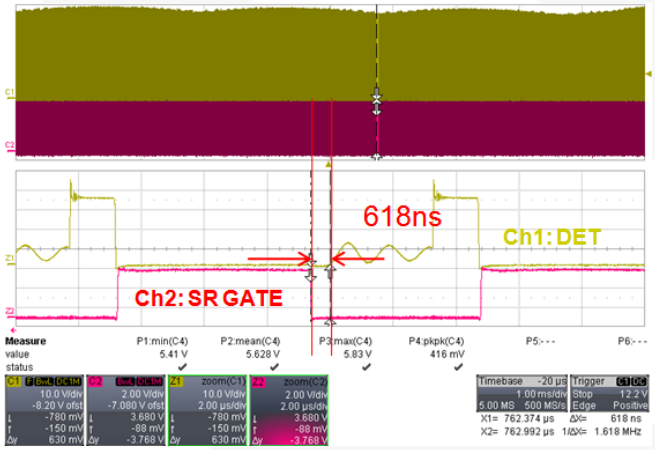

Figure 22. Waveforms at Full Load & High Line

Figure 23 shows the experimental waveforms of CC operation and the output voltage reaches to 1.6 V at AC low line. There is no apparent gate signal overlap between the primary side and secondary side MOSFETs, and the SR is still conducting by the charge pump circuit.

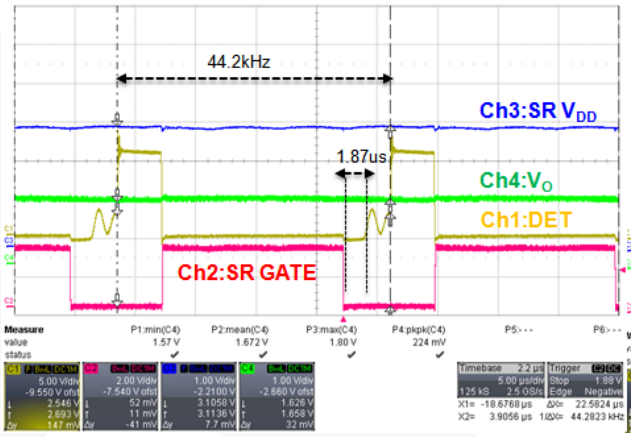

Figure 23. SR Operating with Low V_O (1.6 V) in CC Regulation Mode

Figure 24 shows the measured efficiency for different load conditions at high/low input line voltage. The average efficiencies at 115 V_{AC} and 230 V_{AC} are 87.6% and 86.55%, respectively.

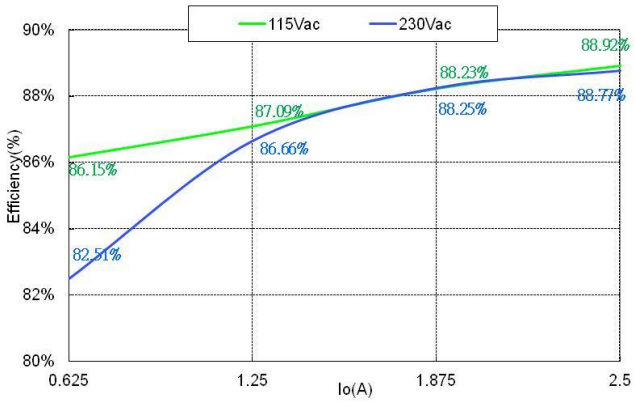

Figure 24. Measured Efficiency

Related Datasheets

FAN6230AMPX — Synchronous Rectification Controller for Flyback and Forward Freewheeling Rectification

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