



Implementing a 310 W Power Supply with the NCP1027, NCP1910 and NCP4303

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APPLICATION NOTE

The following document describes a switch mode power supply (SMPS) with 5 V_{sb} @ 2 A and 12 V @ 25 A output intended for use as part of an ATX power supply. The reference design consists of a double sided 200 x 130 mm printed circuit board with a height of only 35 mm. An overview of the entire SMPS architecture is provided in Figure 1. Achieving a maximum efficiency of 94% at 50%

load and 230 V_{ac}, this reference design achieves > 92% at 50% load and 115 V_{ac}.

This reference document provides a detailed view of the performance achieved with this design in terms of efficiency, performance, and other key parameters. In addition, a detailed list of the bill-off-materials (BOM) is also provided.

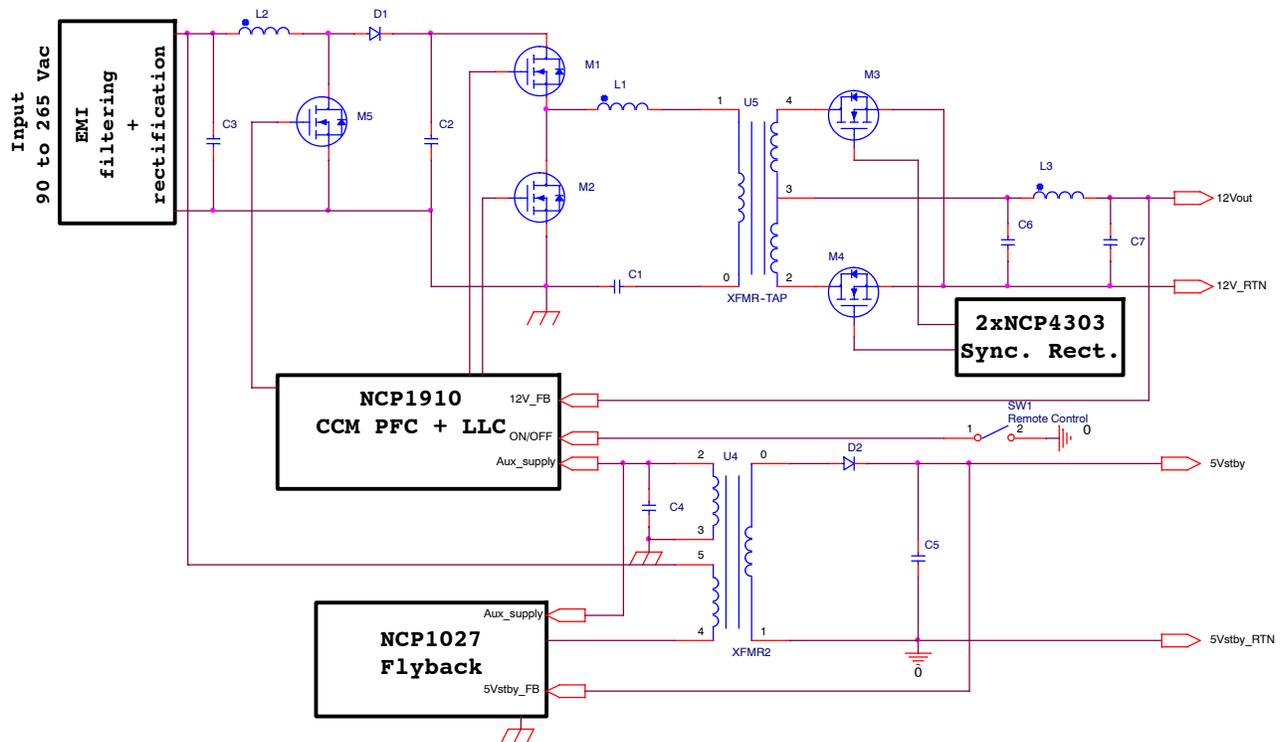


Figure 1. Demo Board Block Diagram

Architecture Overview

Most of today's computing applications like ATX PC use 12 V as the main power rail. This voltage is then further decreased to 5 V and 3.3 V by dc-dc step down converters. Because nearly all power passes through the 12 V output, it is critical that the efficiency of the main power stage is optimized. Most designs today utilize an LLC topology for the power stage to provide high efficiency at a reasonable cost. The LLC power stage provides inherently high efficiency results thanks to zero voltage switching (ZVS) on the primary side and zero current switching (ZCS) on the secondary side. Efficiency however decreases for higher output currents as the secondary RMS current reaches a high level. The solution for these losses on the secondary side is to use synchronous rectification instead of conventional rectifiers (Schottky diode).

The circuit utilizes a Continuous Conduction Mode (CCM) PFC to provide a well regulated PFC output voltage that allows optimization of the downstream converter, and also to minimize the input current ripple.

The ATX kind of power supply needs a remote signal to enable/disable the main output and a power good signal to inform the system for start-up or shut-down. In this demo board,

- For the remote on/off, NCP1910 reserves a dedicated on/off pin to reduce the surrounding circuits. In the demo board, a switch is used to control the on/off pin and hence the operation of main power. A green LED (LED1) indicates the operation status.
- As for the power good signal in the ATX power supply, it is usually managed by a supervisory chip at the secondary side to control the power good timing and also the Over-Current Protection (OCP), Over-Voltage Protection (OVP), Under-Voltage Protection (UVP) on the outputs. It usually needs an enable signal from primary side or from the winding of transformer to start the timing processing and protection features. NCP1910 provides a power good output signal (PGout pin) to instruct this enable signal through opto-coupler. In the demo board, a green LED (LED2) is used to indicate the power good output pin status.

Housed in a SO-24WB package, the NCP1910 combines not only the control core of CCM PFC and LLC, but also the handshakes among PFC, LLC, and the secondary side. These handshakes signals include the remote on/off and the PGout pin mentioned above; and also internal signals to monitor the status of PFC and LLC converter to have correct operation and protection procedures. Rather than jumping directly to the board description, it is interesting to enumerate the various features we have packed in this part.

To have a correct start-up on LLC converter, it is preferred to let PFC operate and regulate the bulk voltage before LLC starts operation. The most popular method on the application with the discrete controllers is to use a high voltage sensing rail to monitor the bulk voltage, so-called brown-out feature, to enable or stop the operation of LLC.

However, it is noted that it is not easy to determine at which bulk voltage to start up the LLC converter especially when the regulated bulk voltage is close to the peak of sinusoidal input. To ensure the operation of LLC converter, the start-up level of bulk voltage is usually designed at below the peak value of the sinusoidal input line. It has a risk that the bulk voltage at start-up phase might be too low to provide a smooth rising waveform on main output. Besides, if there is something wrong in the PFC stage, e.g. the driving resistor is broken; the LLC stage will still operate even when the input ac voltage is at high line.

To avoid the above risk, NCP1910 uses an instinctive logic to control the operating of PFC stage and LLC stage:

- At start-up phase, LLC is inhibited until PFC regulates the bulk voltage.
- LLC can not work continuously if PFC does not regulate the bulk voltage.
- For the protections, there are two kinds of behavior:
 - ♦ If the detected failure is *not* critical, the protection behavior of PFC or LLC does *not* influence or stop each other *immediately*. For example, when the brown-out block finds the bulk voltage is too low, it stops the LLC only, but does not stop PFC. Similarly, the line brown-out block stops the PFC and change the status of PGout signal as the ac input voltage is too low, but stops LLC only after a certain delay (t_{DEL2}) instead of turning-off immediately, which ensures the correct turn-off sequence from falling of power good signal to loss of main output.
 - ♦ If the failure is critical, then both PFC and LLC stop *immediately*. For example, when LLC faces a short circuit situation so that its current information is above latch-off level, both PFC and LLC stop together. Or in case that the PFC feedback loop is out of order so that bulk voltage is above the latch-off level, which is sensed on a dedicated pin (OVP2), then both PFC and LLC stop together.

Let's see an example mentioned above about what happens if PFC driver resistor is broken at high line, e.g. $265 V_{ac}$ ($V_{peak} = \sqrt{2} \cdot 265 = 374 V$). Usually the brown-out level of LLC converter is lower than 374 V, so the LLC will keep operating even when PFC driver resistor is broken. There is no critical concern in this situation but just lost of the PFC function. The electricity company may not be happy with this situation. To avoid this symptom, NCP1910 implements a so-called "*PFC abnormal*" feature by sensing the V_{CTRL} (the output of PFC Operational Trans-conductance Amplifier). If V_{CTRL} is out of its operating range for longer than 1.4 second typically, then PFC latches off. Because this situation is not critical to LLC, LLC doesn't stop immediately. Instead, it stops after 5 ms typically (t_{DEL2}).

Thanks to the combination of the two control cells in NCP1910, the FB pin which represents the information of bulk voltage is also used as the input of comparators to adjust

bulk voltage level to deliver the power good output signal and brown-out of LLC. The benefit of this feature is that it saves the extra high voltage sensing rails and provides accurate control for power good and brown-out level for LLC.

The efficiency requirement is more challenging at low line compared to high line because of the conduction losses on EMI and PFC stage, e.g. the current sense resistor on the PFC stage. To reduce the power losses on this PFC current sensing resistor, the easiest way is to reduce its resistance. However, it comes with a higher peak current limitation level. The current sense scheme of PFC section in NCP1910 solves this problem. It provides a possibility to reduce the conduction losses on the current sense resistor and also keeps the same wanted peak current limitation level. The current source inside the CS pin maintains the CS pin at zero voltage. One can reduce the offset resistor (R17 + R20 in Figure 2) to reduce the maximum voltage drop and hence the power losses on current sense resistor (R12 // R13) depending on the acceptable noise immunity level. At the 90 V_{ac} input and 310 W application, 0.8 W on the sense resistor could be saved by changing the sense resistor from 0.1 Ω to 0.05 Ω, R17//R20 could be adjusted to keep the same current peak level. The most important is that the saving losses is free.

PFC light load efficiency has been improved with the frequency foldback of the NCP1910. When the power decreases below an externally fixed power value, the switching frequency decreases to 38 kHz typically.

The LLC cell of NCP1910 can operate to a frequency up to 500 kHz. To avoid any frequency runaway in light load conditions but also to improve the standby power consumption, the NCP1910B welcomes a skip input (Skip pin) which permanently observes the opto-coupler collector. If this pin senses a low voltage, it cuts the LLC output pulses until the collector goes up again. The NCP1910A does not offer the skip capability and routes the analog ground on pin 16 instead.

NCP1910 combines plenty of protection features for the robustness, which is detailed in datasheet. Together with these built-in handshakes and protections, the surrounding components are saved.

To maximize efficiency of the LLC power stage, Synchronous Rectification (SR) has been implemented on

the secondary side. The NCP4303A SR controller is used to achieve accurate turn-on and turn-off of the SR MOSFETs.

The standby power supply (5 V_{sb}) is requested to work alone without PFC operating, i.e. the PFC is off at remote off mode. A flyback converter driven by NCP1027 is chosen.

In summary, the architecture selected on this demo board allows system optimization so that the maximum efficiency is achieved without significantly increasing the component cost and circuit complexity.

DEMO BOARD SPECIFICATION

Description	Value	Unit
Input voltage Range	90 - 265	V _{rms}
Output Power	310	W
Minimum Output Load Current(s)	0	Adc
Number of Outputs	2	-
Nominal Output Voltage Output1: 12 V Output2: 5 V _{stby}	12 ±5% 5 ±5%	Vdc
Output Current Output1 (min/max) Output2 (min/max)	0/25 0/2	Adc
Maximum startup time	< 300	ms
Standby Power (NCP1910 disabled)	< 0.3	W
Efficiency (115 V _{rms} and 230 V _{rms}) 10% Load 20% load 50% load 100% load	80 88 92 88	%
Maximum Transient Output Power	150	W
Hold up time (50% of full load)	17	ms

Let's focus more on the design of NCP1910. An application note which details the design steps, equations and tips will be published later on. Before that, an Excel based worksheet for calculation of the surrounding components of NCP1910 is provided on the web site. The process is to fill in the needed information, such as the power supply specification, the wished brown out level, the minimum and maximum frequency of LLC converter etc. And then it is done.

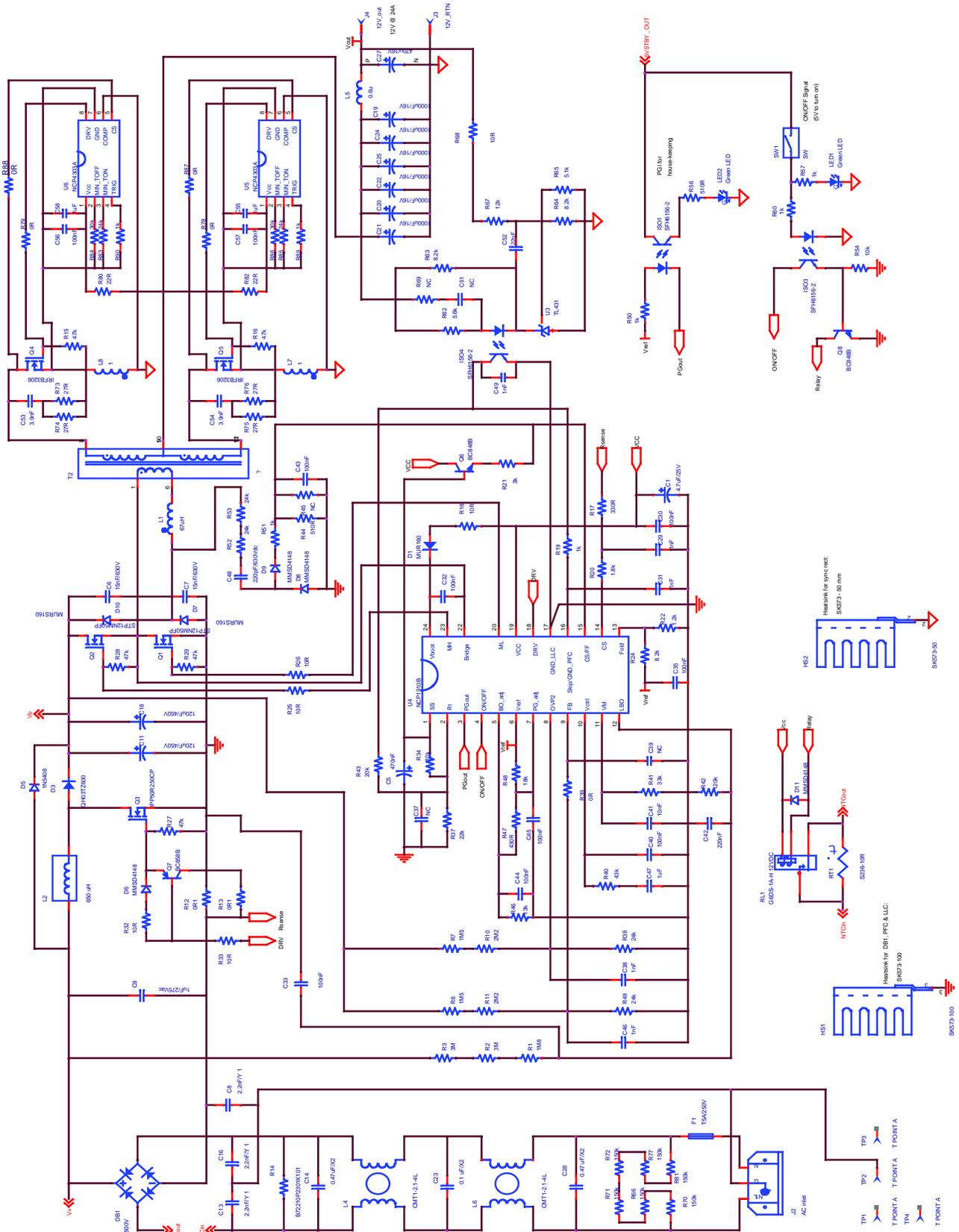


Figure 2. Main Application Schematic PFC and LLC

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Table 1. BILL OF MATERIAL

Qty	Ref	Part	Part Number	Manufacturer
11	C30, C32, C33, C35, C40, C43, C44, C45, C50, C56, C57	100 nF		
1	C34	2.2 nF		
1	C36	2.2 uF		
5	C37, C39, R45, C51, R69	NC		
1	C41	10 nF		
1	C42	220 nF		
3	C47, C55, C58	1 uF		
1	C48	220 pF / 630 Vdc		http://www.epcos.com
1	C52	22 nF		
2	C53, C54	3.9 nF		
1	DB1	GBU8J 8A 600 V		http://www.fairchildsemi.com/
1	D1	MUR160		http://www.onsemi.com
2	D2, D4	D1N4937		http://www.onsemi.com
1	D3	QH03TZ600		http://www.qspeed.com/
1	D5	1N5408		http://www.onsemi.com
4	D6, D8, D9, D11	MMSD4148		http://www.onsemi.com
2	D7, D10	MURS160		http://www.onsemi.com
1	D12	MBRD835L		http://www.onsemi.com
1	F1	T5A / 250V		
1	HS1	SK573-100	SK573-100	http://www.fischerelektronik.de
1	HS2	SK573-50	SK573-50	http://www.fischerelektronik.de
4	ISO1, ISO2, ISO3, ISO4	SFH6156-2		http://www.vishay.com/
1	J1	HEADER 2		
1	J2	AC inlet		
1	J3	12 V_RTN		
1	J4	12 V_out		
2	LED1, LED2	Green LED		
1	L1	67 uH	17462-LLC4	http://cmetransformateur.com/index.html
1	L2	650 uH	QP-3325V	http://www.yujingtech.com.tw/
1	L3	2.2 uH		
2	L4, L6	CMT1-2.1-4L	CMT1-2.1-4L	http://www.coilcraft.com
1	L5	0.6u		
2	L7, L8	1		
2	Q1, Q2	STP12NM50FP		http://www.st.com/
1	Q3	IPP50R250CP		http://www.infineon.com
2	Q4, Q5	IRFB3206		http://www.irf.com
2	Q6, Q8	BC848B		http://www.onsemi.com
1	Q7	BC858B		http://www.onsemi.com

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Table 1. BILL OF MATERIAL

Qty	Ref	Part	Part Number	Manufacturer
1	RL1	G6DS-1A-H 12 VDC	G6DS-1A-H 12VDC	http://www.omron.com/
1	RT1	S236-10R	S236	http://www.epcos.com
1	R1	1M8		
3	R2, R3, R4	3M		
1	R5	2M		
2	R6, R7	1M5		
1	R8	47R		
1	R9	150k		
2	R10, R11	2M2		
2	R12, R13	0R1	LVR03R1000FE12	http://www.vishay.com/
1	R14	B72210P2301K101	B72210	http://www.epcos.com
2	R15, R16	47k		
1	R17	330R		
6	R18, R25, R26, R32, R33, R68	10R		
9	R19, R23, R50, R51, R57, R58, R60, R89, R90	1k		
1	R20	1.8k		
1	R21	3k		
1	R22	1.2k		
3	R24, R63, R64	8.2k		
4	R27, R28, R29, R35	47k		
1	R30	78k		
1	R31	27k		
4	R34, R54, R55, R61	10k		
1	R36	560k		
1	R37	22k		
6	R38, R49, R52, R53, R83, R85	24k		
5	R39, R78, R79, R87, R88	0R		
1	R40	43k		
1	R41	33k		
1	R42	120k		
1	R43	36k		
1	R44	750R		
1	R46	13k		
1	R47	430R		
1	R48	18k		
1	R56	510R		
1	R59	100R		

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Table 1. BILL OF MATERIAL

Qty	Ref	Part	Part Number	Manufacturer
1	R62	5.6k		
1	R65	5.1k		
6	R66, R70, R71, R72, R77, R81	150k		
1	R67	12k		
4	R73, R74, R75, R76	27R		
2	R80, R82	22R		
2	R84, R86	30k		
1	SW1	SW		
4	TP1, TP2, TP3, TP4	T POINT A		
1	T1	17437B		http://cmetransformateur.com/index.html
1	T2	17459-LLC4		http://cmetransformateur.com/index.html
1	U1	NCP1027		http://www.onsemi.com
2	U2, U3	TL431		http://www.onsemi.com
1	U4	NCP1910B		http://www.onsemi.com
2	U5, U6	NCP4303A		http://www.onsemi.com

GENERAL BEHAVIOR

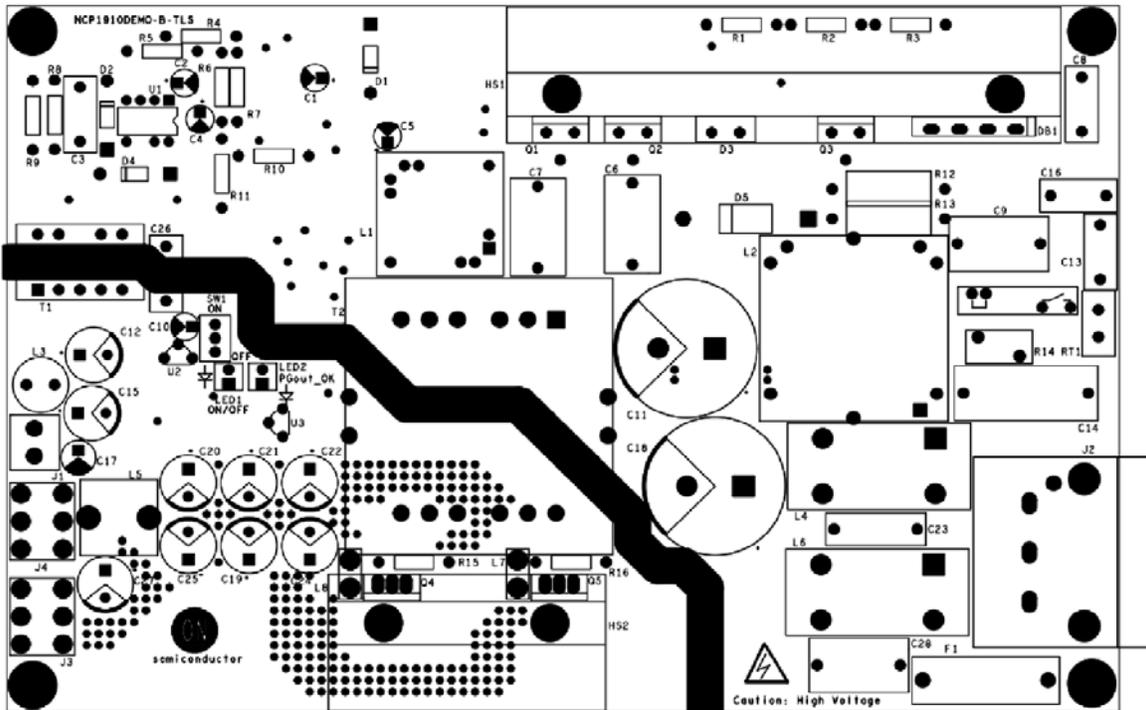


Figure 4. Component Placement (Component Side)

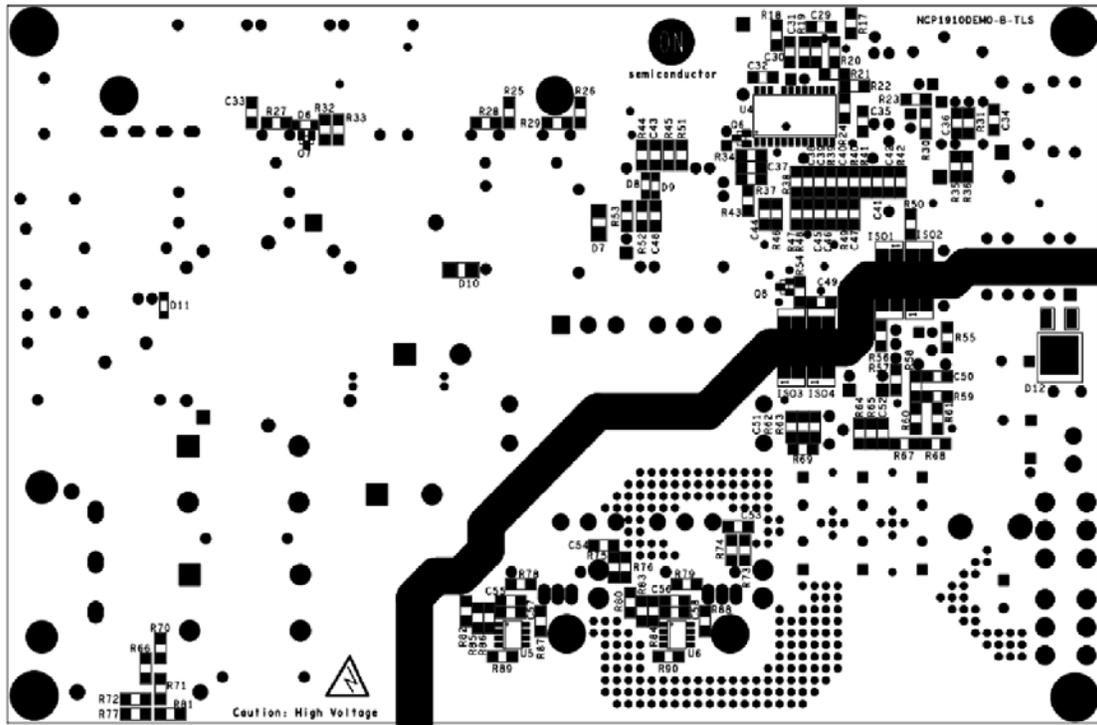


Figure 5. Component Placement (Solder Side)

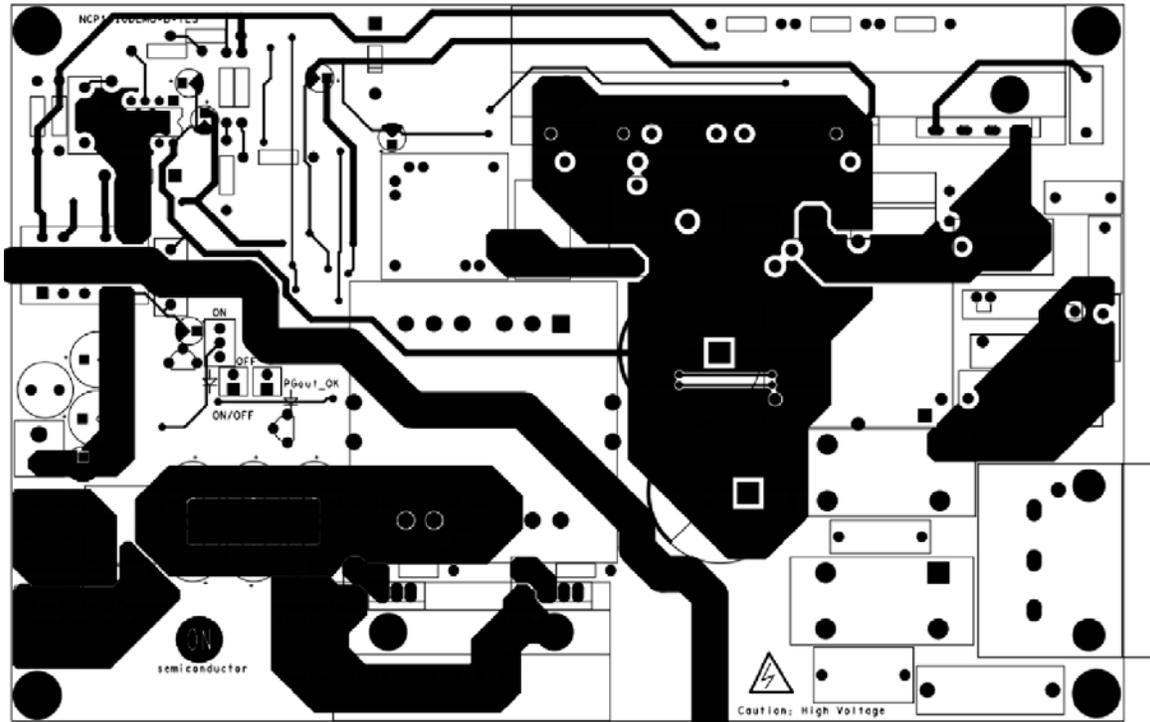


Figure 6. PCB Layout (Component Side)

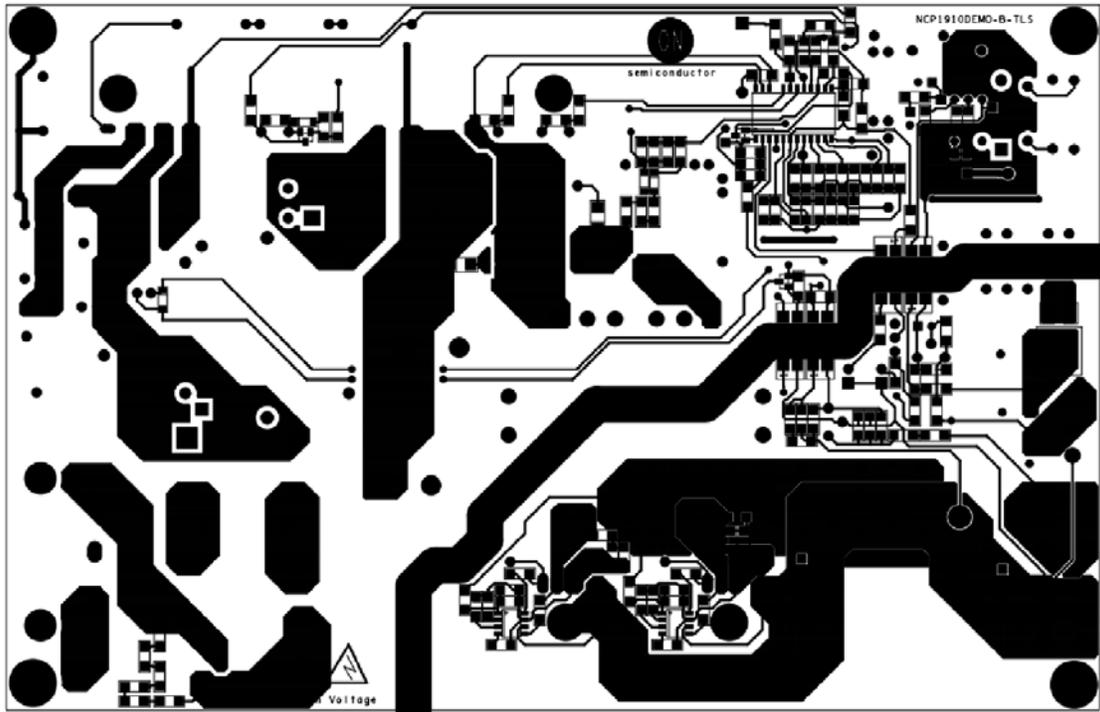


Figure 7. PCB Layout (Solder Side)

Efficiency results:

Figure 8 illustrates the efficiency of the demonstration board when the standby power supply is unloaded at different output loads and different input voltages. Also the Climate Savers Computing Initiative (CSC) Silver and Gold levels have been drawn for reference. The efficiency of the board should be above of the following Silver or Gold levels for the two inputs voltage: 115 V_{rms} and 130 V_{rms} . In order to validate the Gold level of the demonstration board, the input voltage has been lowered to 100 V_{rms} , even with this low input voltage the demo board still pass the Gold level.

Efficiency Measurements

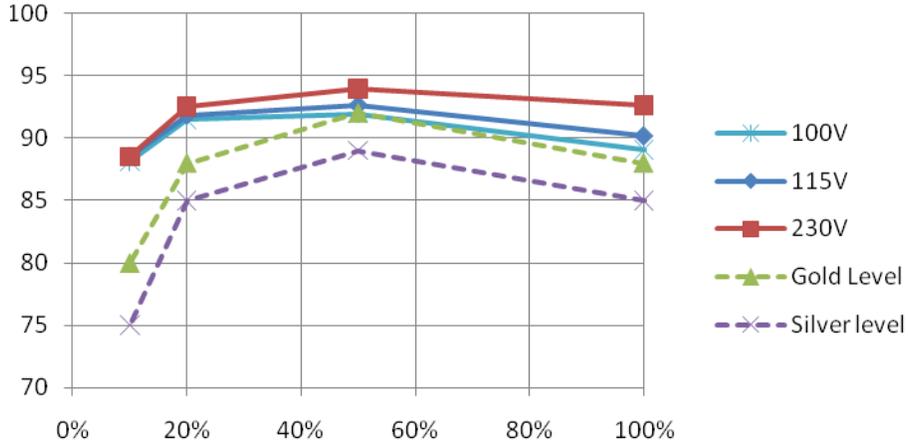


Figure 8. Efficiency vs. Output Power at Different Input Voltage

Power Factor Measurements

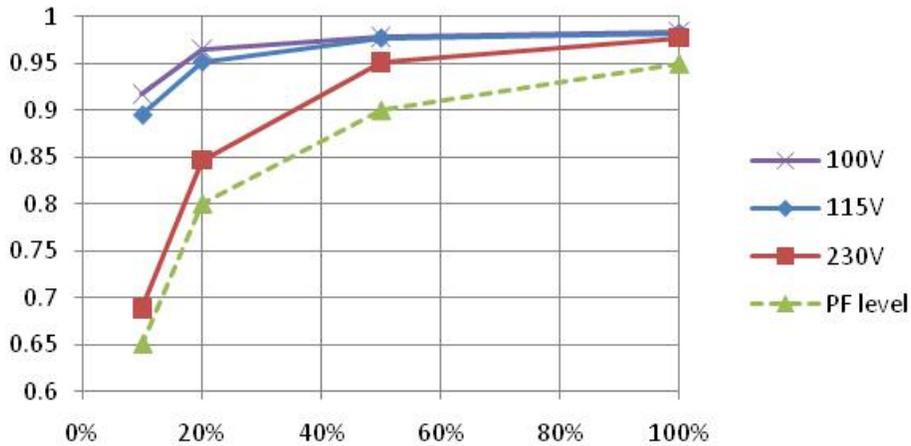


Figure 9. Power Factor vs. Output Power at Different Input Voltage

Typical Waveforms:

PFC section:

Input voltage and current waveforms

The following figures illustrate the input current and voltage delivered to the power supply (V_{ac} and I_{ac}) at different output loads (full load, 50% and 20% load) and two different input mains (115 V_{ac} and 230 V_{ac}).

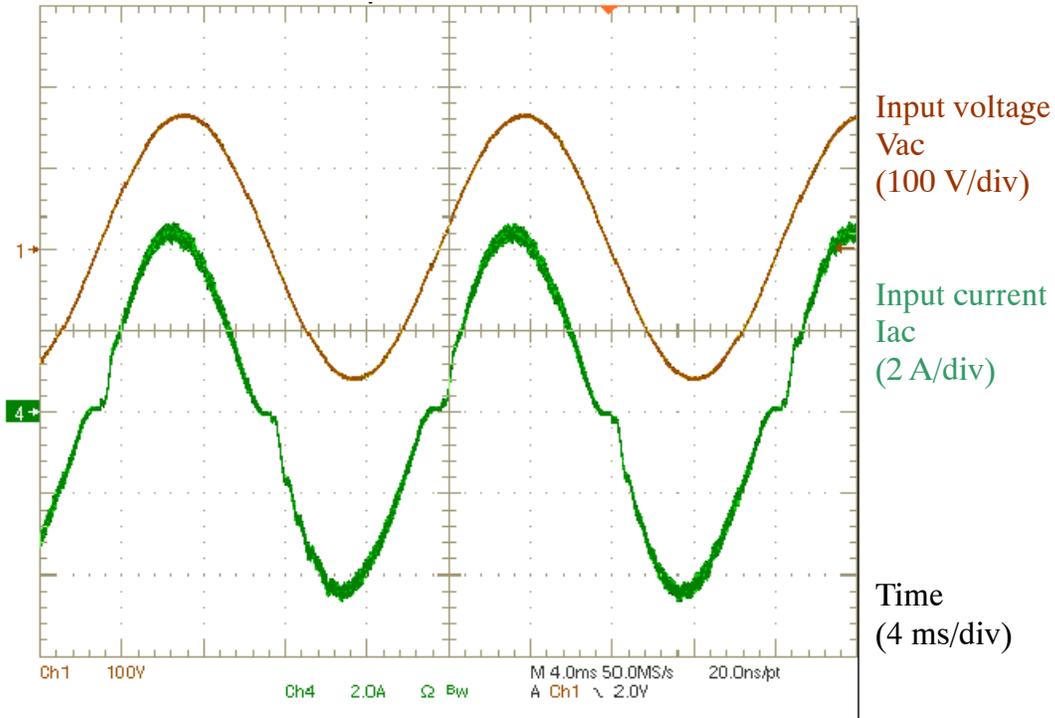


Figure 10. $V_{ac} = 115 V_{ac}$, $P_{in} = 332 W$, $V_{out} = 12 V$, $I_{out} = 25 A$, $PF = 0.982$, $THD = 9.96\%$

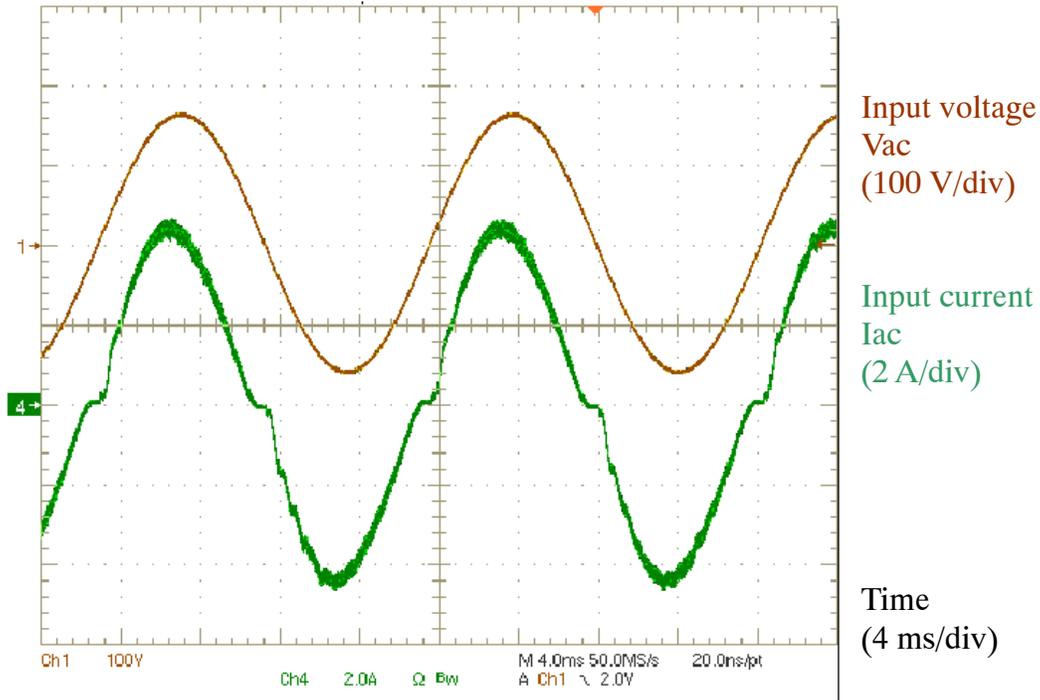


Figure 11. $V_{ac} = 115 V_{ac}$, $P_{in} = 163 W$, $V_{out} = 12 V$, $I_{out} = 12.5 A$, $PF = 0.978$, $THD = 11.59\%$

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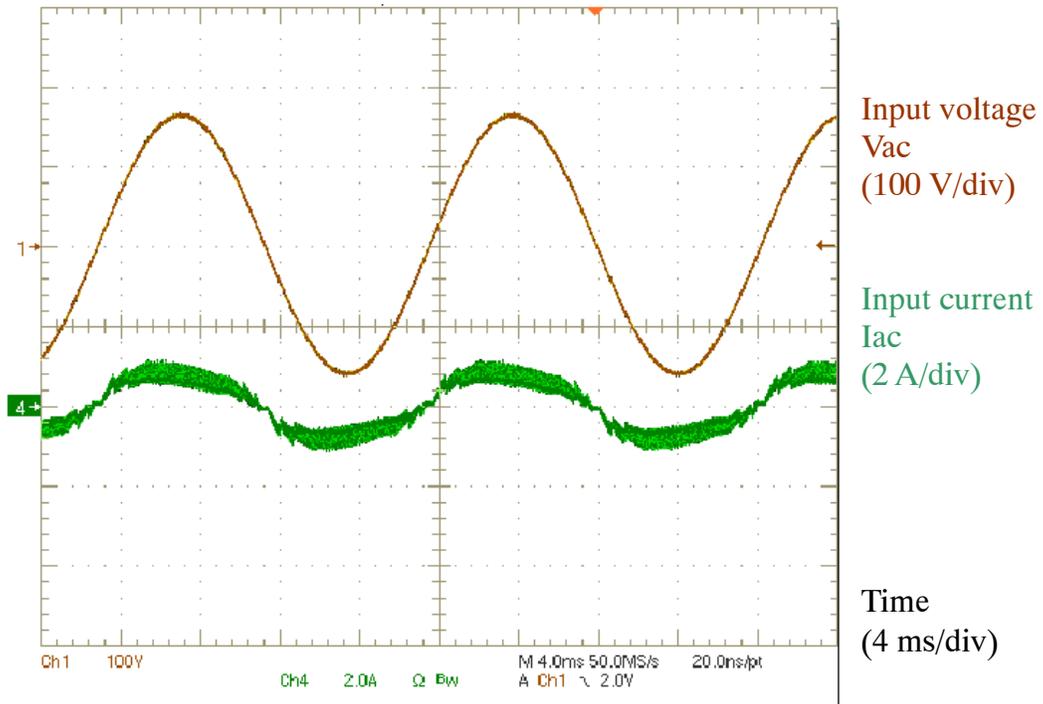


Figure 12. $V_{ac} = 115 \text{ Vac}$, $P_{in} = 65.5 \text{ W}$, $V_{out} = 12 \text{ V}$, $I_{out} = 5 \text{ A}$, $PF = 0.972$, $THD = 12.8\%$

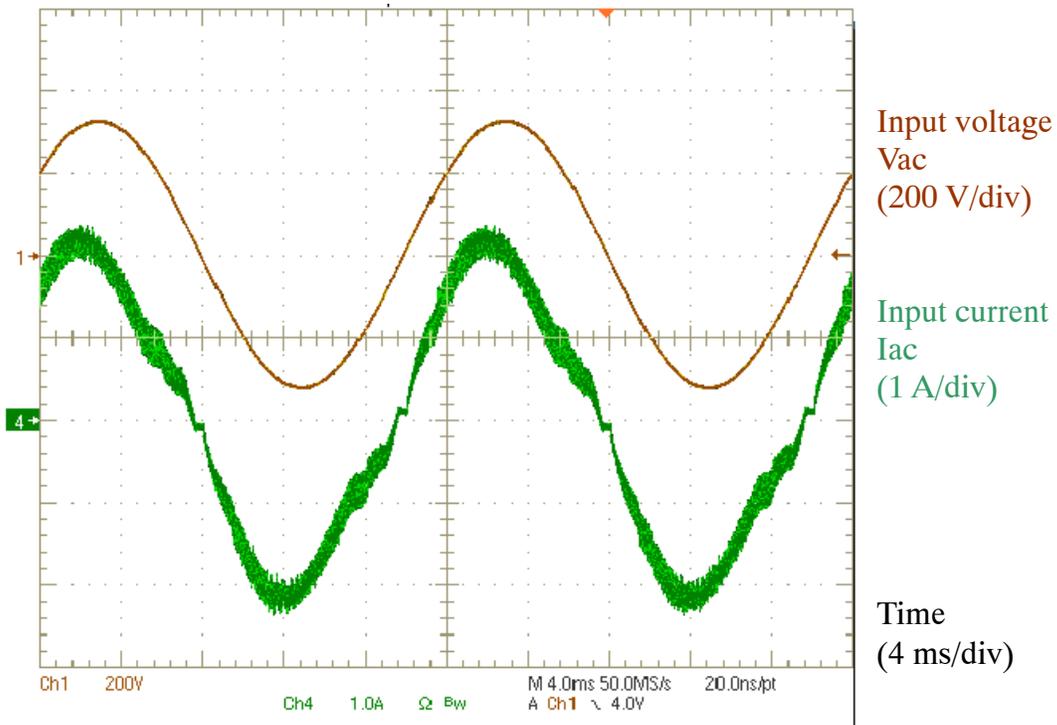


Figure 13. $V_{ac} = 230 \text{ Vac}$, $P_{in} = 324 \text{ W}$, $V_{out} = 12 \text{ V}$, $I_{out} = 25 \text{ A}$, $PF = 0.979$, $THD = 10.06\%$

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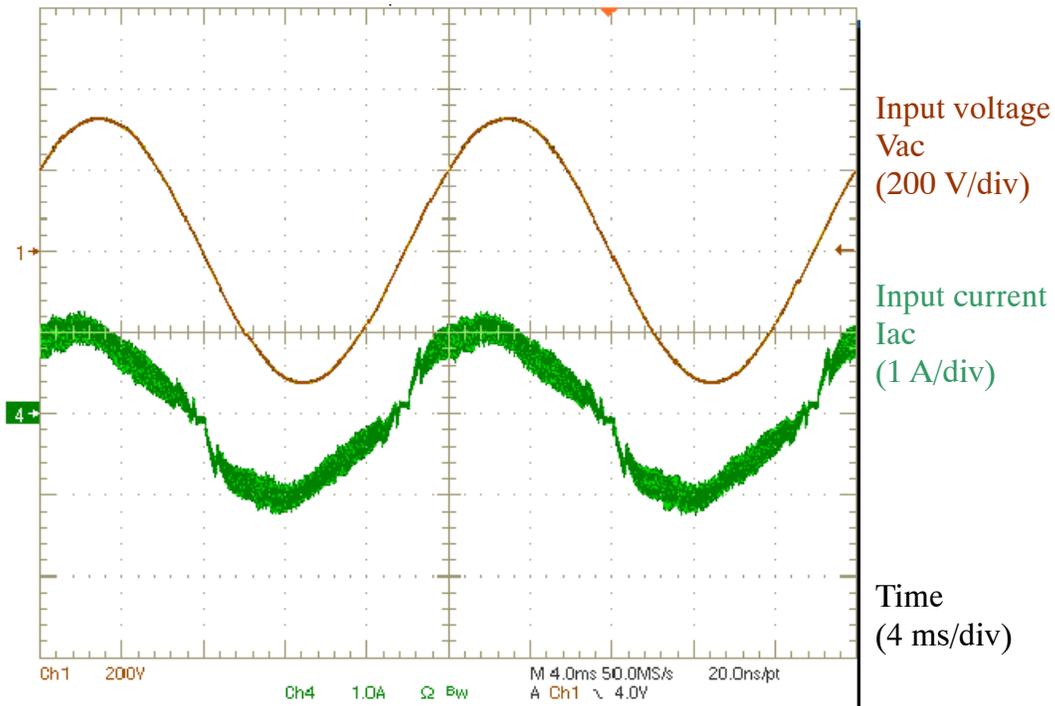


Figure 14. $V_{ac} = 230 \text{ Vac}$, $P_{in} = 160 \text{ W}$, $V_{out} = 12 \text{ V}$, $I_{out} = 12.5 \text{ A}$, $PF = 0.957$, $THD = 10.75\%$

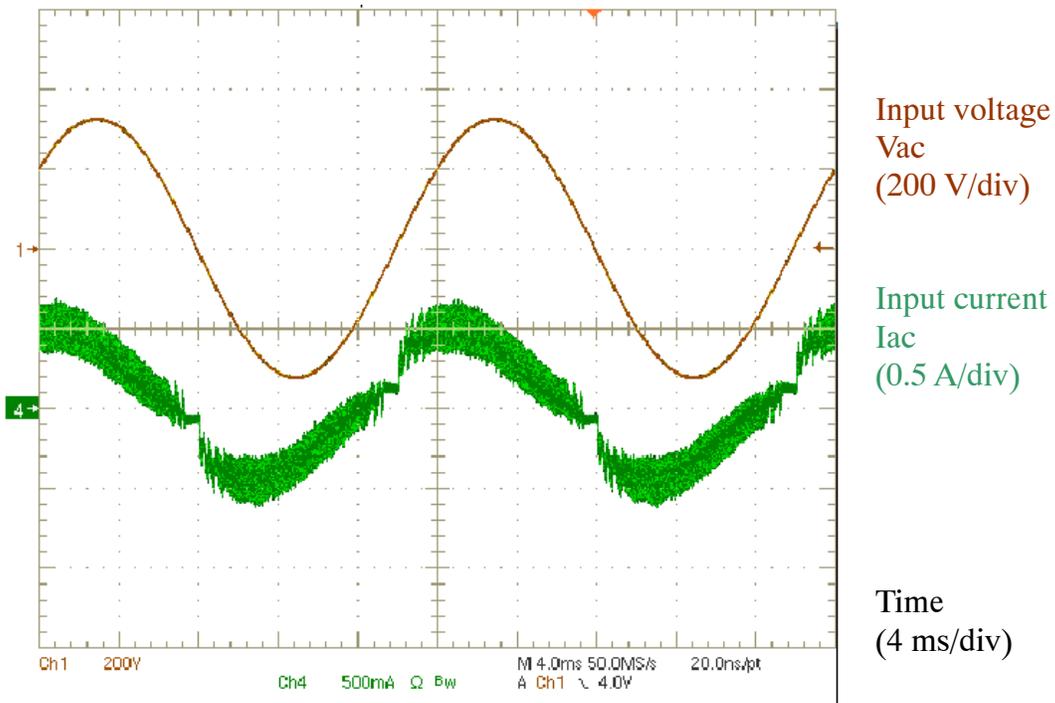


Figure 15. $V_{ac} = 230 \text{ Vac}$, $P_{in} = 64.9 \text{ W}$, $V_{out} = 12 \text{ V}$, $I_{out} = 5 \text{ A}$, $PF = 0.858$, $THD = 14.45\%$

Soft-Start

The two following curves illustrate the PFC's soft-start at 115 V_{ac} and 230 V_{ac} input line voltage.

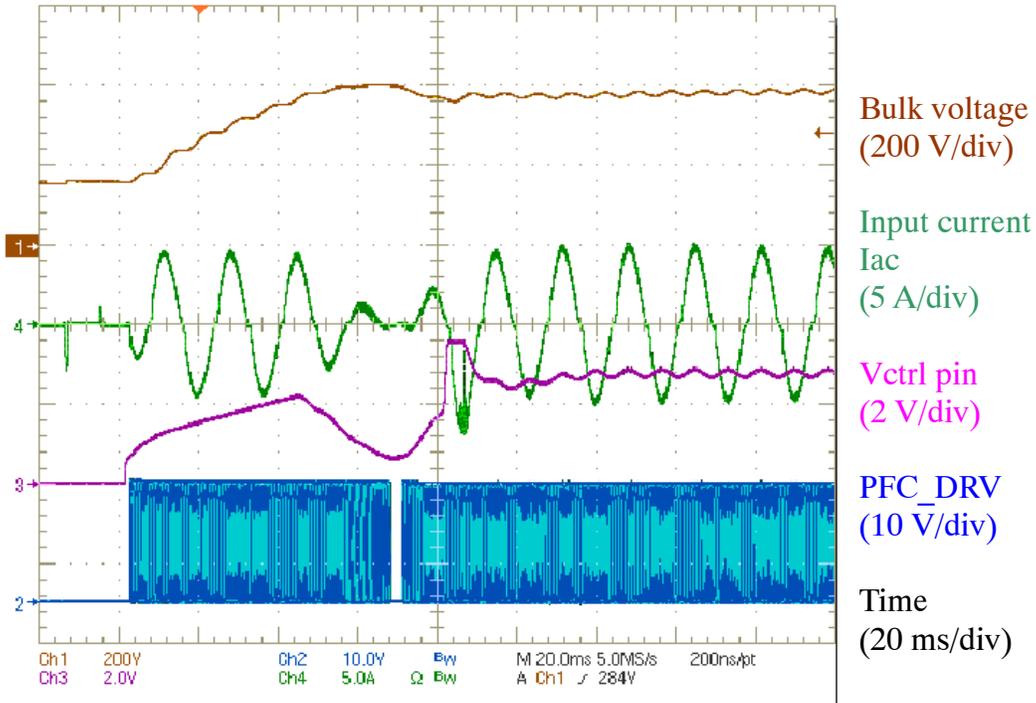


Figure 16. Soft-Start @ 115 V & I_{out} = 25 A

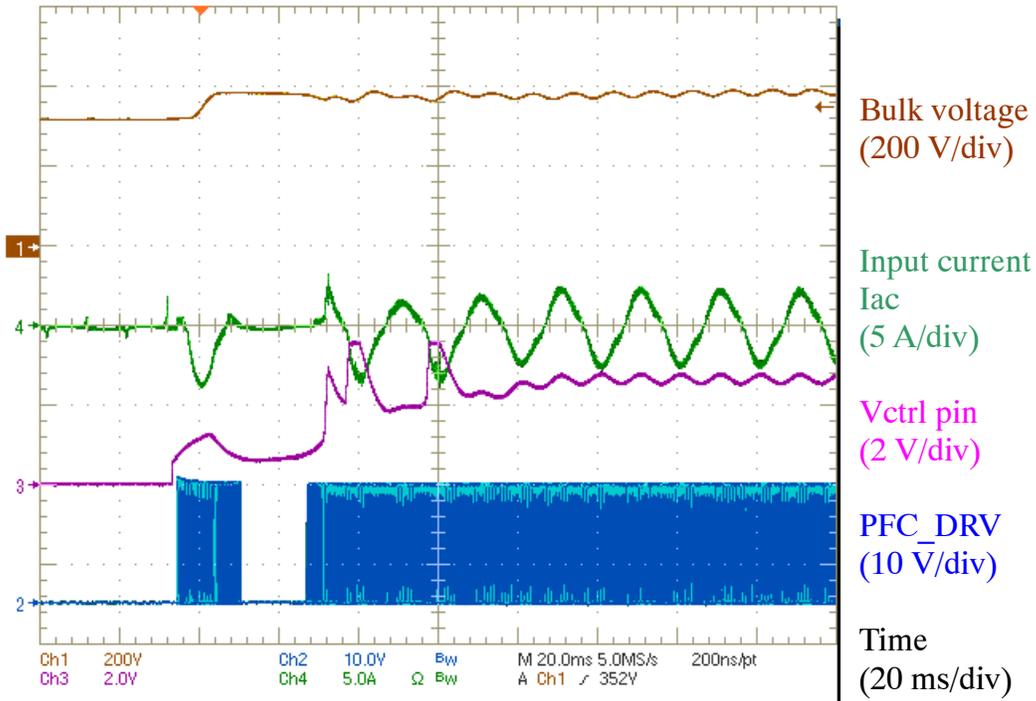


Figure 17. Soft-Start @ 230 V & I_{out} = 25 A.

Line Brown Out Test:

Input line voltage has been increased then decreased in order to test the brown out level. Figure 18 illustrates the start-up and shut down of the power supply when the input line voltage is varying from 60 V_{ac} to 115 V_{ac} and respectively from 115 V_{ac} to 60 V_{ac}.

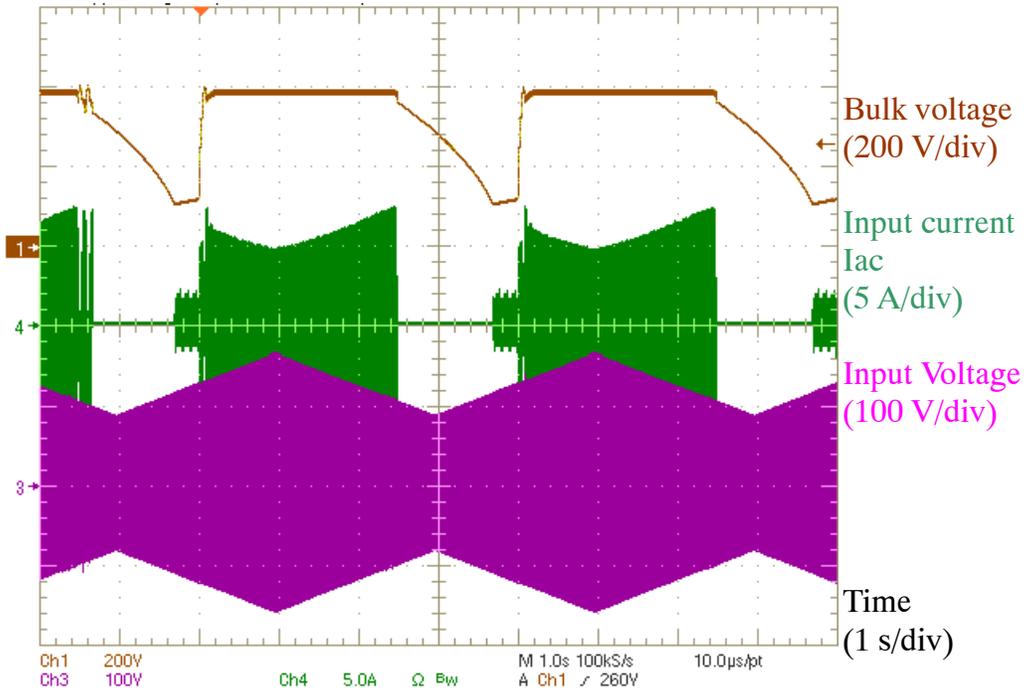


Figure 18. Line Brown Out Test

As depicted by the following figure, a zoom-in of the previous figure allows to measure accurately the bulk on level of the brown-out.

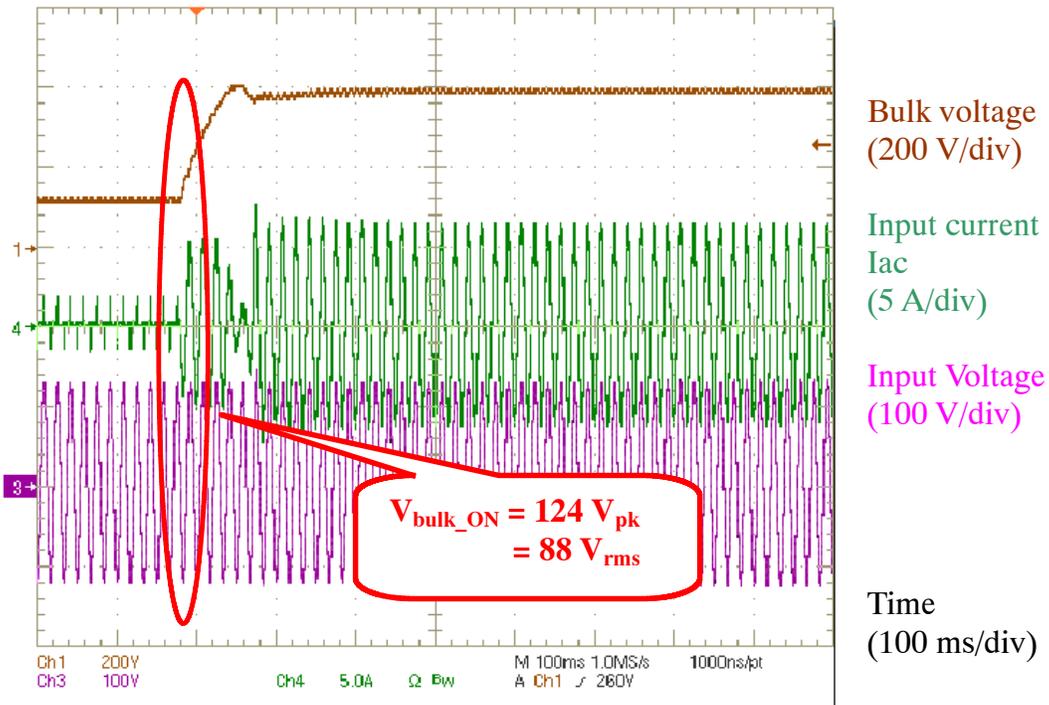


Figure 19. Line Brown Out Test: $V_{\text{bulk_ON}}$

Here after is a zoom-in on the shut down when the bulk off level is reached.

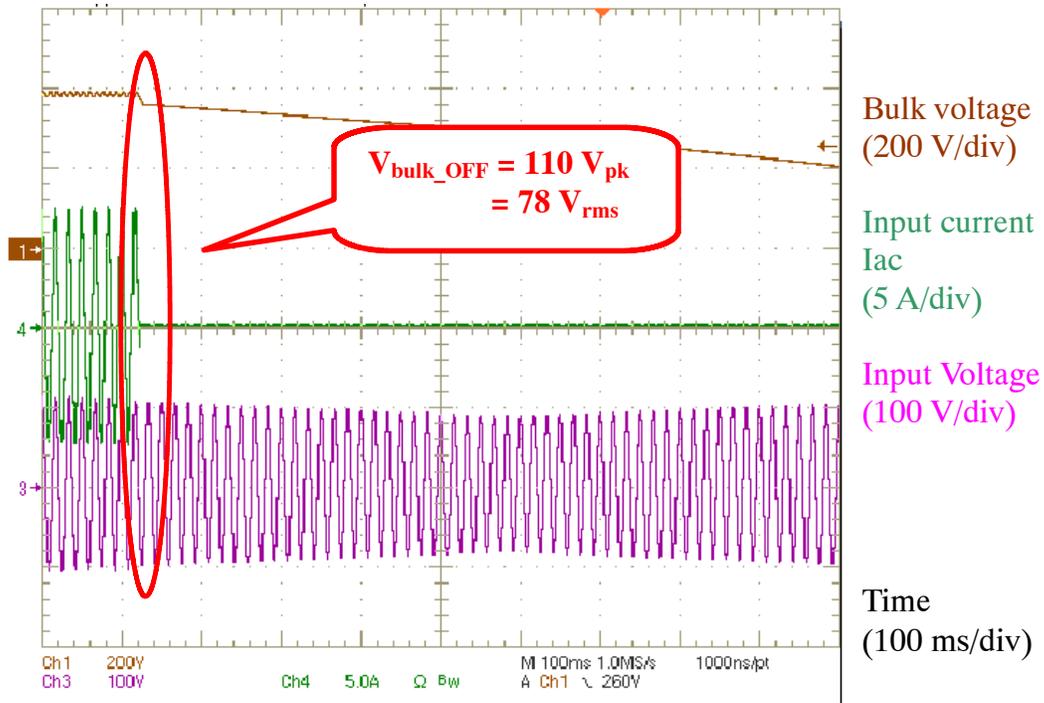


Figure 20. Line Brown Out Test: $V_{\text{bulk_OFF}}$

Figure 21 illustrates a 50% line sag @ 230 V_{ac} , there is no disruption on 12 V output. The output drops only by 5.3% (640 mV).

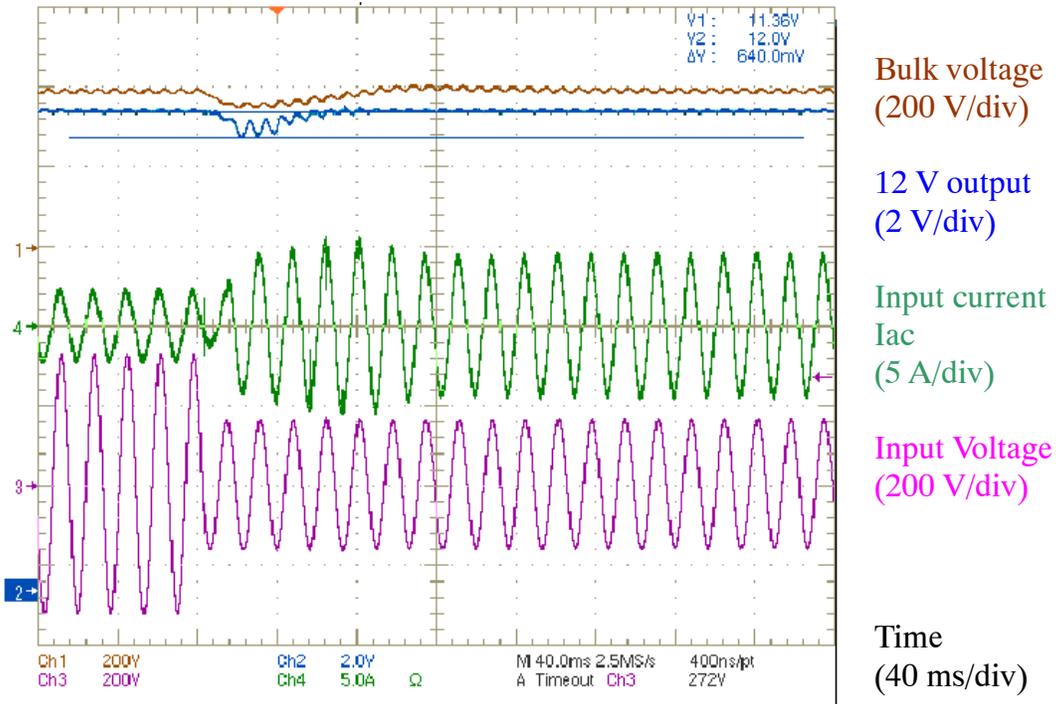


Figure 21. Input Voltage Changing from 230 Vac to 115 Vac

Transient Load

The following figures illustrate the power supply stability when a step load output of 50% is applied. The step load has been applied with the following conditions:

- $V_{ac} = 115 V_{ac}$ @ 60 Hz.
- Step load from 12.5 A to 25 A, with a 1 A/μs slope and 2 ms period.

Figure 22 shows a step load response of ±435 mV, or ±3.6% of the 12 V output voltage.

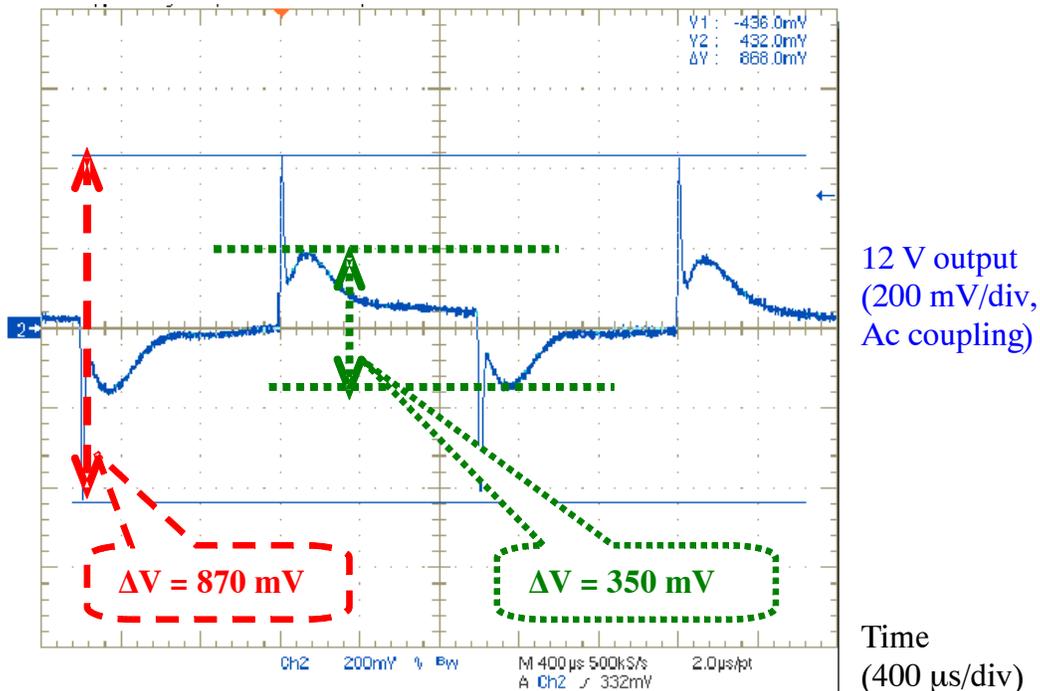


Figure 22. Step Load Response Between 50% & 100%

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Output step load response illustrated with Figure 22 shows the step load response due to the closed loop regulation of the LLC added by spike due to the LC output switching filter. If L_5 from the output filter is shorted, in that case the spike when the step load is applied disappears: Figure 23 illustrates the step load response of the LLC converter itself.

However as the LC output switching frequency filter is now shorted the ripple noise due to the LLC switching frequency is bigger than the one in Figure 22.

Moreover a short calculation shows that the drop at the beginning of step load is mainly due to L_5 .

The voltage drop across L_5 can be expressed as follow (the drop due to its ESR is not taken into account in this calculation):

$$V_{L_5} = L_5 \frac{\Delta I}{\Delta t} \quad (\text{eq. 1})$$

Where: $L_5 = 0.6 \mu\text{H}$, $\Delta I = 12.5 \text{ A}$, $\Delta t = 12.5 \mu\text{s}$ (slope of step load 1 A/ μs)

$$V_{L_5} = 0.6 \mu \frac{12.5}{12.5 \mu} = 0.6 \text{ V} \quad (\text{eq. 2})$$

The difference between the drop measured and the drop calculated can be explained as follow:

The step load is partially filtered by the output capacitor of the LC, thus the slope and ΔI can be a little bit smaller compare to the calculation.

As $L_5 = 0.6 \mu\text{H}$ with $\pm 20\%$ $\rightarrow L_5 - 20\% = 0.48 \mu\text{H}$, the new drop will be 480 mV, thus L_5 should be probably closer to its minimum value than its typical value.

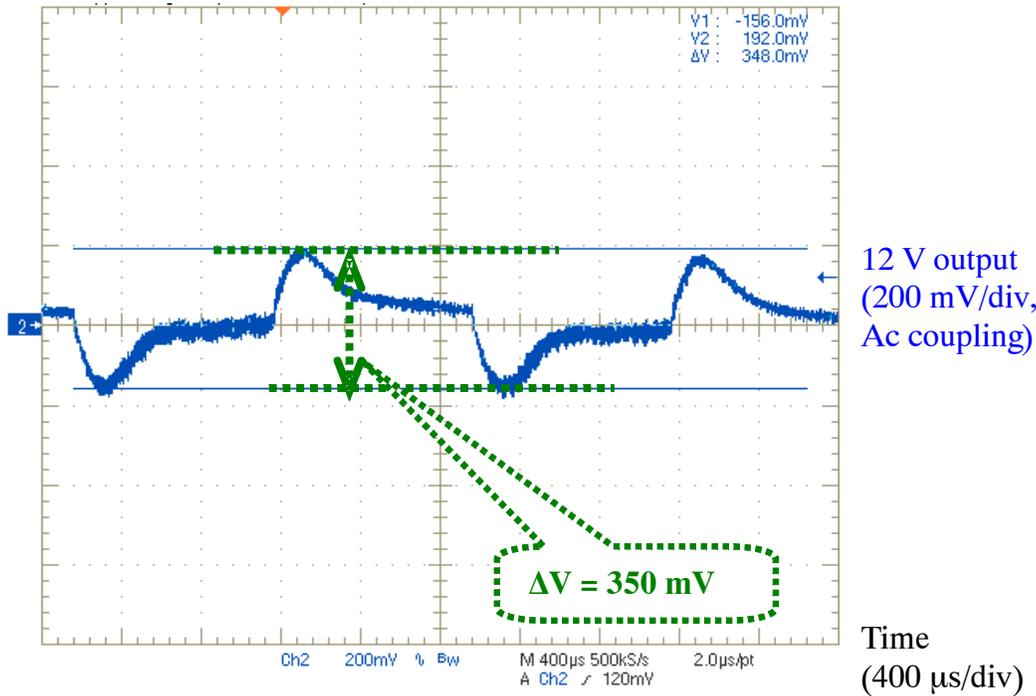


Figure 23. Step Load Response Between 50% & 100%, when L_5 is Shorted

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