AND9077/D

NCP1611/NCP1612 Tips and Tricks

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APPLICATION NOTE

Introduction

The NCP1611 and the NCP1612 are designed to feature most functions required when designing a PFC stage. However, designers often have unique specifications and needs to address, that may require the addition of specific circuitries around the controller. This application note addresses typical questions that can be raised when developing a power supply. The following topics are covered:

1. I do not need the brown-out function
2. I want to increase the brown-out hysteresis
3. I want to inhibit the skip function
4. I need premium PF and THD performance
5. I face burst operation when the line voltage is low or at the border between the low and high line ranges

The solutions given in this paper are generally illustrated by NCP1611-based schematics. However, they can be re-used in the NCP1612 applications.

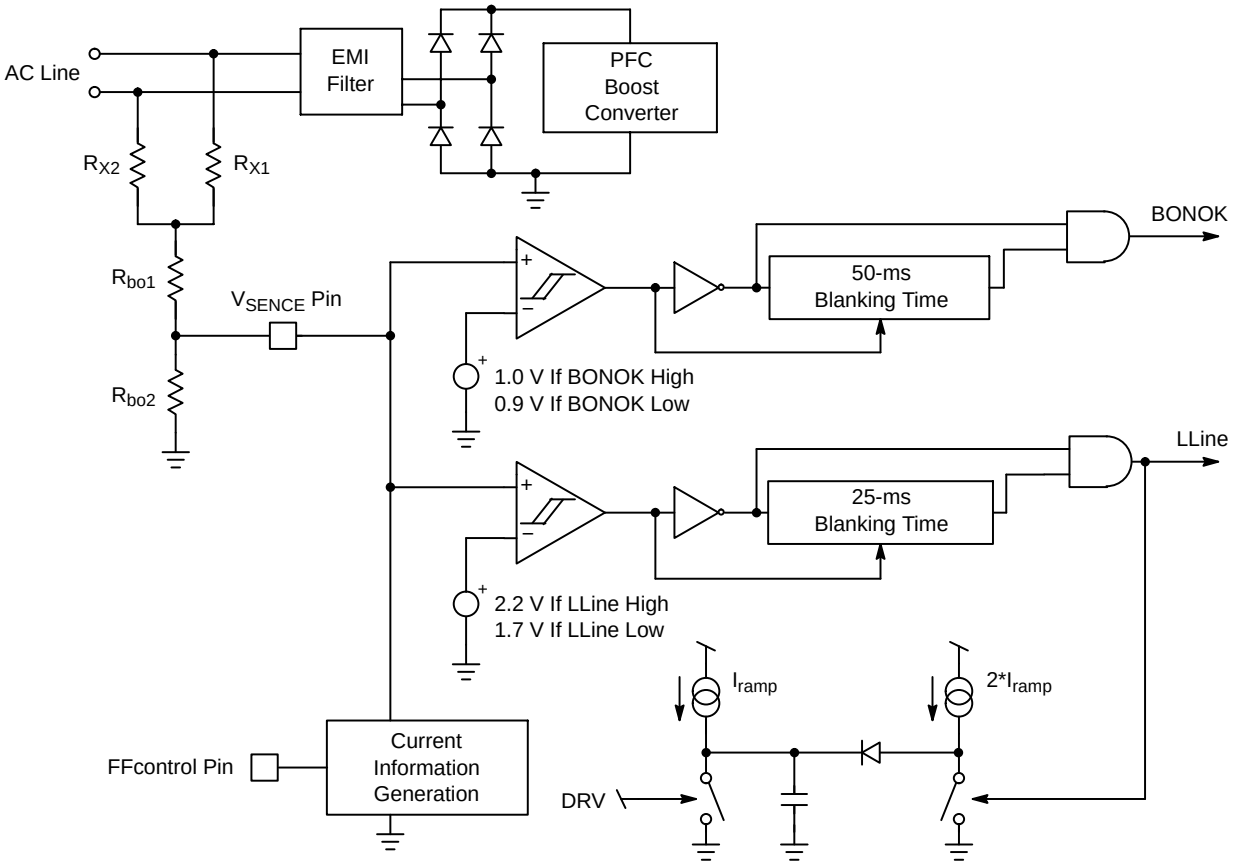


Figure 1. Brown-Out and Line Range Detection Block

I DO NOT NEED THE BROWN-OUT FUNCTION

The NCP1611 and NCP1612 are designed to detect low ac line conditions and stops operation thus protecting the PFC stage from excessive stress.

To do so, the V_{SENSE} pin must receive a portion of the instantaneous input voltage (V_{in}). As V_{in} is a rectified sinusoid, the monitored signal normally varies between zero (or a small voltage) and a peak value.

Hence, the input voltage can easily be detected as sufficient when it exceeds a preset level. In contrast, the rectified sinusoidal nature of the input voltage leads it to be low or very low part of the line cycle. The line voltage magnitude is then considered as too low if it cannot exceed a preset level for a time longer than a line cycle.

Practically:

- The V_{SENSE} pin voltage that receives a portion of the input voltage is compared to a 1 V reference.
- If V_{SENSE} exceeds 1 V, the input voltage is considered sufficient and the PFC stage can enter operation.
- If V_{SENSE} remains below 0.9 V for 50 ms, the circuit detects a brown-out situation (100 mV hysteresis) and the PFC stage stops operating. Taking into account tolerance, the 50 ms delay has a minimum value of 35 ms that prevents the PFC stage from stopping operating in the case of a 20 ms mains interruption which, thus, helps pass usual hold-up time specifications.

Similarly, the NCP1611 and NCP1612 detect the line range for feed-forward. By default, the circuit operates the “low-line gain” mode. In this state, the on-time is limited to 25 μs (typically). If V_{SENSE} exceeds 2.2 V, the circuit detects a high-line condition and both the loop gain and the maximum on-time are reduced by a ratio of 3 ($t_{on,max} \cong$ 8.3 μs, typically). Figure 1 sketches the corresponding circuitry.

One simple way to inhibit the brown-out function consists of applying a V_{CC} portion to the V_{SENSE} pin. This option is sketched in Figure 2 for the NCP1611. The same can be used for the NCP1612. Considering that the maximum possible value of the 1 V brown-out reference voltage is 1.04 V, resistors R_{sense1} and R_{sense2} must be selected so that:

$$\left(\frac{R_{sense2}}{R_{sense1} + R_{sense2}} \cdot V_{CC} \geq 1.04 \right) \qquad \text{(eq. 1)}$$

Two other constraints may have to be taken into account:

- These resistors load the V_{CC} rail. The extra consumption it costs, must be minimized if start-up resistors are used to charge the V_{CC} capacitor at start-up. In this case, use high-impedance to reduce their impact. (R_{sense1} + R_{sense2}) in the range of 500 kΩ or higher generally give good results.
- The voltage applied to V_{SENSE} must not exceed 2.2 V upper threshold for line range detection (2.1 V min.) if the PFC stage needs a maximum on-time higher than 8.3 μs.

Finally the above requirements for resistors R_{sense1} and R_{sense2} can be summarized as follows:

$$R_{sense1} + R_{sense2} \geq 500\ k\Omega$$

$$1.04 \leq \frac{R_{sense2} \cdot V_{CC}}{R_{sense1} + R_{sense2}} \leq 2.10 \qquad \text{(eq. 2)}$$

For instance, if V_{CC} varies between 10 V and 18 V, we can for instance use:

$$R_{sense2} = 56\ k\Omega$$
$$R_{sense1} = 470\ k\Omega \qquad \text{(eq. 3)}$$

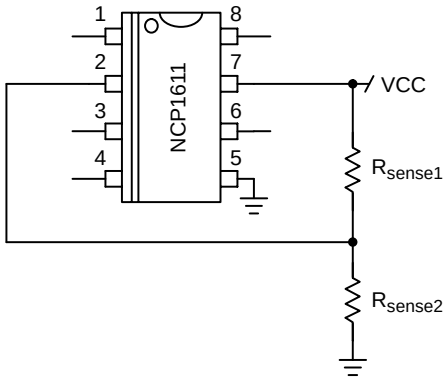


Figure 2. Inhibiting the Brown-out Function

In applications where a 8.3-μs maximum on-time is sufficient, select R_{sense1} and R_{sense2} of Figure 2 so that more than 2.3 V is applied to the V_{sense} pin. Doing so, the circuit will enter the high-line mode and hence, limit the maximum on-time to 8.3 μs typically. **Keep V_{sense} below 4.5 V anyway since the maximum V_{sense} voltage that is recommended for optimal operation is 4.5 V.**

I WANT TO INCREASE THE BROWN-OUT HYSTERESIS

As aforementioned in section 1 (*I do not need the brown-out function*), the brown-out comparator has a 100 mV hysteresis which represents 10% of the upper level. The PFC stage is hence supposed to detect a brown-out situation when the line amplitude is 90% of the level necessary to start operation. This 10% hysteresis is generally far sufficient to address the small drop that the PFC operation can produce on the measured line voltage (sag due to the input current within the cable and EMI filter resistive components) when entering into operation.

If not, the hysteresis can be easily increased by offsetting the V_{SENSE} pin voltage when the circuit is in operation. In fact, pulling up the V_{SENSE} pin voltage by V_{OFFSET} amounts to a decrease of the brown-out fault detection threshold from 0.9 V down to (0.9 V − V_{OFFSET}). The DRV signal is low in high state when the circuit is off and only happens to be high when the controller is active. It then seems the right signal to use to generate this offset. Figure 3 portrays three ways to do it.

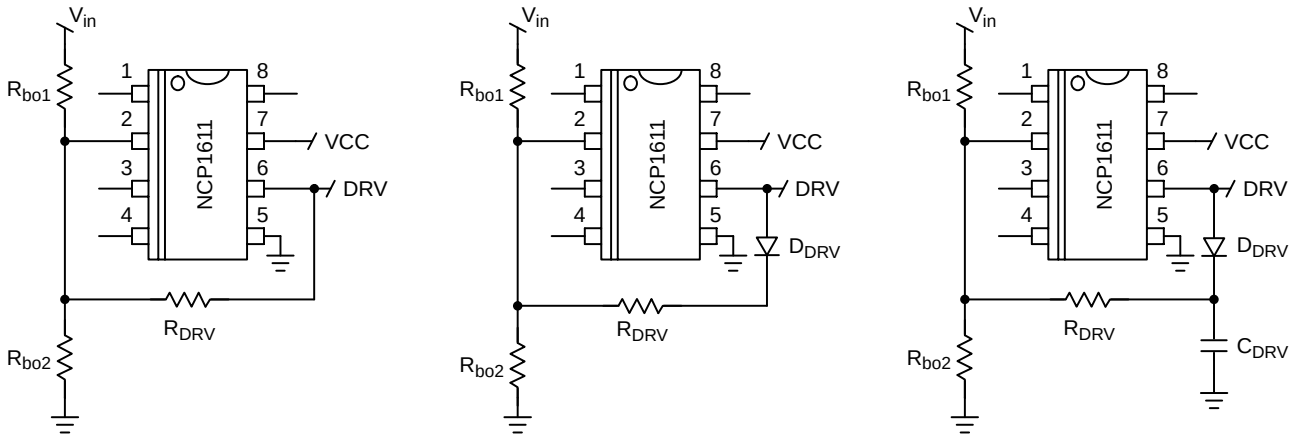


Figure 3. Increasing the Brown-out Hysteresis

In Figure 3a, a simple resistor is inserted between the DRV and V_{SENSE} pins. It is assumed here that (R_{DRV} >> $R_{bo1} \parallel R_{bo2}$) so that when the DRV pin is in low state, the portion of the line voltage applied to the V_{SENSE} pin is not significantly impacted by R_{DRV}. Hence, the minimum line voltage allowing the PFC stage to enter operation is not affected by R_{DRV}. When this is not the case, the option of Figure 3a should be preferred where the diode prevents the DRV from interfering when in low state. The line voltage to enter operation is hence not affected by the tweak.

Options a) and b) rely on the fact that forcing the V_{SENSE} pin above 1 V once every line cycle is enough not to detect a brown-out situation (the 50 ms blanking time timer of being reset during this event). That is why the pulsing nature of the V_{OFFSET} offset is acceptable. However, filtering capacitors are generally placed on the V_{SENSE} pin that can drastically mitigate V_{OFFSET} particularly in the case of short DRV pulses. In this case, option c is to be preferred where DRV pulses are rectified to form a dc voltage across capacitor C_{DRV}.

In the three cases, neglecting the voltage drop across D_{DRV}, V_{OFFSET} is approximately given by:

$$V_{OFFSET} = \frac{R_{bo1} \parallel R_{bo2}}{R_{DRV} + R_{bo1} \parallel R_{bo2}} \cdot V_{DRV} \qquad \textit{(eq. 4)}$$

Where V_{DRV} is the DRV pin voltage in high-state that is V_{CC} or $V_{DRV(high)}$ if V_{CC} is higher than $V_{DRV(high)}$. $V_{DRV(high)}$ is the DRV voltage clamp.

In general, R_{bo1} is very large compared to R_{bo2} and Equation 4 can be simplified as follows:

$$V_{OFFSET} \cong \frac{R_{bo2}}{R_{DRV} + R_{bo2}} \cdot V_{DRV} \qquad \textit{(eq. 5)}$$

For instance, if V_{DRV} is 12 V ($V_{DRV(high)}$), R_{bo2} is 120 kΩ and R_{DRV} is 10 MΩ, we have:

$$V_{OFFSET} \cong \frac{120\ k}{10000\ k + 120\ k} \cdot 12 \cong 0.14\ V \quad \textit{(eq. 6)}$$

The brown-out lower threshold is then changed from 0.90 V down to 0.76 V.

I WANT TO INHIBIT THE SKIP FUNCTION

The NCP1611 and NCP1612 feature a FFcontrol pin that sources a current proportional to the (rectified) line current. When as recommended, a resistor connects the pin to ground, the FFcontrol pin voltage is a rectified sinusoid in phase with the input voltage. The PFC stage stops operating whenever the FFcontrol pin voltage goes below 0.65 V and keeps on skipping cycles until this voltage exceeds 0.75 V. This prevents the PFC stage from operating near the line zero crossing where the power transfer is particularly inefficient. The efficiency is hence improved (particularly at light load) but on the other hand, the skip function does result in a slightly increased distortion of the current. If superior power factor is required, the FFcontrol pin should be prevented from dropping below 0.65 V to inhibit the skip function. To have a good margin (taking account the skip threshold tolerance), we would recommend to force a 0.8 V minimum voltage on the FFcontrol pin.

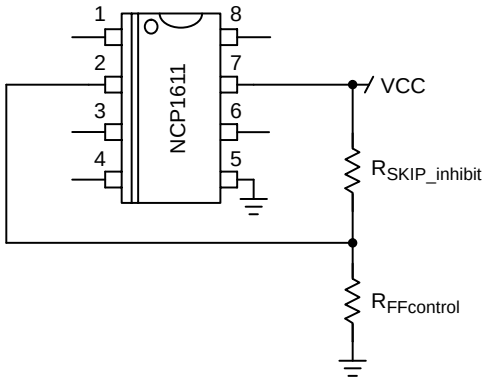


Figure 4. Inhibiting the Skip Mode Function

As shown in Figure 4, the inhibition can be made by adding a resistor $R_{SKIP-inhibit}$ between the V_{CC} rail and the FFcontrol pin, $R_{SKIP-inhibit}$ being the normal resistor placed to adjust the current controlled frequency foldback characteristic.

With this arrangement, the FFcontrol pin voltage becomes:

$$V_{FFcontrol} = \left(\left(R_{FFcontrol} \parallel R_{skip-inhibit}\right) \cdot I_{FFcontrol}\right) + \left(\frac{R_{FFcontrol} \cdot V_{CC}}{R_{FFcontrol} + R_{skip-inhibit}}\right) \quad \text{(eq. 7)}$$

Hence, the minimum FFcontrol pin voltage is:

$$\left(\frac{R_{FFcontrol} \cdot V_{CC}}{R_{FFcontrol} + R_{skip-inhibit}}\right)$$

and we need to force:

$$\frac{R_{FFcontrol} \cdot V_{CC}}{R_{FFcontrol} + R_{SKIP-inhibit}} = 0.8\ V$$

If the nominal V_{CC} voltage is 16 V:

$$\frac{R_{FFcontrol} \cdot 16}{R_{FFcontrol} + R_{skip-inhibit}} = 0.8\ V \quad \text{(eq. 8)}$$

$$\Rightarrow \frac{R_{FFcontrol}}{R_{FFcontrol} + R_{SKIP-inhibit}} = \frac{0.8}{16} = 0.05$$

As shown by the above example, the required ratio being small, $R_{SKIP-inhibit}$ is large compared to $R_{FFcontrol}$. The FFcontrol pin voltage expression can then simplify as follows:

$$V_{FFcontrol} \cong \left(R_{FFcontrol} \cdot I_{FFcontrol}\right) + \left(\frac{R_{FFcontrol}}{R_{SKIP-inhibit}} \cdot V_{CC}\right) \quad \text{(eq. 9)}$$

Hence, the FFcontrol pin voltage is offset by 0.8 V which slightly changes the CCFF characteristic. This modification is generally acceptable. If not, another option is shown in Figure 8 where the FFcontrol pin voltage is unchanged when it is higher than 0.8 V and clamped otherwise. To do so, a 1.5 V voltage is created from V_{CC} (($R_{SKIP-inhibit2} \times V_{CC}$)/($R_{SKIP-inhibit1} + R_{SKIP-inhibit2}$)) and applied through a diode so that about a (1.50 V − 0.65 V) minimum voltage is applied to the FFcontrol pin. Please note that the impedance of ($R_{SKIP-inhibit1}$//$R_{SKIP-inhibit2}$) must be small compared to $R_{FFcontrol}$. Otherwise, the voltage generated at the diode anode would be affected by $R_{FFcontrol}$.

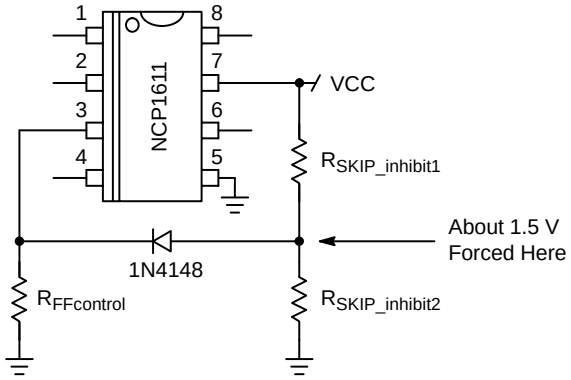


Figure 5. FFcontrol Pin Voltage being Prevented from Dropping below 0.8 V

I NEED PREMIUM PF AND THD PERFORMANCE

The NCP1611 and NCP1612 are designed to yield excellent performance in term of THD and PF. The reduction of the frequency together with a circuitry that compensates the dead-times for proper current shaping in low frequency mode (Note 1) even help improve the light load performance when compared to traditional Critical conduction mode (CrM) solutions.

Still applications exist where extremely challenging PF and THD performance are requested. In this case, you may have to further improve the operation. This section deals with possible options and aspects to check. This is not exhaustive.

Reduce the $V_{CONTROL}$ Ripple

PFC stages absorb a sinusoidal current from a sinusoidal line voltage. Hence, these converters provide the load with a squared sinusoid power that matches the demand in average only. Despite the bulk capacitor buffer role, this leads the output voltage to exhibit a low-frequency ripple (e.g. 120 Hz in USA) that must not be taken into account by the regulation loop since the error amplifier output voltage must keep as constant as possible for a proper current shaping.

That is why the regulation bandwidth must be set as low as possible to limit this ripple. You can refer to the design tool available on the web to optimally adjust the loop (refer to [1] or [2]).

Please note that the NCP1611 and the NCP1612 feature the dynamic response enhancer (Note 2) as well as an accurate and soft over-voltage protection that drastically limit possible deviations of the bulk voltage from the regulation point in case of a sharp load or line change.

This ripple impact actually depends on its relative magnitude with respect to the $V_{CONTROL}$ dc value. $((\Delta V_{CONTROL})/(V_{CONTROL,avg}))$ where $(V_{CONTROL,avg})$ is the $V_{CONTROL}$ averaged or dc value and $(\Delta V_{CONTROL})$ the $V_{CONTROL}$ ripple, is the actual magnitude to minimize.

The loop gain of circuits that do not feature the feed-forward function, is proportional to the square of the line magnitude. This is attested by the power delivery expression that depends on $V_{CONTROL,avg}$ and on the square of the rms line voltage $(P_{in,avg} = k \times ((V_{line,rms}^2 \cdot V_{CONTROL,avg})/(L)))$ where k is a constant. Hence, the $V_{CONTROL}$ dc value is very low at high line, light load and becomes larger when the load increases or the line decreases. That is why the ripple impact is much significant at high line, light load where the $V_{CONTROL}$ dc value is small. The NCP1611 and NCP1612 improve the situation since they feature a 2-level feed-forward function that limits the $V_{CONTROL}$ decay at high line.

If not sufficient, it can be good to note that the inductor value appears in the denominator of the power expression. Hence, the higher the inductor value, the higher the $V_{CONTROL}$ dc value for an operating point (see the exact power expressions given in the data sheet). Hence, in that perspective, using a higher-inductance coil can help improve the PF/THD performance.

Inhibit the Skip Mode Function

The skip mode prevents the operation near the line zero crossing for an optimized efficiency particularly at light load. This is however at the cost of some THD degradation. The skip mode function must then be inhibited if the THD is too low. See the “I want to inhibit the skip function” section.

Limit the Size of the X2 Capacitors

Power factor generally declines in high line conditions. This decay is mainly due to the EMI filter and in particular to the X2 capacitors and other filtering capacitors. In fact, the voltage across these capacitors is sinusoidal. These capacitors are then the seat of a reactive current that charges and discharges them as necessary to force this sinusoidal voltage $(i_c(t) = C \times ((d)/(dt))(v_c(t))$. These currents add to the current drawn by the PFC stage to form the line current.

The simple simulation circuit of Figure 6 can illustrate this phenomenon. A sinusoidal voltage source V_1 is applied to a resistor R_2 through a filter C_1, L_1 and C_2. Elements V_3, V_4, V_5 and V_2 are 0 V voltage sources only used to monitor the current flowing through them. The R_2 resistive load represents an ideal PFC stage that draws a pure sinusoidal current.

1. In general, discontinuous conduction mode PFC stages actually are designed to operate in critical conduction mode. They exhibit relatively poor PF ratios when the switching frequency is clamped. ON Semiconductor Frequency Clamped CrM controllers (e.g. NCP1605 or NCP1631) solve the issue by the implementation of a “V_{TON} processing block” that modulates the on-time with respect to dead-times sensed during the precedent switching periods. The same proved structure is re-used in the newest NCP1611 and NCP1612 CCFF circuits (see data sheet).
2. The Dynamic Response Enhancer dramatically speeds-up the regulation loop when the output voltage goes below 95.5% of its regulation level.

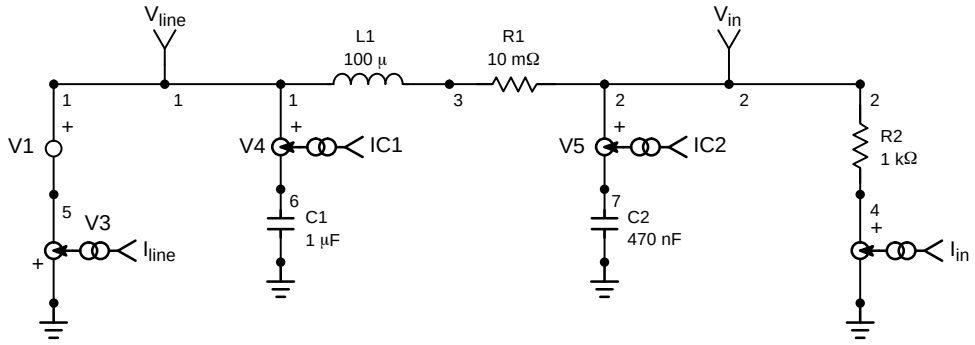


Figure 6. A Simple Circuit to Simulate the Impact of the EMI Capacitors

As illustrated by Figure 7, the currents circulating within C_1 (I_{c1}) and C_2 (I_{c2}) are sinusoidal but 270° phase shift compared to the line. They must be added to the PFC current (I_{R2}) to obtain the line current. Finally, the line current is the sum of the three sinusoidal currents ($I_{in} + I_{c1} + I_{c2}$) and hence is a phase shift sinusoid. See below:

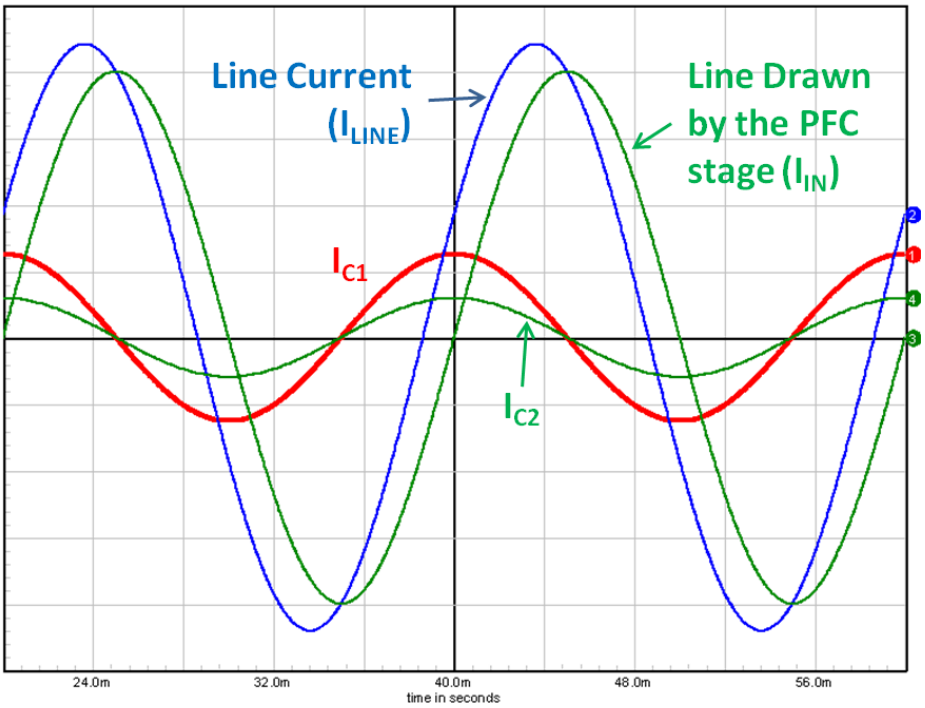


Figure 7. Line Current

At light load, the effect is worse compared to full load. In fact, the PFC stage current (I_{in}) is small since the power demand is low. On the other hands, yet, the reactive current within the capacitors that only depends on the line frequency and on the line magnitude, does not decay. Hence $I_{c1} + I_{c2}$ have a higher relative impact on I_{line} that is the sum: $I_{in} + I_{c1} + I_{c2}$. This is why PF drops in light load conditions.

By the way, the input voltage ac content is larger in high-line conditions. So are the C_1 and C_2 voltage swings and hence, the I_{c1} and I_{c2} currents. This is why high PF ratios are particularly difficult to obtain in high-line and light-load situations.

Thus, High PF ratios impose the capacitors to be as low as possibly allowed by the EMI constraints.

Limit the Changes in the Switching Frequency

The NCP1611 and the NCP1612 are designed to drive PFC boost stages in so-called **C**urrent **C**ontrolled **F**requency **F**old-back (**CCFF**). In this mode, the PFC stage classically operates in **Cr**itical conduction **M**ode (**CrM**) when the line current exceeds a programmable value. When the current is below this preset level, the NCP1612 linearly reduces the frequency down to about 20 kHz when the current is nearly zero. **CCFF** maximizes the efficiency at both nominal and light load. In particular, stand-by losses are reduced to a minimum. Similarly to **FCCrM** controllers, an internal circuitry allows near-unity power factor even when the switching frequency is reduced.

Practically, as a result of an internal computation, the FFcontrol pin sources a current representative of the line current. A resistor is then connected between the FFcontrol and ground pins to generate a voltage representative of the line current. When this voltage exceeds the internal 2.5 V reference (V_{REF}), the circuit operates in critical conduction mode. If the FFcontrol pin voltage ($V_{FFcontrol}$) is below 2.5 V, a dead-time is generated that approximately equates ($66\ \mu s \times (1 - ((V_{FFcontrol})/(V_{REF}))$). By this means, the circuit forces a longer dead-time when the line current is small and a shorter one as the line current is higher. Also as aforementioned, the circuit further skips cycles whenever the FFcontrol pin is below 0.65 V to prevent the PFC stage from operating near the line zero crossing where the power transfer is particularly inefficient.

The CCFF operation is summarized by Figure 8.

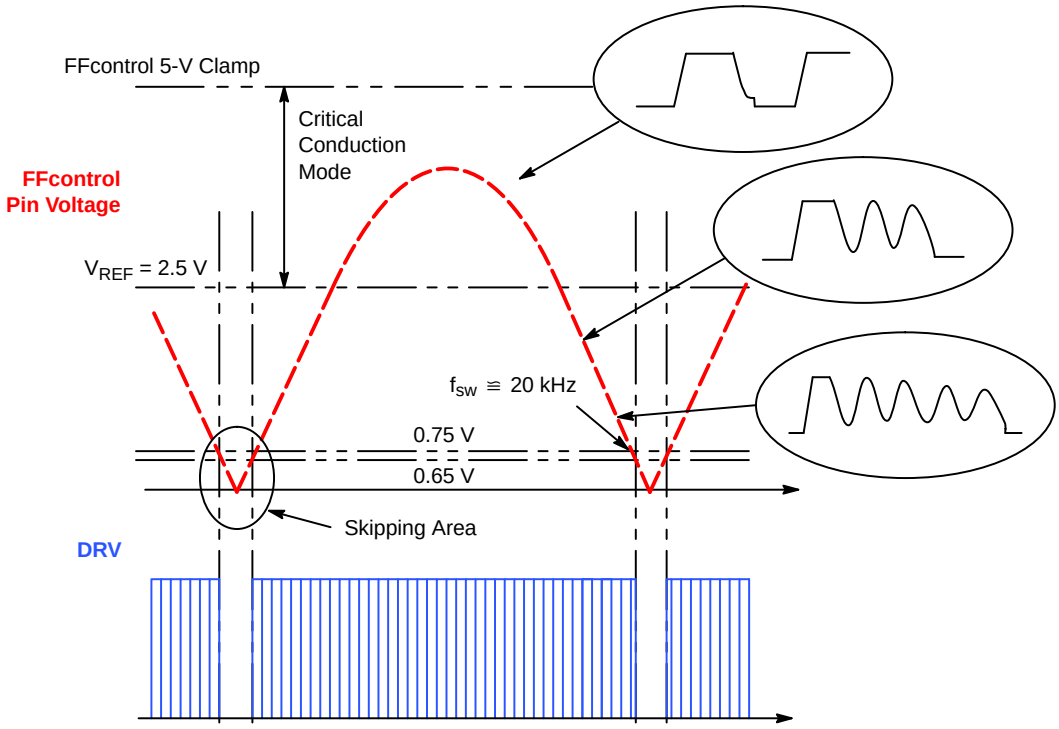


Figure 8. Current Controlled Frequency Fold-back

As aforementioned, clamping the switching frequency of a CrM PFC boost normally leads to a distorted line current since traditional current shaping schemes assume a critical conduction mode operation. This traditional limitation is solved in the NCP1611 and the NCP1612 in the same way as in FCCrM circuits from ON Semiconductor (NCP1605 for instance): a V_{TON} processing block is integrated that modulates the on-time to compensate the presence of dead-times. This block is based on an integrator (see data sheet for more details) whose time constant is nearly 100 μs for a proper filtering of the switching ripple.

As suggested by Figure 8, the switching frequency can vary very rapidly from 20 kHz DCM operation to CrM operation in heavy load conditions. The V_{TON} processing block may have difficulties to adapt to the rapid changes in the dead-times durations and to timely compensate them. This can lead to the circled glitches observed on the line current shape of Figure 10a) and degrade the THD.

The impact on the THD can be minimized by limiting the FFcontrol swing (and hence the switching frequency variations) as shown in Figure 9 where R_{FF} is the resistor that placed on the FFcontrol pin sets the wished line current level below CCFF reduces the switching frequency (as returned by the NCP1611 or NCP1612 Design Worksheet (Note 3) for instance). Two ways are sketched in Figure 9 that give similar results meaning that:

- The line current below which the system reduces the switching frequency is approximately the same as if the tweak was not applied.
- The FFcontrol swing is about 30% of the signal amplitude in both cases. Such an amount remains welcome to maintain the skip mode synchronized to the line.

3. Design tool available at http://www.onsemi.com/PowerSolutions/supportDoc.do?type=tools&rpn=NCP1611 (NCP1611) or http://www.onsemi.com/PowerSolutions/supportDoc.do?type=tools&rpn=NCP1612 (NCP1612)

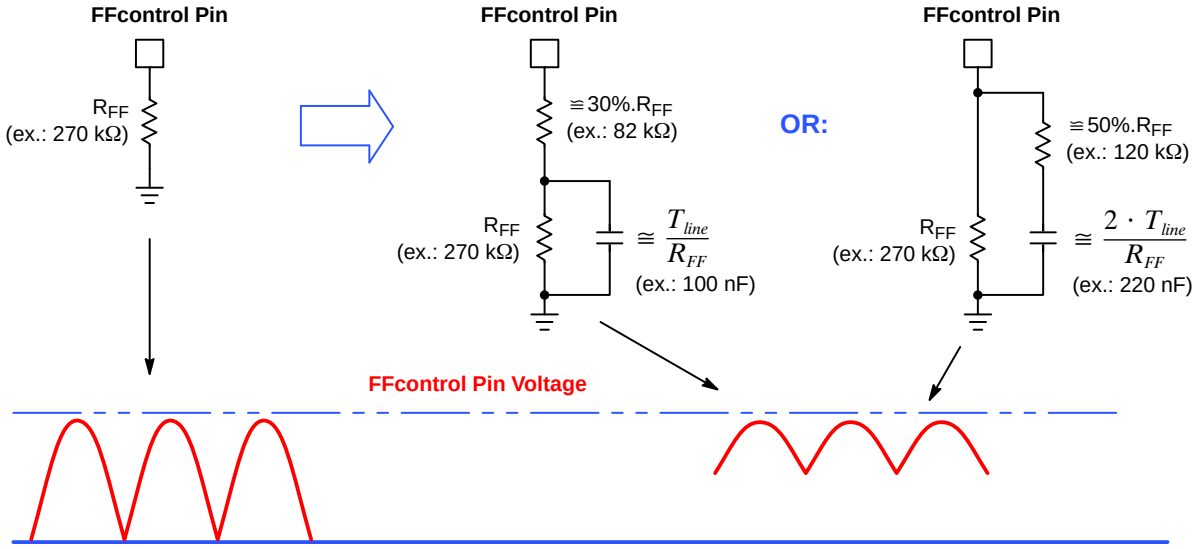
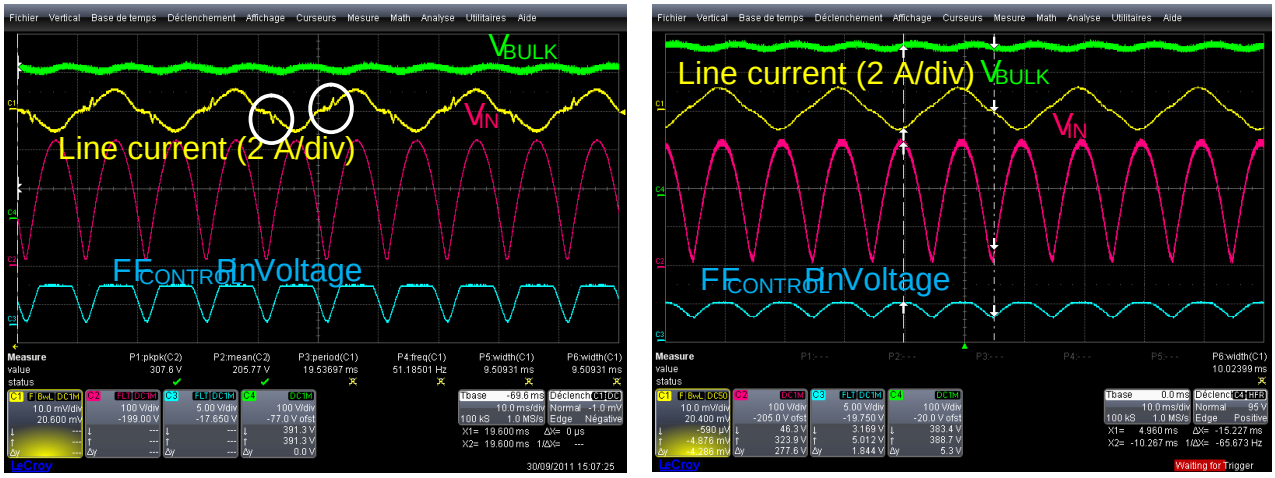


Figure 9. Reducing the FFcontrol Pin Swing to Slow Down the Switching Frequency Variations

Contrary to the NCP1611 evaluation board (“NCP1611GEVB”), the NCP1612 evaluation board (“NCP1612GEVB”) consists of the tweak. This is why, as shown in Figure 10b), the NCP1612GEVB line current is cleaner since the glitches are suppressed. The THD is particularly improved in light load conditions: for instance, at 20% load, we have 8% instead of 20% at 115 V or 18% instead of 33% at 230 V. More data could be found in the evaluation board manual:
(refer to http://www.onsemi.com/pub_link/Collateral/EVBUM2051−D.PDF for NCP1612GEVB,
to http://www.onsemi.com/pub_link/Collateral/EVBUM2049−D.PDF for NCP1611GEVB).



a. NCP1611EVB Configuration

b. NCP1612GEVB Configuration

Figure 10. NCP1611/2 Evaluation Board @ 230 V, full load

I FACE BURST OPERATION WHEN THE LINE VOLTAGE IS LOW OR AT THE BORDER BETWEEN THE LOW AND HIGH LINE RANGES

As aforementioned, the NCP1611 and NCP1612 detect the line range for feed-forward. By default, the circuit operates the “low-line gain” mode. In this state, the on-time is limited to 25 μs (typically). If V_{SENSE} exceeds 2.2 V, the circuit detects that the circuit operates in high-line condition and both the PWM gain and the maximum on-time are reduced by a ratio of 3 ($t_{on,max} \cong 8.3$ μs, typically). The PFC stage remains in the high−line configuration until V_{SENSE} happens to stay below 1.7 V for more than 25 ms. See Figure 1. This 2-step feed-forward capability limits the open loop gain variations (see Figure 11) that otherwise, would vary as a function of the square of the line amplitude.

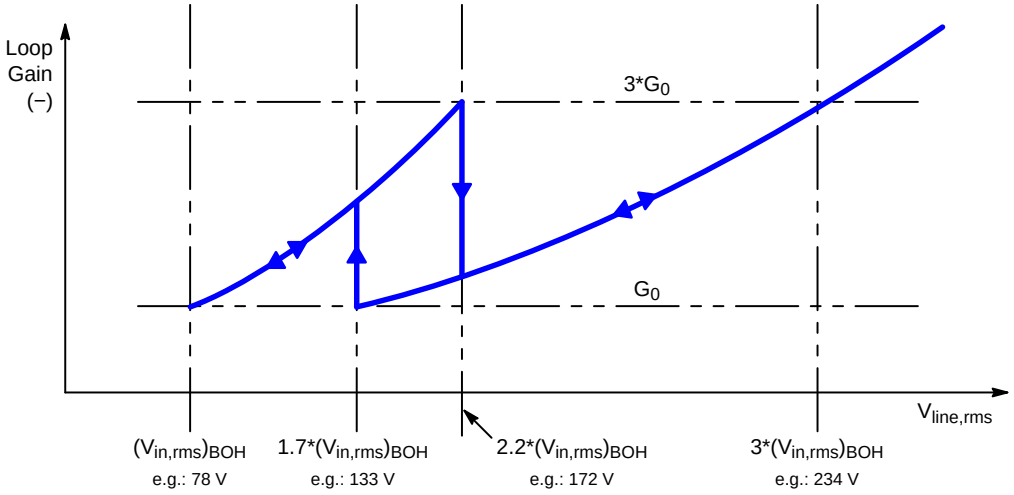


Figure 11. Open Loop Gain Characteristics

When the line voltage slowly decays and leads the V_{SENSE} pin voltage to go below 1.7 V, the low-line range is detected. In virtue of the feed-forward function, the on-time is suddenly multiplied by 3. So is the power delivery. A transient power excess occurs that is particularly significant in heavy load conditions. PFC stages exhibiting a low loop bandwidth, they slowly react and have difficulty to sharply contain the bulk voltage rise. As a consequence, the Over-Voltage Protection may trip and (despite its soft nature – see data sheet) promptly stop the power delivery. However, the differential mode inductor generally inserted in the EMI filter prevents the line current from immediately dropping to zero. Hence, the line current continues flowing until the differential mode inductor is fully discharged. During this discharge delay, the PFC stage must absorb the line current imposed by the magnetic element but stops fueling the output. Ultimately, the energy drawn from the mains, charges the input capacitor (C_{in} placed across the diode bridge at the input of the PFC stage).

If the voltage across C_{in} is monitored by the controller, it may detect that the V_{SENSE} pin exceeds the 2.2 V upper threshold for line range detection and sets the high-line range detection. Hence, the circuit recovers the exact initial configuration. A new detection of the low-line range followed by an OVP event all that finishing into new high-line detection.

This hiccup functioning is illustrated by Figure 12.

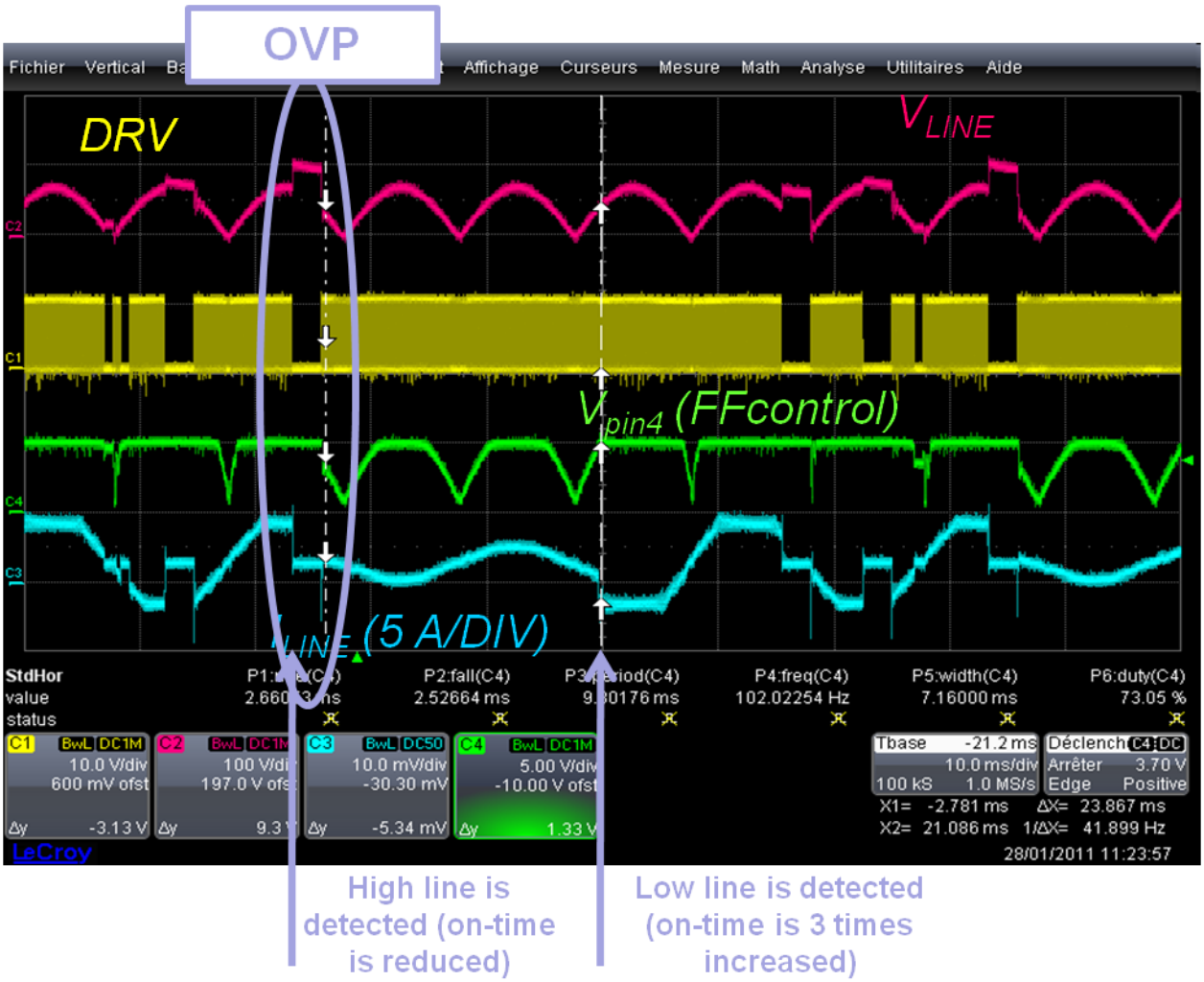


Figure 12. Hesitations Between the Low-Line and High-Line Ranges

Such a risk is highly limited by the soft OVP function (see data sheet) and the large hysteresis of the line range detection comparator (2.2 V and 1.7 V are the thresholds). However, it is wise to sense the input voltage as illustrated by Figure 13. The line voltage is monitored in the mains side of the differential mode inductor so that the sensed voltage is not affected in case of a sudden stop of the PFC stage operation. The solution re-uses the resistors generally placed between the two line wires to discharge the X2 capacitors (safety requirements). These resistors, $\mathbf{R_{X1}}$ and $\mathbf{R_{X2}}$ scale down the input voltage that can then be easily sensed by the controller. Refer to [3] or [4] for more details.

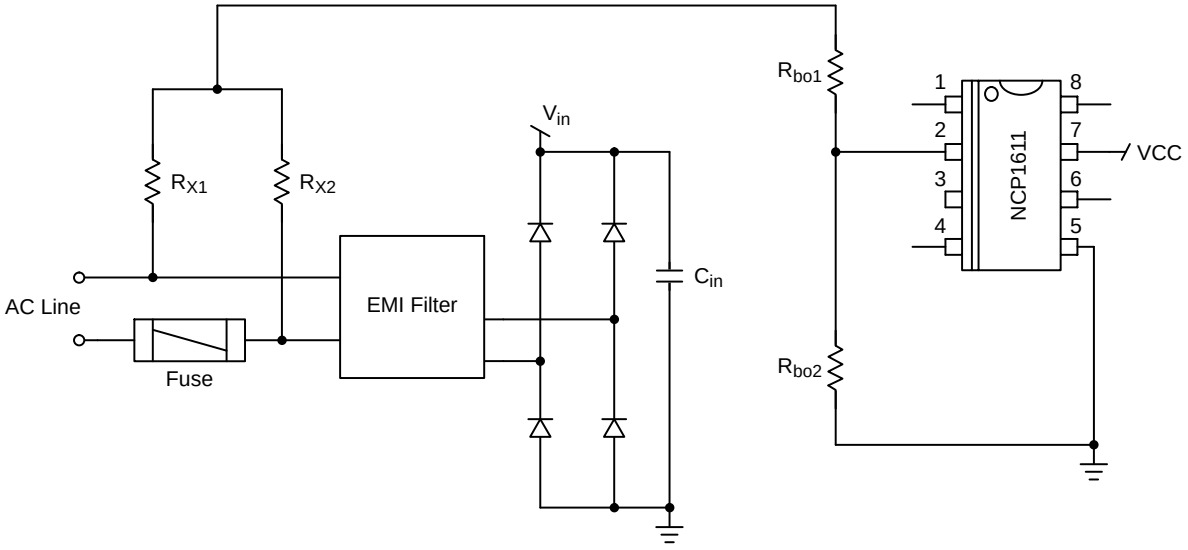


Figure 13. Sensing the Line Voltage

References

[1] NCP1611 Design Worksheet, refer to http://www.onsemi.com/PowerSolutions/supportDoc.do?type=tools&rpn=NCP1611

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