AND8456/D

Further Improve the Low-Power Efficiency of Your NCP1631-Driven Interleaved PFC

ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

Environmental concerns lead to new efficiency requirements when designing modern power supplies. For instance, the 80 PLUS® initiative and moreover its bronze, silver and gold derivatives force desktops and servers manufacturers to work on innovative solutions (Note 1). An important focus is on the PFC stage that with the EMI filter can be easily consume 5% to 8% of the output power at low line, full load. Interleaved PFC (IPFC) is one of the options to meet these new requirements.

Interleaving consists in paralleling two "small" stages in lieu of a bigger one, which may be more difficult to design. Practically, two 150 W PFC stages are combined to form our 300 W PFC pre-regulator. Requiring more but smaller components, IPFC becomes particularly popular in applications where a strict form factor has to be met like for instance, in slim notebook adapters or in LCD TVs.

Critical Conduction Mode (CrM) and furthermore its frequency-limited version (Frequency Clamped Critical conduction Mode – FCCrM) are very efficient and cost-effective techniques (no need for low t_{rr} diodes). In addition to the well-known other IPFC merits (reduced ripple of the input/output current, improved heating distribution…), interleaving also extends the load range for which the power is optimally processed in CrM and FCCrM.

The NCP1631 is designed to operate in CrM when the input current is high. It generally clamps the frequency near the line zero crossing where the current is low. The fixed frequency operation also takes place over the entire line sine-wave at light load. This is particularly true with the NCP1631 that linearly decays the clamp frequency as a function of the power to maintain high efficiency levels even in very light load. The power threshold under which frequency reduces is programmed by the resistor placed between pin 6 and ground. To prevent any risk of regulation loss at no load, the circuit further skips cycles when the error amplifier reaches its low clamp level.

This application note gives recommendations on how adjusting the frequency fold-back characteristics to optimize the efficiency over the load range.

NCP1631 Frequency Fold-back

Figure 2 portrays the way the NCP1631 manages the frequency fold-back function. V_{REGUL} is a signal derived from the $V_{control}$ output of the regulation block. As detailed in Reference 1, this signal dictates the power delivery following the following equation:

$$P_{in,avg} = \frac{(R_T)^2 \cdot V_{REGUL}}{26.9 \cdot 10^{12} \cdot L \cdot k_{BO}{}^2} \qquad \textit{(eq. 1)}$$

Where:

- R_t is the timing resistor connected to pin 3 to set the maximum on-time
- L is the inductor value
- k_{BO} is the brown-out scale-down factor

Please note that owing to the NCP1631 $\mathbf{V_{in}^2}$ feed-forward function, the power expression is independent from the line magnitude. In a specific design, R_t, L and k_{BO} are fixed values and the power delivery is the only function of $\mathbf{V_{REGUL}}$. $\mathbf{V_{REGUL}}$ is linked to the control signal as follows:

$$V_{REGUL} = \frac{V_{control} - V_F}{1.8} \qquad \textit{(eq. 2)}$$

Where:

- $V_{control}$ is the control signal available on pin 5 that peaks to 3.6 V
- $\mathbf{V_F}$ is the minimum $\mathbf{V_{control}}$ level (about 0.6 V)

$V_{control}$ varying between about 0.6 V and 3.6 V. Thus as illustrated in Figure 1, V_{REGUL} is between 0 V and 1.66 V that corresponds to the maximum power that can be delivered ($(P_{in,avg})_{HL}$).

1. Refer to http://www.80plus.org/ for more details.

January, 2013 – Rev. 1
Publication Order Number:
AND8456/D

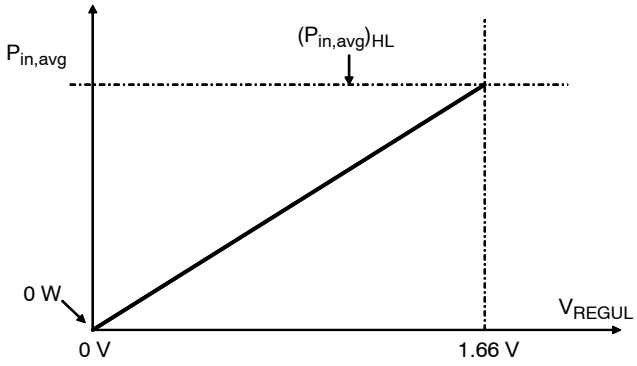

Figure 1. Averaged Input Power versus the V_{REGUL} Signal

As shown in Reference 1, $(P_{in,avg})_{HL}$ that designates the maximum power capability of the PFC stage (i.e., the power provided if V_{REGUL} equals its 1.66 V maximum value), is selected at least 30% higher than the power really needed in the application to offer some margin ($(P_{in,avg})_{HL} \geq 130\%$ $(P_{in,avg})_{max}$) (Note 2).

Substitution of V_{REGUL} by its maximum value in Equation 1 leads to:

$$\left(P_{in,avg}\right)_{HL} = \frac{(R_t)^2 \cdot (V_{REGUL})_{max}}{26.9 \cdot 10^{12} \cdot L \cdot k_{BO}{}^2} \cong \cong \frac{(R_t)^2}{16.2 \cdot 10^{12} \cdot L \cdot k_{BO}{}^2} \quad \textit{(eq. 3)}$$

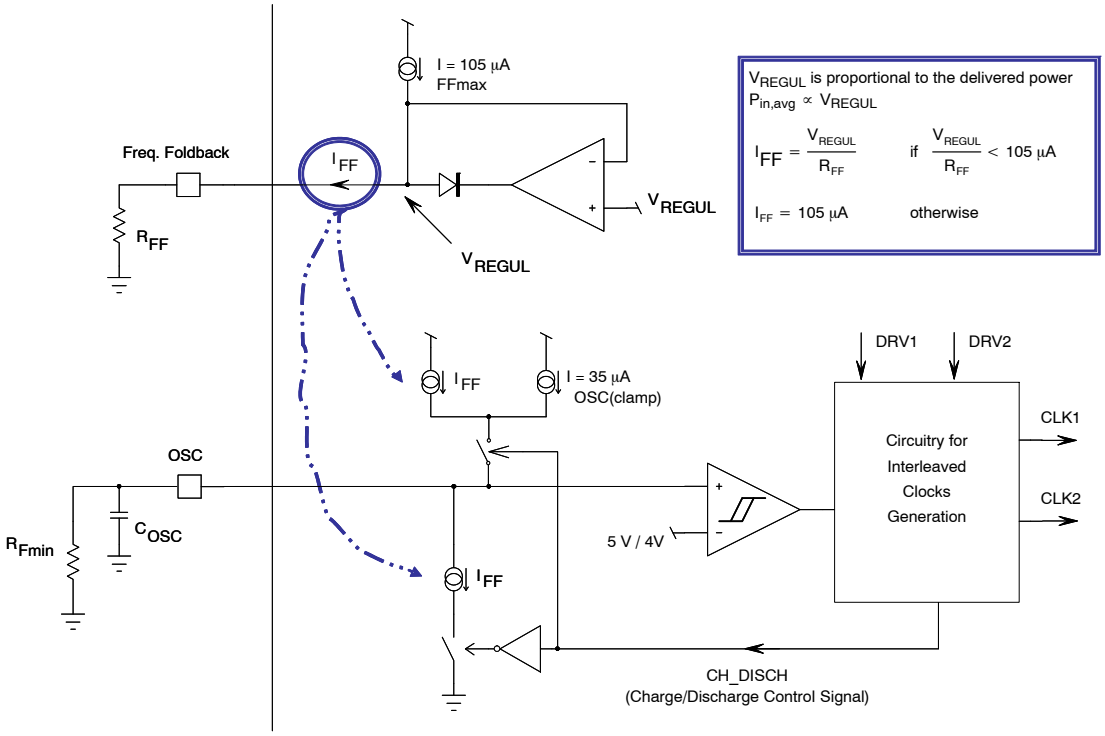

Figure 2. Oscillator and Frequency Fold-back

2. $(P_{in,avg})_{HL}$ stands for Highest Level of the power.

As illustrated in Figure 2, the circuit maintains the voltage $\mathbf{V_{REGUL}}$ on the Frequency Fold-back pin. An external resistor, $\mathbf{R_{FF}}$, is placed that connects pin 6 to ground. The circuit sources the current I_{FF}necessary to force the $\mathbf{V_{REGUL}}$ voltage across $\mathbf{R_{FF}}$ resistor. However, pin 6 has a current capability that is purposely limited to I_{FFmax} (I_{FFmax} = 105 μA). As long as $\mathbf{V_{REGUL}}$ is below ($R_{FF} \cdot I_{FFmax}$), the I_{FF} current is high enough to maintain $\mathbf{V_{REGUL}}$ on pin 6. When $\mathbf{V_{REGUL}}$ exceeds ($R_{FF} \cdot I_{FFmax}$), I_{FF} equates it clamp value I_{FFmax}.

As a matter of fact:

- $I_{FF} = (V_{REGUL}/V_{FF})$ when $V_{REGUL} \le R_{FF} \cdot I_{FFmax}$
- $I_{FF} = I_{FFmax}$ when $V_{REGUL} \ge R_{FF} \cdot I_{FFmax}$

The current I_{FF} is used to charge and discharge the oscillator external capacitor:

- The charge current is ($I_{FF} + I_{OSC(clamp)}$) where $I_{OSC(clamp)}$ is a fixed 35 μA current source
- The discharge current is I_{FF}

The frequency clamp is then maximal at high load when ($V_{REGUL} \ge R_{FF} \cdot I_{FFmax}$). This is the nominal frequency. When $V_{REGUL} \le R_{FF} \cdot I_{FFmax}$, the clamp frequency linearly decreases as a function of $\mathbf{V_{REGUL}}$ until its minimum level. This minimal frequency is adjusted by the resistor placed in parallel with the oscillator capacitor ($\mathbf{R_{Fmin}}$ of Figure 2). See Reference 1 to see how to compute this resistor or use the Microsoft Excel® spreadsheet available at http://www.onsemi.com/pub/Collateral/NCP1631%20DWS.XLS.

A Steeper Frequency Fold-back Characteristic

The frequency fold-back can be tweaked by adding a resistor between the pfcOK and Frequency Fold-back pins. This is portrayed by Figure 3. When the PFC stage operates in nominal operation, the pfcOK pin provides a 5 V voltage source. The voltage on the FF pin is $\mathbf{V_{REGUL}}$. Hence, the bottom resistor ($\mathbf{R_{FF2}}$) placed between the FF pin and ground sinks (V_{REGUL}/R_{FF2}) as long as the pin 6 current does not exceed (I_{FFmax} = 105 μA). The upper resistor ($\mathbf{R_{FF1}}$) added between the pfcOK and FF pins provides ($(5\ V - V_{REGUL})/R_{FF1}$). Finally, the FF pin sources:

$$\left(\frac{V_{REGUL}}{R_{FF2}} - \frac{5\ V - V_{REGUL}}{R_{FF1}}\right)$$

or

$$\left(\left(\frac{R_{FF1} + R_{FF2}}{R_{FF1} \cdot R_{FF2}} V_{REGUL}\right) - \frac{5\ V}{R_{FF1}}\right)$$

Then:

- $I_{FF} = I_{FFmax}$ if

$$V_{REGUL} \ge \frac{R_{FF2} \cdot \left(\left(R_{FF1} \cdot I_{FFmax}\right) + 5\ V\right)}{R_{FF1} + R_{FF2}}$$

- $I_{FF} = 0$ if

$$V_{REGUL} \le \frac{R_{FF2} \cdot 5\ V}{R_{FF1} + R_{FF2}}$$

- $I_{FF} = \left(\left(\frac{R_{FF1} + R_{FF2}}{R_{FF1} \cdot R_{FF2}} V_{REGUL}\right) - \frac{5\ V}{R_{FF1}}\right)$ otherwise

Where I_{FFmax} is the clamp value of the current source by the FF pin (I_{FFmax} = 105 μA).

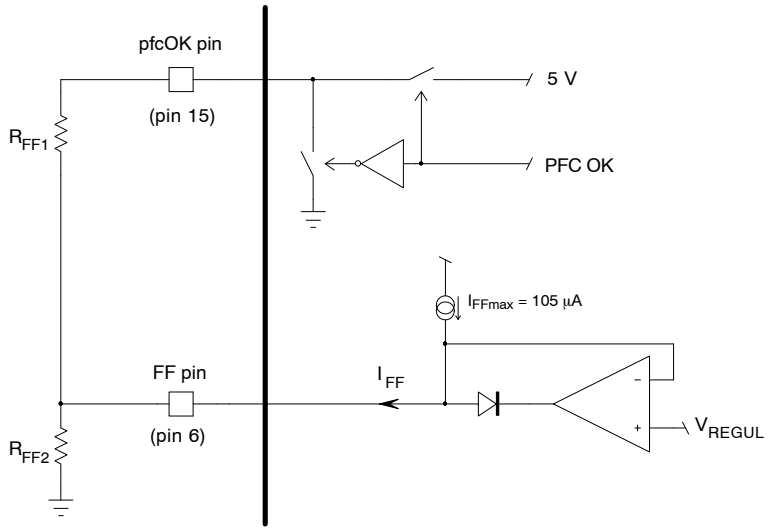

Figure 3. Resistor R_{FF1} Tweaks the Fold-back Characteristic

The oscillator is then charged and discharged by currents that depend on $\mathbf{V_{REGUL}}$ until this voltage reaches ($R_{FF} \cdot I_{FFmax}$) so that the frequency decreases when $\mathbf{I_{FF}}$ decays (see Figure 2).

The lowest efficiency ratios are generally obtained at low line. Hence, the PFC stage must be optimized in this condition. Experiments show that in most applications, the clamp frequency must be minimal at 20% of the load but that operation in CrM is optimal at 50% of the load.

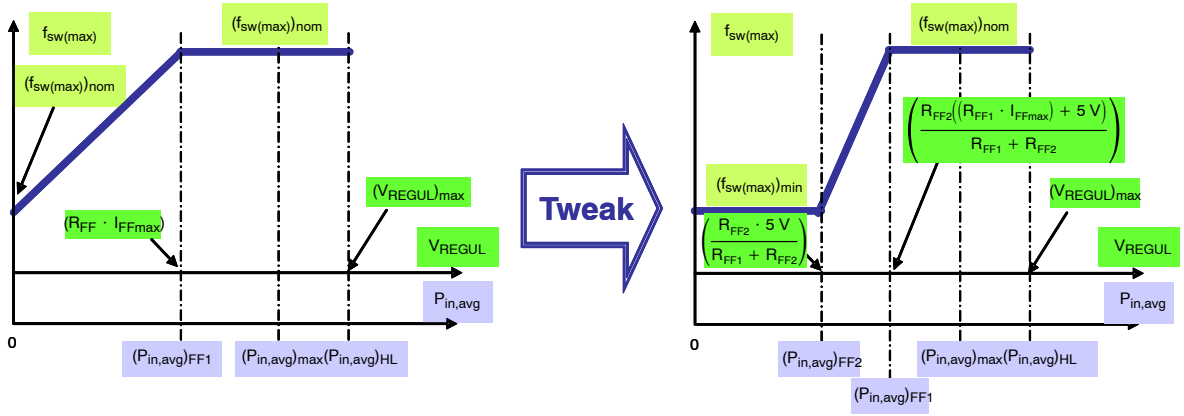

Figure 4. Change in the Frequency Clamp ($f_{sw(max)}$) Characteristic as a Function of the Frequency Fold-back Setting

Table 1 summarizes the fold-back power levels as a function of the PFC stage power capability $(P_{in,avg})_{HL}$. $(P_{in,avg})_{HL}$ is the power that can be delivered by the PFC stage based on the selected timing resistor ($\mathbf{R_t}$ applied to pin 3 to set the maximum on-time). $(P_{in,avg})_{HL}$ must be chosen so that $(P_{in,avg})_{HL}$ is at least 30% higher than $(P_{in,avg})_{max}$, the power actually needed.

Table 1. FREQUENCY FOLD-BACK POWER THRESHOLD WITH AND WITHOUT THE TWEAK

	Without Tweak	With Tweak
Maximum power of your application	$(P_{in,avg})_{max}$	$(P_{in,avg})_{max}$
Power Capability of the PFC stage	$\left(P_{in,avg}\right)_{HL} \cong \frac{R_t^{\,2}}{16209 \cdot 10^9 \cdot L \cdot k_{BO}^{\,2}}$	$\left(P_{in,avg}\right)_{HL} \cong \frac{R_t^{\,2}}{16209 \cdot 10^9 \cdot L \cdot k_{BO}^{\,2}}$
Power threshold below which the frequency reduces	$\frac{\left(P_{in,avg}\right)_{FF1}}{\left(P_{in,avg}\right)_{HL}} = \frac{R_{FF} \cdot I_{FFmax}}{\left(V_{REGUL}\right)_{max}}$	$\frac{\left(P_{in,avg}\right)_{FF1}}{\left(P_{in,avg}\right)_{HL}} \cong \frac{\frac{R_{FF2} \cdot \left(\left(R_{FF1} \cdot I_{FFmax}\right) + 5\,V\right)}{R_{FF1} + R_{FF2}}}{\left(V_{REGUL}\right)_{max}}$
Power level below which the minimal frequency is obtained	$\frac{\left(P_{in,avg}\right)_{FF2}}{\left(P_{in,avg}\right)_{HL}} \cong 0$	$\frac{\left(P_{in,avg}\right)_{FF2}}{\left(P_{in,avg}\right)_{HL}} \cong \frac{\frac{R_{FF2} \cdot 5\,V}{R_{FF1} + R_{FF2}}}{\left(V_{REGUL}\right)_{max}}$

Where:

- R_T is the timing resistor applied to pin3 to adjust the maximum on-time
- k_{BO} is the brown-out scale-down factor
- L is the inductor value
- I_{FFmax} is the maximum current that can be sourced by the FF pin: I_{FFmax} = 105 μA
- $(V_{REGUL})_{max}$ is the maximum V_{REGUL} voltage: $(V_{REGUL})_{max}$ = 1.66 V

Practical Implementation

The method has been applied on the 300 W NCP1631 demo-board. As documented in Reference 2, in this application:

- R_T = 18 kΩ is the timing resistor applied to pin 3 to adjust the maximum on-time
- $k_{BO} = \frac{120\ k\Omega}{120\ k\Omega + 7200\ k\Omega} = \frac{1}{61}$ (since a 7,200 kΩ $\mathbf{R_{BO1}}$ resistor is applied between the input voltage rail and the BO pin and a 120 kΩ $\mathbf{R_{BO2}}$ resistor connects the BO pin to ground − $k_{BO} = \frac{R_{BO1}}{R_{BO1} + R_{BO2}}$)
- L = 150 μH
- R_{FF} = 4.7 kΩ

For the tweak, R_{FF} is replaced by (R_{FF2} = 2 kΩ) and (R_{FF1} = 33 kΩ) is placed between the pfcOK and FF pins. Table 2 gives the new FF power levels.

Table 2. EXAMPLE WITH A 300 W APPLICATION

	Without Tweak	With Tweak
Maximum power of your application	320 W	320 W
Power Capability of the PFC stage	$\left(P_{in,avg}\right)_{HL} \cong \frac{18000^2}{16209 \cdot 10^9 \cdot 150 \cdot 10^{-6} \cdot \frac{1}{61}2} \cong 496$ $\Rightarrow \left(P_{in,avg}\right)_{max} \cong 64\% \cdot \left(P_{in,avg}\right)_{HL}$	$\left(P_{in,avg}\right)_{HL} \cong \frac{18000^2}{16209 \cdot 10^9 \cdot 150 \cdot 10^{-6} \cdot \frac{1}{61}2} \cong 496$ $\Rightarrow \left(P_{in,avg}\right)_{max} \cong 64\% \cdot \left(P_{in,avg}\right)_{HL}$
Power threshold below which the frequency reduces	$\frac{\left(P_{in,avg}\right)_{FF1}}{\left(P_{in,avg}\right)_{HL}} = \frac{4.7k \cdot 105\mu}{1.66} \cong 30\%$ or $\frac{\left(P_{in,avg}\right)_{FF1}}{\left(P_{in,avg}\right)_{max}} = \frac{30\% \cdot \left(P_{in,avg}\right)_{HL}}{64\% \cdot \left(P_{in,avg}\right)_{HL}} \cong 46\%$	$\frac{\left(P_{in,avg}\right)_{FF1}}{\left(P_{in,avg}\right)_{HL}} \cong \frac{\frac{2k \cdot ((33k \cdot 105\mu) + 5\ V)}{2k + 33k}}{1.66} \cong 29\%$ or $\frac{\left(P_{in,avg}\right)_{FF1}}{\left(P_{in,avg}\right)_{max}} \cong \frac{29\% \cdot \left(P_{in,avg}\right)_{HL}}{64\% \cdot \left(P_{in,avg}\right)_{HL}} \cong 45\%$
Power level below which the minimal frequency is obtained	$\frac{\left(P_{in,avg}\right)_{FF1}}{\left(P_{in,avg}\right)_{HL}} = 0$ or $\frac{\left(P_{in,avg}\right)_{FF1}}{\left(P_{in,avg}\right)_{max}} = 0$	$\frac{\left(P_{in,avg}\right)_{FF2}}{\left(P_{in,avg}\right)_{HL}} = \frac{\frac{2k \cdot 5\ V}{33k + 2k}}{1.66} \cong 17\%$ or $\frac{\left(P_{in,avg}\right)_{FF2}}{\left(P_{in,avg}\right)_{max}} = \frac{17\% \cdot \left(P_{in,avg}\right)_{HL}}{64\% \cdot \left(P_{in,avg}\right)_{HL}} \cong 27\%$

The novel frequency fold-back characteristic was implemented. The nominal clamp frequency $(f_{sw(max)})_{nom}$ was doubled (250 kHz instead of 125 kHz) to obtain a critical conduction mode operation at 50% of the load. Instead of the 270 kΩ initially selected, a ($\mathbf{R_{Fmin}}$ = 820 kΩ) resistor was placed across the oscillator capacitor to set a 20 kHz minimum clamp frequency ($(f_{sw(max)})_{min}$ = 20 kHz). As shown by Table 2, the clamp frequency decays from 45% of the load down to $(f_{sw(max)})_{min}$ at 27% of the load.

As wished, operation @ 50% of the load is in CrM and the frequency is clamped to 20 kHz at 20% of the load for a flatter efficiency characteristic over the power range, as depicted by Figure 5.

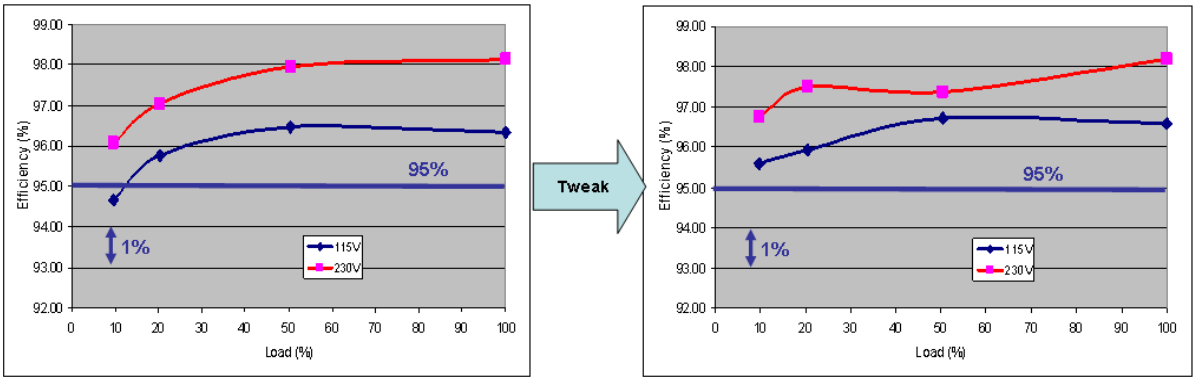

Figure 5. Efficiency Comparison

These results are obtained with small 150 μH, PQ2620 inductors.

References

1. Joel Turchi, “Key steps to design an interleaved PFC stage driven by the NCP1631”, Application Notes AND8407, http://www.onsemi.com/pub/Collateral/AND8407–D.PDF.
2. Stephanie Conseil, “Performance of a 300 W Interleaved PFC driven by the NCP1631”, Evaluation Board Documents NCP1631EVB/D, http://www.onsemi.com/pub/Collateral/NCP1631EVB–D.PDF.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81–3–5817–1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative