REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add case outline L. - drw	99-09-01	Raymond Monnin
B	Drawing updated to reflect current requirements. - rrp	04-12-15	Raymond Monnin
C	Redrawn. Update paragraphs to MIL-PRF-38535 requirements. - drw	17-01-12	Charles F. Saffle

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C		
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12		

PMIC N/A

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Dan Wonnell

CHECKED BY
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APPROVED BY
Ray Monnin

DRAWING APPROVAL DATE
96-07-25

REVISION LEVEL
C

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, DIGITAL-LINEAR, CMOS, SINGLE SUPPLY, 600 KSPS, 12-BIT, A/D CONVERTER, MONOLITHIC SILICON

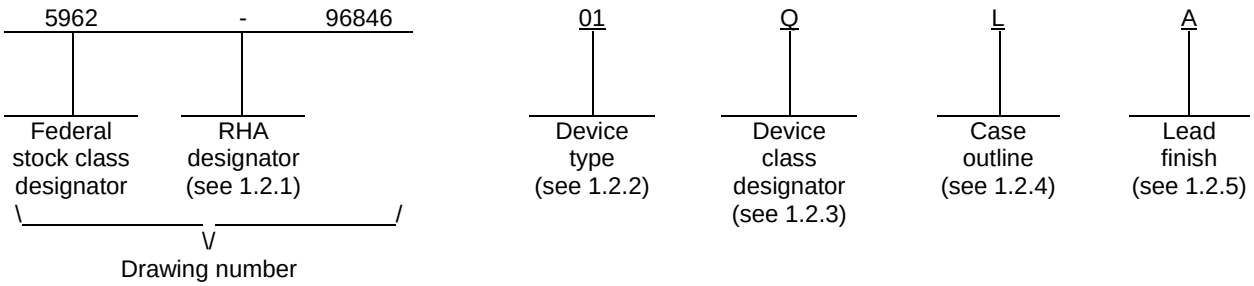
SIZE	CAGE CODE	
A	**67268**	**5962-96846**

SHEET 1 OF 12

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	7892S	Single supply 12-bit 600 KSPS ADC

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/

V_{DD} to AGND	-0.3 V dc to +7 V dc
V_{DD} to DGND	-0.3 V dc to +7 V dc
Analog input voltage to AGND	±17 V dc
Reference input voltage to AGND	-0.3 V dc to V_{DD} + 0.3 V dc
Digital input voltage to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
Digital output voltage to DGND	-0.3 V dc to V_{DD} + 0.3 V dc
Power dissipation (P_D)	450 mW
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+150°C
Lead temperature (soldering, 10 sec)	+300°C
Thermal resistance, junction-to-ambient (θ_{JA})	70°C/W

1.4 Recommended operating conditions.

Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Signal to noise ratio + distortion ratio	SNR	f_{IN} = 100 kHz, f_{SAMPLE} = 500 ksps	1, 2, 3	01	70		dB
Total harmonic distortion	THD		1, 2, 3	01		-78	dB
Peak harmonic or spurious distortion	PHD		1, 2, 3	01		-79	dB
Intermodulation distortion	IMD	f_s = 49 kHz, f_b = 50 kHz	1, 2, 3	01		-78	dB
Resolution	RES		1, 2, 3	01		12	Bits
Minimum resolution for which no codes are guaranteed	RES_{MIN}		1, 2, 3	01		12	Bits
Relative accuracy	RA		1, 2, 3	01		±1	LSB
Differential nonlinearity	DNL		1, 2, 3	01		±1	LSB
Positive and negative full-scale error	FSE		1, 2, 3	01		±5	LSB
Bipolar zero error	BZE		1, 2, 3	01		±3	LSB
Input voltage range	V_{IN}	Input applied to V_{IN1} with V_{IN2} grounded	1, 2, 3	01		±10	V
Input resistance	R_{IN}	Input applied to V_{IN1} with V_{IN2} grounded	1, 2, 3	01	8		kΩ
REF IN input voltage range	V_{REFIN}	See 4.4.1c	4	01	2.38	2.625	V
Input impedance	R_{REF}	Resistor connected to internal reference node	1, 2, 3	01	1.6		kΩ
Reference input capacitance	C_{RIN}	See 4.4.1c	4	01		10	pF
REF OUT error	V_{RE}		1	01		±10	mV
			2, 3			±25	
Input high voltage	V_{INH}	V_{DD} = 5 V ±5%	1, 2, 3	01	2.4		V
Input low voltage	VINL	V_{DD} = 5 V ±5%	1, 2, 3	01		0.8	V
Input current	I_{IN}	V_{IN} = 0 V to V_{DD}	1, 2, 3	01		±10	µA
Input capacitance	C_{IN}	See 4.4.1c	4	01		10	pF
Output high voltage	V_{OH}	I_{SOURCE} = 200 µA	1, 2, 3	01	4		V
Output low voltage	V_{OL}	I_{SINK} = 1.6 mA	1, 2, 3	01		0.4	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Floating state capacitance	C_{FS}	DB11 - DB0, see 4.4.1c	4	01		15	pF
Floating state leakage current	I_{LKG}	DB11 - DB0	1, 2, 3	01		±10	µA
Power supply current	I_{DD}	normal operation	1, 2, 3	01		19	mA
Power dissipation	P_D	normal operation	1, 2, 3	01		95	mW
Conversion time	t_{CONV}	2/, see figure 2	1, 2, 3	01		1.68	µs
Acquisition time	t_{ACQ}	2/, see figure 2, see 4.4.1c	9, 10, 11	01	320		ns
$\overline{\text{CONVST}}$ pulse width	t_1	2/, see figure 2, see 4.4.1c	9, 10, 11	01	45		ns
$\overline{\text{EOC}}$ pulse width	t_2	2/, see figure 2, see 4.4.1c	9, 10, 11	01	60		ns
$\overline{\text{EOC}}$ falling edge to $\overline{\text{CS}}$ falling edge setup time	t_3	2/, see figure 2, see 4.4.1c	9, 10, 11	01	0		ns
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ setup time	t_4	2/, see figure 2, see 4.4.1c	9, 10, 11	01	0		ns
Read pulse width	t_5	2/, see figure 2, see 4.4.1c	9, 10, 11	01	45		ns
Data access time after falling edge of $\overline{\text{RD}}$	t_6	2/, 3/, see figure 2, see 4.4.1c	9, 10, 11	01		40	ns
Bus relinquish time after rising edge of $\overline{\text{RD}}$	t_7	2/, 4/, see figure 2, see 4.4.1c	9, 10, 11	01	5	40	ns
$\overline{\text{CS}}$ to $\overline{\text{RD}}$ hold time	t_8	2/, see figure 2, see 4.4.1c	9, 10, 11	01	0		ns
$\overline{\text{RD}}$ to $\overline{\text{CONVST}}$ setup time	t_9	2/, see figure 2, see 4.4.1c	9, 10, 11	01	200		ns
$\overline{\text{RFS}}$ low to SCLK falling edge setup time	t_{10}	2/, see figure 2, see 4.4.1c	9, 10, 11	01	35		ns
$\overline{\text{RFS}}$ low to data valid delay	t_{11}	2/, 3/, see figure 2, see 4.4.1c	9, 10 11	01		30	ns
SCLK high pulse width	t_{12}	2/, see figure 2, see 4.4.1c	9, 10, 11	01	25		ns
SCLK low pulse width	t_{13}	2/, see figure 2, see 4.4.1c	9, 10, 11	01	25		ns
SCLK rising edge to data valid hold time	t_{14}	2/, 3/, see figure 2, see 4.4.1c	9, 10, 11	01	5		ns
SCLK rising edge to data valid delay time	t_{15}	2/, 3/, see figure 2, see 4.4.1c	9, 10, 11	01		30	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{RFS}$ to SCLK falling edge hold time	t_{16}	2/, see figure 2, see 4.4.1c	9, 10, 11	01	30		ns
Bus relinquish time after rising edge of $\overline{RFS}$	t_{17}	2/, 4/, see figure 2, see 4.4.1c	9, 10, 11	01	0	30	ns
Bus relinquish time after rising edge of SCLK	t_{17A}	2/, 4/, see figure 2, see 4.4.1c	9, 10, 11	01	0	30	ns

1/ V_{DD} = +5 V ± 5%, AGND = DGND = 0 V, REF IN = +2.5 V.

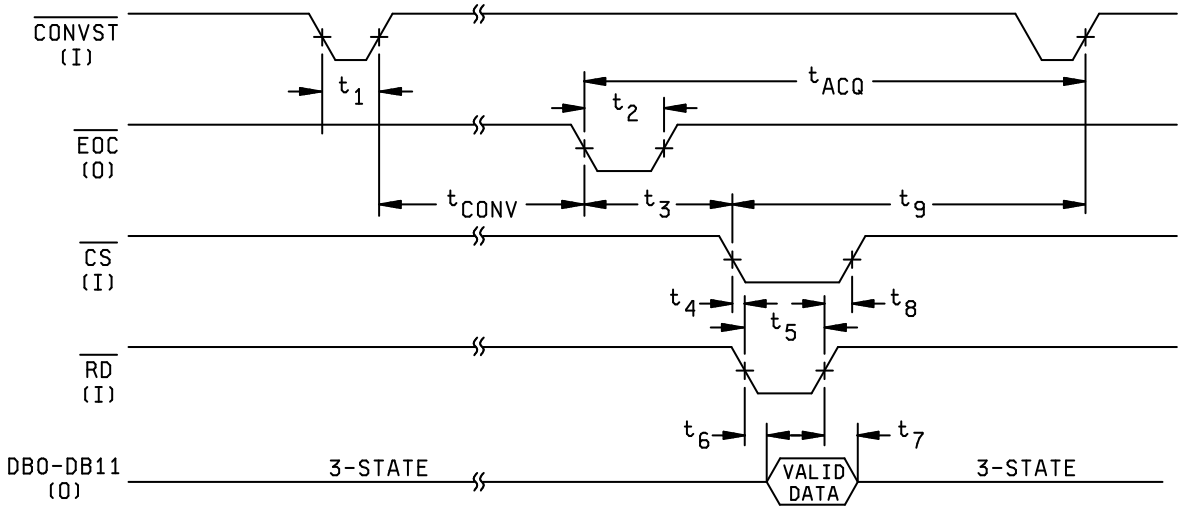
2/ All input signals are measured with tr = tf = 1 ns (10% to 90% of +5 V) and timed from a voltage level of +1.6 V.

3/ Defined as the time required for an output to cross 0.8 V or 2.4 V.

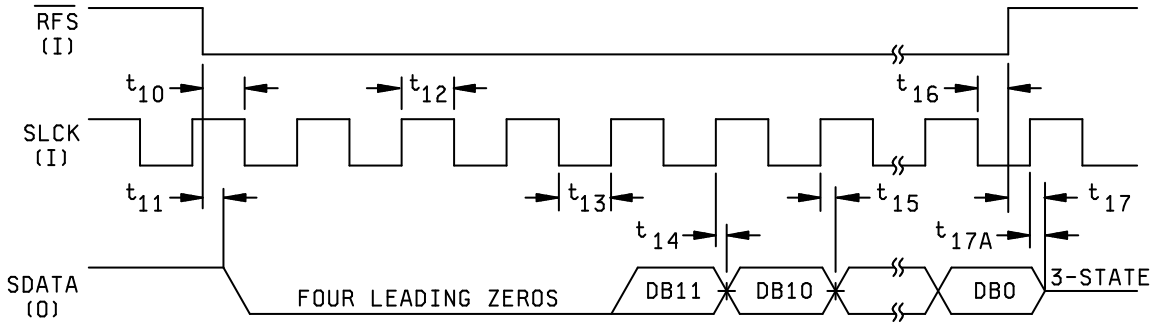
4/ These times are derived from the measured time taken by the data outputs to change 0.5 V. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. Therefore these timing characteristics are the true bus relinquish times and as such are independent of external bus loading capacitances.

Device type	01
Case outline	J and L
Terminal number	Terminal symbol
1	V_{DD}
2	$\overline{\text{STANDBY}}$
3	V_{IN2}
4	V_{IN1}
5	REF OUT/REF IN
6	AGND
7	MODE
8	DB11/LOW
9	DB10/LOW
10	DB9
11	DB8
12	DB7
13	DB6
14	DGND
15	DB5/SDATA
16	DB4/CSCLK
17	DB3/RFS
18	DB2
19	DB1
20	DB0(LSB)
21	$\overline{\text{RD}}$
22	$\overline{\text{CS}}$
23	$\overline{\text{EOC}}$
24	$\overline{\text{CONVST}}$

FIGURE 1. Terminal connections.



PARALLEL MODE TIMING DIAGRAM



SERIAL MODE TIMING DIAGRAM

FIGURE 2. Timing waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 4, 9, 10, and 11 shall be measured only for the initial test and after process or design changes that may effect these parameters and shall be guaranteed to the limits specified in table I.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 2, 3	1, 2, 3
Final electrical parameters (see 4.2)	1, 2, 3, 4 9, 10, 11, 1/	1, 2, 3, 4 9, 10, 11, 1/
Group A test requirements (see 4.4)	1, 2, 3, 4, 9, 10, 11	1, 2, 3, 4, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1	1
Group D end-point electrical parameters (see 4.4)	1	1
Group E end-point electrical parameters (see 4.4)	- - -	- - -

1/ PDA applies to subgroup 1.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-01-12

Approved sources of supply for SMD 5962-96846 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9684601QJA	3/	AD7892SQ-1/QML
5962-9684601QLA	24355	AD7892SQ-1/QML

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland