Mixed-Signal Control Processor with ARM Cortex-M4/M0 and 16-Bit ADCs

Silicon Anomaly List

ADSP-CM411F/412F/413F/416F/417F/418F/419F

ABOUT ADSP-CM411F/412F/413F/416F/417F/418F/419F SILICON ANOMALIES

These anomalies represent the currently known differences between revisions of the ADSP-CM411F/412F/413F/416F/417F/418F/419F product(s) and the functionality specified in the ADSP-CM411F/412F/413F/416F/417F/418F/419F data sheet(s) and the Hardware Reference book(s).

PRODUCT REVISIONS

A product revision letter with the form "-x" is branded on all parts. The implementation field bits <31:28> of the JTAG0_IDCODE register for the processor and <15:0> of the STATUSREG0 register for the Analog Front End (AFE) can be used to differentiate the revisions as shown below.

Product REVISION	JTAG0_IDCODE<31:28>	AFE_STATUSREG0<15:0>
C	0x2	0x3082
0.0	0x1	0x3080

ANOMALY LIST REVISION HISTORY

The following revision history lists the anomaly list revisions and major changes for each anomaly list revision.

Date	Anomaly List Revision	Data Sheet Revision	Additions and Changes
07/24/2017	C	PrB	Added Silicon Revision C Added Anomalies: 17000067, 17000080, 17000082, 17000083
06/27/2016	B	PrB	Added Anomalies: 17000063, 17000064, 17000066, 17000075, 17000076, 17000077 Revised Anomalies: 17000040, 17000041, 17000042, 17000043, 17000046, 17000049, 17000059
12/17/2015	A	PrA	Initial Version

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SUMMARY OF SILICON ANOMALIES

The following table provides a summary of ADSP-CM411F/412F/413F/416F/417F/418F/419F anomalies and the applicable product revision(s) for each anomaly.

No.	ID	Description	Rev 0.0	Rev C
1	17000033	SMC Byte Enable Signals Tri-State during Read Operations	x	.
2	17000035	Timer0 Status Interrupt Is Not Functional	x	.
3	17000036	JTAG May Inadvertently Enter EXTEST Mode	x	.
4	17000038	M0 DMA Debug Halt Is Not Functional	x	.
5	17000040	Internal LDO Increases VDD_INT	x	.
6	17000041	Incorrect VMU Voltage Trip Values	x	.
7	17000042	Oscillator Watch Dog Frequency Is Not Correct	x	.
8	17000043	ADC Reference Voltages Do Not Match Specification	x	.
9	17000044	DAC Output Current Limit Is Less Than Specified	x	.
10	17000046	ADC Auxiliary Bypass Mode Cannot Be Cleared By Register Write	x	.
11	17000048	Monitor ADC Conversion Time Exceeds Specification	x	.
12	17000049	FOCP_LATCH_0/1/2 Latches Have Incorrect Power-Up Value	x	.
13	17000050	CRC On Over Voltage and Under Voltage DAC Are Incorrect	x	.
14	17000055	Flash Security Features Are Not Fully Operational	x	.
15	17000057	PLL Malfunctions at Higher Frequencies	x	.
16	17000059	Security Keys for Devices Connected in a JTAG Chain Require Leading Zeroes	x	.
17	17000060	adi_rom_MemCopy() ROM API Leaves MDMA Enabled	x	.
18	17000063	System Watchpoint Units 3 and 4 Incorrectly Alias Master IDs	x	.
19	17000064	Back-to-back Writes to Internal SRAM May Be Lost	x	.
20	17000066	Manual ECC Error Diagnostic Testing of Flash Memory Is Not Functional	x	.
21	17000067	ADCC Frame Interrupt Status Register Must Be Cleared Between Frames	x	.
22	17000075	Primary ADC Conversions May Fail with Higher Delays Between Subsequent Conversions	x	.
23	17000076	First Conversion of ADC0 Fails after AFE Registers Are Accessed	x	.
24	17000077	FOCP Over Voltage and Under Voltage DAC Output Limited by Offset and Gain Errors	x	.
25	17000080	Logic Block Array (LBA) Combinatorial Mode Is Not Functional	x	.
26	17000082	Primary ADC Gain Error Correction Is Not Functional	.	x
27	17000083	Floating Point Saturation Unit Is Not Functional	x	.

Key: x = anomaly exists in revision
. = Not applicable

DETAILED LIST OF SILICON ANOMALIES

The following list details all known silicon anomalies for the ADSP-CM411F/412F/413F/416F/417F/418F/419F including a description, workaround, and identification of applicable product revisions.

1. 17000033 - SMC Byte Enable Signals Tri-State during Read Operations:

DESCRIPTION:
During SMC read operations, the byte enable signals (**SMC0_ABE0** and **SMC0_ABE1**) are tri-stated instead of being driven low. Therefore, when an 8-bit SMC write access is followed by a 16-bit or 32-bit read access, the read access may fail if the device requires active low byte enable signals during read operations.

WORKAROUND:
While interfacing with the external SRAM, the SRAM byte enable signals can be driven low during read operations using external logic as shown in the figure.

For SMC read operations, the **SMC0_AOE** signal is low. This drives the **SRAM_BHE** and **SRAM_BLE** signals low.
This external logic does not affect the SMC write operations, as the **SMC0_AOE** signal is high during write operations.

APPLIES TO REVISION(S):
0.0

2. 17000035 - Timer0 Status Interrupt Is Not Functional:

DESCRIPTION:
SYSBLK_SISTAT15.TIMER0_STAT bit is always read as 0. Therefore, Timer0 Status Interrupt is not functional.

WORKAROUND:
None.

APPLIES TO REVISION(S):
0.0

3. 17000036 - JTAG May Inadvertently Enter EXTEST Mode:

DESCRIPTION:
When performing a JTAG instruction register scan in multiple parts using the Pause-IR JTAG state, the JTAG controller erroneously enters the EXTEST state while in the Pause-IR state. The I/O pins may incorrectly drive the rest of the system for multiple JTAG cycles.

WORKAROUND:
Using Pause-IR to break the instruction scan into parts must be avoided. If Pause-IR is used, ensure the ADI JTAG Instruction Register does not have a value of b'00000 at the pause point. When in the Exit-IR state, if the ADI JTAG Instruction Register contains a value of b'00000, the JTAG clock must not be stopped. This leaves the I/O pins in an undetermined state until the JTAG clocks resume.

APPLIES TO REVISION(S):
0.0

4. 17000038 - M0 DMA Debug Halt Is Not Functional:

DESCRIPTION:
The M0 system's DMA debug logic that halts the DMA traffic does not function when a cross trigger unit halts. The DMA operations may continue in real-time during debug halt.

WORKAROUND:
None.

APPLIES TO REVISION(S):
0.0

5. 17000040 - Internal LDO Increases VDD_INT:

DESCRIPTION:
The internal LDO increases VDD_INT by 250 mV (approximately).

WORKAROUND:
Run the flash info block initialization code each time the flash info block is erased. This modifies the internal LDO register to adjust the voltage. It is available in the EVAL-CM41X-EZBRD/EVAL-CM41X-EZLITE evaluation platform Board Support Package (BSP). For more information about how to program the flash info block, refer to the IAR projects located in the **`ProgramInfoSpace`** directory.

APPLIES TO REVISION(S):
0.0

6. 17000041 - Incorrect VMU Voltage Trip Values:

DESCRIPTION:
The most significant bit of the voltage trim values for the VDD_EXT and VDD_INT power supply trip levels are not programmed at power-on-reset. As a result of this,

1. The VMU may detect a fault when the VDD_EXT and VDD_INT voltage levels are within specified range, and/or
2. The VMU may not detect the VDD_EXT and VDD_INT voltage levels operating outside the specified range.

WORKAROUND:
A software patch available in the **`startup.c`** file in the EVAL-CM41X-EZBRD/EVAL-CM41X-EZLITE evaluation platform Board Support Package (BSP) trims the VMU.

APPLIES TO REVISION(S):
0.0

7. 17000042 - Oscillator Watch Dog Frequency Is Not Correct:

DESCRIPTION:
The trim values for the Oscillator Watch Dog (OSCWD) are not loaded properly at boot time, resulting in an incorrect OSCWD frequency.

WORKAROUND:
Manually load the correct trim values for OSCWD as shown in the following code:

```
#define BITM_TEPADS_PCFG0_AUXTRMEN 0x00010000
*pREG_PADS1_PCFG0 |= BITM_TEPADS_PCFG0_AUXTRMEN;
*pREG_PADS1_PCFG0 &= ~BITM_TEPADS_PCFG0_AUXTRMEN;
```

APPLIES TO REVISION(S):
0.0

8. 17000043 - ADC Reference Voltages Do Not Match Specification:

DESCRIPTION:
The ADC reference voltages (VREF0, VREF1, and VREF2) are not calibrated to the specified 2.5 V.

WORKAROUND:
Use the actual ADC reference voltage values in ADC calculations, not the specified value.

APPLIES TO REVISION(S):
0.0

9. 17000044 - DAC Output Current Limit Is Less Than Specified:

DESCRIPTION:
The maximum DAC output current load specification is 5 mA. The actual DAC output current load is limited to 1 mA.

WORKAROUND:
None.

APPLIES TO REVISION(S):
0.0

10. 17000046 - ADC Auxiliary Bypass Mode Cannot Be Cleared By Register Write:

DESCRIPTION:
The auxiliary bypass bit cannot be cleared by a register write. If the ADC is set to enter auxiliary buffer bypass mode during operation, it cannot subsequently be reverted to non-bypass mode.

WORKAROUND:
If the auxiliary bypass bit is set, a soft reset is required to take the AFE out of auxiliary buffer bypass mode. The ADCC drivers include the **`adi_adcc_SetRegister()`** function to communicate with the AFE through the ADCC module. The ADCC drivers are furnished in the EVAL-CM41X-EZBRD/EZLITE evaluation platform Board Support Package (BSP).

The following is an example to issue the soft reset to the Analog Front End:

```
#include <drivers/adcc/adi_adcc.h>
ADI_ADCC_HANDLE handle;
ADI_ADCC_RESULT result;
static char space[ADI_ADCC_MEMORY];

result = adi_adcc_Open(0, space, &handle, false);
result = adi_adcc_SetRegister(handle, REG_USER_CONFIG_REG0_USERCFG, 0x00400000);
if (result == ADI_ADCC_SUCCESS)
{
   /* Success! */
}
else
{
   /* Failure! */
}
```

For more information about the APIs, refer to Device Driver documentation and example codes in the Board Support Package (BSP).

APPLIES TO REVISION(S):
0.0

11. 17000048 - Monitor ADC Conversion Time Exceeds Specification:

DESCRIPTION:
The minimum conversion time of the Monitor ADC (ADC0) is 600 ns (instead of 500 ns as per the specifications). Therefore, the maximum sampling rate of the ADC0 is 1.667 MSPS.

WORKAROUND:
None.

APPLIES TO REVISION(S):
0.0

12. 17000049 - FOCP_LATCH_0/1/2 Latches Have Incorrect Power-Up Value:

DESCRIPTION:
During power-up, the status bits of the **FOCP_LATCH_0**, **FOCP_LATCH_1**, and **FOCP_LATCH_2** registers are set to 1.

WORKAROUND:
Reading the **FOCP_LATCH_0**, **FOCP_LATCH_1**, and **FOCP_LATCH_2** registers after power-up clears the latches and allows normal operation. The ADCC software drivers include the **adi_adcc_GetRegister()** function to read the Analog Front End (AFE) registers through the ADCC module. The ADCC drivers are available in the EVAL-CM41X-EZBRD/EZLITE evaluation platform Board Support Package (BSP).

The following is an example to read from the **FOCP_LATCH_0, FOCP_LATCH_1, FOCP_LATCH_2** registers:

```
#include <drivers/adcc/adi_adcc.h>
ADI_ADCC_HANDLE handle;
ADI_ADCC_RESULT result;
uint32_t val;
static char space[ADI_ADCC_MEMORY];

result = adi_adcc_Open(0, space, &handle, false);
result = adi_adcc_GetRegister(handle, REG_USER_CONFIG_REG0_STATUSREG0, &val);
if (result == ADI_ADCC_SUCCESS)
{
   /* Success! */
}
else
{
   /* Failure! */
}
```

For more information about the APIs, refer to Device Driver documentation and example codes in the Board Support Package (BSP).

APPLIES TO REVISION(S):
0.0

13. 17000050 - CRC On Over Voltage and Under Voltage DAC Are Incorrect:

DESCRIPTION:
The CRC values on the Over Voltage (OV) DAC and Under Voltage (UV) DAC are incorrect.

WORKAROUND:
Do not use CRC on the OV DAC or UV DAC.

APPLIES TO REVISION(S):
0.0

14. 17000055 - Flash Security Features Are Not Fully Operational:

DESCRIPTION:
All the security features and key management processes may be exercised. However, flash memory contents are not fully protected by the security measures even if the part is locked. Security measures are planned to be fully functional in production silicon.

WORKAROUND:
None.

APPLIES TO REVISION(S):
0.0

15. 17000057 - PLL Malfunctions at Higher Frequencies:

DESCRIPTION:
The Clock Generation Unit (CGU) derives all the processor clocks from the phase-locked loop (PLL) voltage-controlled oscillator (VCO) output, called PLLCLK. When PLLCLK is configured to operate at frequencies above 600 MHz, it may malfunction.

WORKAROUND:
Configure the processor PLL such that the PLLCLK frequency does not exceed 600 MHz.
For example, consider an application that requires a CCLK:SYSCLK ratio of 240:96, with a SYS_CLKIN of 24 MHz. Set **`CGU_CTL.MSEL`** = 20 (480 MHz), and adjust the divisors by setting **`CGU_DIV.CSEL`** = 2 and **`CGU_DIV.SYSSEL`** = 5. This ensures that the PLL clock frequency does not exceed 600 MHz and the core clock/system clock frequency requirements are met.

APPLIES TO REVISION(S):
0.0

16. 17000059 - Security Keys for Devices Connected in a JTAG Chain Require Leading Zeroes:

DESCRIPTION:
When multiple ADSP-CM41x controllers are placed in a JTAG scan chain, the first part in the chain uses all 128 user debug security bits. For all other parts, zeroes are appended with respect to the position of the part in the scan chain. This issue occurs when security keys are provided through the TAPC security scan path.

For example, if three ADSP-CM41x parts are connected in series in the JTAG chain:
- The first part in the chain uses all 128 security bits ([127:0]).
- The second part in the chain uses 127 security bits ([127:1]). Bit 0 is set to 0.
- The third part in the chain uses 126 security bits ([127:2]). Bits 0 and 1 are both set to 0.

The example assumes that the parts are connected as individual JTAG controllers. The issue can also occur if multiple tap controllers are enabled in the scan chain, resulting in multiple zeroes from each part, and when non-ADSP-CM41x devices are included in the scan chain.

WORKAROUND:
Use memory-mapped writes through the DAP instead of the TAPC security scan path to provide security keys.

APPLIES TO REVISION(S):
0.0

17. 17000060 - adi_rom_MemCopy() ROM API Leaves MDMA Enabled:

DESCRIPTION:
The **`adi_rom_MemCopy()`** function in the ROM does not disable the MDMA channels upon completion. This may result in MDMA errors when the application attempts to reprogram the MDMA channels. This issue occurs with both ROM API and application code.

WORKAROUND:
Application code must manually disable the MDMA source and destination channels after calling the **`adi_rom_MemCopy()`** routine by setting **`DMA12_CFG.EN`** = 0 and **`DMA13_CFG.EN`** = 0.

APPLIES TO REVISION(S):
0.0

18. 17000063 - System Watchpoint Units 3 and 4 Incorrectly Alias Master IDs:

DESCRIPTION:

SWU3 and SWU4 only monitor the 6 LSBs of the SWU ID instead of 9 bits. As a result, the Master ID of the masters that share the same 6 LSBs, but have different MSBs, are incorrectly aliased. The SWUs cannot exactly track the master write to the FFT (monitored by SWU3) or SMC (monitored by SWU4).

Table 1 shows the SWU IDs with respect to various masters. The bits highlighted in the table are not monitored by the SWU. An "X" in the table indicates "don't care".

Table 1: SWU3 and SWU4 Master IDs

ID Bits [8:0]	Masters
00000X000	DMA4 (UART1_TX)
00000X001	DMA5 (UART1_RX)
00000X010	DMA6 (SPI1_TX/UART2_TX)
00000X011	DMA7 (SPI1_RX/UART2_RX)
00000X100	DMA8 (HAE_IN0/UART3_TX)
00000X101	DMA9 (HAE_OUT/UART3_RX)
00000X110	DMA10 (HAE_IN1/UART4_TX/SPORT0A)
00000X111	DMA11 (SPORT0B/UART4_RX)
01000X000	DMA12 (MDMA0_RD)
01000X001	DMA13 (MDMA0_WR)
10000X000	SINC
10000X001	ADCC0/DACC0
10000X010	FFT
11000X011	CONT_MST
11000X100	SUPER_MST

Table 2 shows the masters with ID bits [5:0] in common that are affected by this anomaly.

Table 2: SWU3 and SWU4 Aliased Master IDs

ID Bits [5:0]	Aliased Masters
00X000	DMA4 (UART1_TX), DMA12 (MDMA0_RD), SINC
00X001	DMA5 (UART1_RX), DMA13 (MDMA0_WR), ADCC0/DACC0
00X010	DMA6 (SPI1_TX/UART2_TX), FFT
00X011	DMA7 (SPI1_RX/UART2_RX), CONT_MST (M4 Controller)
00X100	DMA8 (HAE_IN0/UART3_TX), SUPER_MST (M0 Master (DMA0: SPI0_TX, DMA1: SPI0_RX))

WORKAROUND:

None.

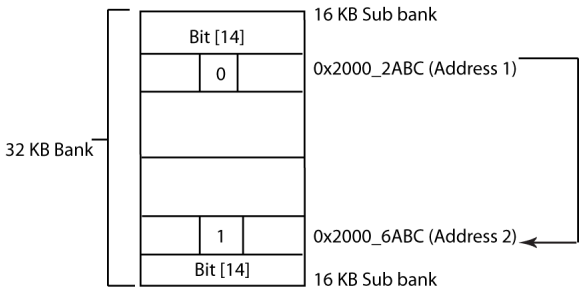
APPLIES TO REVISION(S):

0.0

19. 17000064 - Back-to-back Writes to Internal SRAM May Be Lost:

DESCRIPTION:
When back-to-back writes are performed to the same 32 KB bank of the internal SRAM, the first write may be lost if address bit 14 is different (all other bits are the same) on the second write.

The figure shows an example where address bit 14 is different for two accesses.



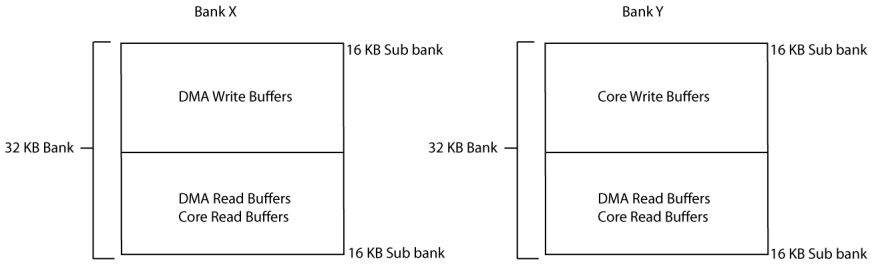
WORKAROUND:
The following workarounds utilize memory placement strategies, where two consecutive write addresses are not 16 KB apart.

For core-based accesses, the anomaly can occur on adjacent writes on the same bus between a local and global variable with addresses 16 KB apart and in the same bank.
In this case, the workaround is to use linker segments for code and variables to segregate them in a single 16 KB bank. If the total size is greater than 16 KB, place the variables in a separate 32 KB bank.

For DMA-based accesses, there are several cases to consider:

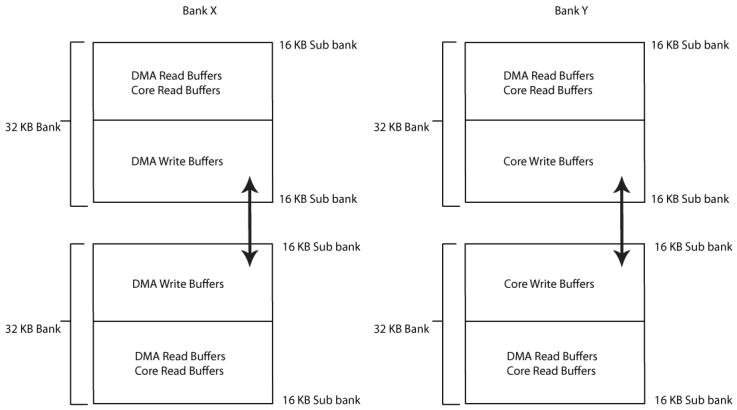
1. If DMA requires less than 16 KB of data space or DMA requires between 16 KB and 32 KB of data space, but less than 16 KB for DMA writes, the workaround is to place the segregated write buffers either at the top or bottom half of the 32 KB bank. Ensure that the writable DMA data regions and read-only DMA data regions are in different half banks. Core-writable variables may be placed in the other half of the 32 KB bank that contains read-only DMA regions.

   The figure shows the memory placement when DMA and Core write buffers are less than 16 KB.



2. If DMA requires more than 16 KB but less than 32 KB for writes, and DMA writes are a single linear stream, the workaround is to place the write data buffer in a single bank that has data in both halves of the bank. This issue does not exist in case of a linear addressed DMA.
   If DMA writes are not sequential and ordered and the DMA buffer requires more than 16 KB, the region must start from the higher half of the bank and continue into the lower half of the next bank. Core-writable variables may be placed in the other half of the 32 KB bank that contains read-only DMA regions.

   The figure shows the memory placement when DMA write buffers are between 16 KB and 32 KB.



3. If DMA requires more than 32 KB for writes, ensure that the writes are linear. This issue does not exist in case of a linear addressed DMA.

4. If Read-only DMA buffer has to be initialized, the code and variables of the function performing the initialization must reside in a separate 32 KB bank.

For DMA-based accesses, a high DMA latency value (**M4P_SRAM_CFG_DMAMAXLAT**) decreases the probability of writes getting lost when back-to-back writes are performed to SRAM.

APPLIES TO REVISION(S):
0.0

20. 17000066 - Manual ECC Error Diagnostic Testing of Flash Memory Is Not Functional:

DESCRIPTION:
The **FLC_CTL.MECC** bit is intended to induce a Flash ECC error. This bit is not functional.

WORKAROUND:
None.

APPLIES TO REVISION(S):
0.0

21. 17000067 - ADCC Frame Interrupt Status Register Must Be Cleared Between Frames:

DESCRIPTION:
When the **ADCC_NUMFRAMx** register is zero, the **ADCC_FISTAT.FINTx** bit is set after all the events related to a frame have completed.

When the **ADCC_NUMFRAMx** register is non-zero, the **ADCC_FISTAT.LFINTx** bit is also set after all the events related to all the frames (**ADCC_NUMFRAMx** + 1) have completed.

When the **ADCC_FISTATx** status bits are set, they must be cleared before the next ADCC timer trigger. Else, a trigger overrun error interrupt (**ADCC_ERR**) is generated, which stops subsequent sampling, leading to data loss. An event interrupt handler (**ADCC_TMR_EVT**) clears the **ADCC_FISTATx** status bits. This leads to a long sequence of actions (allowing the sampling to complete, DMA to drain, and handler to be invoked), which may prevent three to five ADC conversion slots in the frame from being used, especially at higher conversion rates.

WORKAROUND:
1. Use the **ADCC_TMRx_EVT** trigger master source to trigger a memory DMA transfer that writes to the ADCC system MMR space to clear the **ADCC_FISTAT.FINTx** bits. This removes the core from processing the event and automates hardware handling for it.
2. Periodically update the **ADCC_NUMFRAMx** register to prevent the **ADCC_FISTAT.LFINTx** bit from getting set. The **ADCC_NUMFRCNT** register increments until it reaches the value in the **ADCC_NUMFRAMx** register, upon which the **ADCC_FISTAT.LFINTx** bit is set. Read the **ADCC_NUMFRCNT** register periodically, and update the **ADCC_NUMFRAMx** register to a value that is less than the value read. For example, perform this check and adjustment in the ADCC timer event handler triggered by assertion of the **ADCC_FISTAT.FINTx** bit. When the **ADCC_NUMFRAMx** register is non-zero, the delay incurred to clear the **ADCC_FISTAT.FINTx** bit will not cause an overflow error.

APPLIES TO REVISION(S):
0.0

22. 17000075 - Primary ADC Conversions May Fail with Higher Delays Between Subsequent Conversions:

DESCRIPTION:
At room temperature, primary ADC (ADC1 and ADC2) conversion fails when the delay between the subsequent conversions is greater than 2.8 ms.

This issue can occur with single-channel conversions or simultaneous conversions. In the case of simultaneous sampling conversions, only the first conversion fails.

WORKAROUND:
The following workarounds can be used:
1. Place an additional NOP between the conversions.
2. Set the delay between the conversions to less than 2.8 ms on the primary ADCs.

APPLIES TO REVISION(S):
0.0

23. 17000076 - First Conversion of ADC0 Fails after AFE Registers Are Accessed:

DESCRIPTION:
When a read/write operation is performed on the **AFE_STATUSREG0**, **AFE_STATUSREG1**, or **AFE_USERCFG** registers, the first conversion on ADC0 fails. For example, the AFE Initialization after power-on-reset is done via the ADC0 interface (one time initialization). If ADC0 is used in the application, the first conversion fails. This issue also occurs when FOCP status reading or DAC selection is performed, followed by ADC0 conversion.

WORKAROUND:
Discard the first sample or perform a dummy access on ADC0.

APPLIES TO REVISION(S):
0.0

24. 17000077 - FOCP Over Voltage and Under Voltage DAC Output Limited by Offset and Gain Errors:

DESCRIPTION:
The following errors limit the output of the Fast Over Current Protection (FOCP) Under Voltage (UV)/Over Voltage (OV) DACs:

- OV/UV DAC offset error (**OFFSET_ERROR**): 40±8 mV
- OV/UV full scale error (**FULLSCALE_ERROR**): -5±1 mV
- Gain error (**GAIN_ERROR = FULLSCALE_ERROR - OFFSET_ERROR**): -45±9 mV

WORKAROUND:
Set the input to the 8-bit OV and UV DACs based on the following equation:

```
OV/UV DAC_OUTPUT = OFFSET_ERROR + (DAC_INPUT/256)*(3.0 + GAIN_ERROR)
```

In the above equation, **DAC_INPUT** is the 8-bit digital input to the OV/UV DAC from the DAC controller, and **DAC_OUTPUT** is the analog output from the OV/UV DAC.

APPLIES TO REVISION(S):
0.0

25. 17000080 - Logic Block Array (LBA) Combinatorial Mode Is Not Functional:

DESCRIPTION:
The **SYSBLK0_ENG_MODE_CFG0.LBA_COMB_MODE** bit is used to enable the LBA combinatorial mode. This bit is not functional.

WORKAROUND:
None.

APPLIES TO REVISION(S):
0.0

26. 17000082 - Primary ADC Gain Error Correction Is Not Functional:

DESCRIPTION:
Primary ADC (ADC1 and ADC2) gain error correction is not functional. This feature is disabled. The primary ADC gain error is between -3% to -5%.

The ADC input voltage is less than the full scale voltage of 3 V. It varies from device to device. It also varies between the three primary ADC Muxes within a device.

WORKAROUND:
Calibrate the gain error for each device on the primary ADC Muxes (ADC1 MUX A, ADC1 MUX B, ADC1 MUX C, ADC2 MUX A, ADC2 MUX B, and ADC2 MUX C) through software, if required.

APPLIES TO REVISION(S):
C

27. 17000083 - Floating Point Saturation Unit Is Not Functional:

DESCRIPTION:
The Floating Point Saturation (FSAT) unit is used to implement a 32-bit floating point saturation. This unit is not functional.

WORKAROUND:
None.

APPLIES TO REVISION(S):
0.0