REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
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TITLE
MICROCIRCUIT, LINEAR, 1.2 GHz, CLOCK FANOUT BUFFER, MONOLITHIC SILICON

SIZE	CODE IDENT. NO.	DWG NO.
A	16236	V62/13626

REV

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 1.2 GHz clock fanout buffer microcircuit, with an operating temperature range of -55°C to +105°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/13626	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD9508-EP	1.2 GHz clock fanout buffer

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	24	MO-220-WGGD	Quad lead frame chip scale package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD}) .... 3.6 V
Maximum digital input voltage .... -0.5 V to V_{DD} + 0.5 V
CLK to $\overline{CLK}$ .... -0.5 V to V_{DD} + 0.5 V
Maximum digital output voltage .... -0.5 V to V_{DD} + 0.5 V
Storage temperature range (T_{STG}) .... -65°C to +150°C
Lead temperature (soldering, 10 seconds) .... +300°C
Junction temperature range (T_J) .... +150°C

1.4 Recommended operating conditions. 2/

Supply voltage (V_{DD}) .... 2.5 V
Operating temperature range (T_A) .... -55°C to +105°C

1.5 Thermal characteristics.

Thermal characteristic 3/	Symbol	Limit 4/	Unit
Thermal resistance, junction-to-ambient per JEDEC JESD51-2 (still air)	θ_{JA}	43.5	°C/W
Thermal resistance, junction-to-ambient , 1.0 m/second airflow per JEDEC JESD51-6 (moving air)	θ_{JMA}	40	°C/W
Thermal resistance, junction-to-ambient , 2.5 m/second airflow per JEDEC JESD51-6 (moving air)	θ_{JMA}	38.5	°C/W
Thermal resistance, junction-to-board per JEDEC JESD51-8 (still air)	θ_{JB}	16.2	°C/W
Junction to case thermal resistance (die-to-heat sink) per MIL-STD-883, method 1012	θ_{JC}	7.1	°C/W
Characterization parameter, junction-to-top of package per JEDEC JESD51-2 (still air)	ψ_{JT}	0.33	°C/W

1/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user's risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

3/ The exposed pad on the bottom of the package must be soldered to ground (V_{SS}) to achieve the specified thermal performance.

4/ Results are from simulations. The printed circuit board (PCB) is a JEDEC multilayer type.
Thermal performance for actual applications requires careful inspection of the conditions in the application to determine whether they are similar to those assumed in these calculations.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

EIA/JESD 51-2a	-	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
EIA/JEDEC 51-6	-	Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)
EIA/JESD 51-8	-	Integrated Circuits Thermal Test Method Environment Conditions – Junction-to-Board
JEDEC PUB 95	-	Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer’s part number as shown in 6.3 herein and as follows:

A. Manufacturer’s name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer’s part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Power supply current and temperature conditions.							
Supply voltage	V_S		-55°C to +105°C	01	2.375	2.625	V
			+25°C		2.5 typical		
Current consumption.							
Low voltage differential signaling (LVDS) configuration		Input clock at 1200 MHz, differential mode; all LVDS output drivers at 1200 MHz	-55°C to +105°C	01		148	mA
			+25°C		132 typical		
		Input clock at 800 MHz, differential mode; all LVDS output drivers at 200 MHz	-55°C to +105°C			108	
			+25°C		96 typical		
High speed transceiver logic (HSTL) configuration		Input clock at 1200 MHz, differential mode; all HSTL output drivers at 1200 MHz	-55°C to +105°C	01		175	mA
			+25°C		156 typical		
		Input clock at 491.52 MHz, differential mode; all HSTL output drivers at 491.52 MHz	-55°C to +105°C			136	
			+25°C		121 typical		
		Input clock at 122.88 MHz, differential mode; all HSTL output drivers at 122.88 MHz	-55°C to +105°C			96	
			+25°C		86 typical		
Complementary metal oxide semiconductor (CMOS) configuration		Input clock at 1200 MHz, differential mode; all CMOS output drivers at 200 MHz, C_L = 10 pF	-55°C to +105°C	01		159	mA
			+25°C		142 typical		
		Input clock at 800 MHz, differential mode; all CMOS output drivers at 200 MHz, C_L = 10 pF	-55°C to +105°C			132	
			+25°C		118 typical		
		Input clock at 100 MHz, differential mode; all CMOS output drivers at 100 MHz, C_L = 10 pF	-55°C to +105°C			85	
			+25°C		76 typical		
Full power down			-55°C to +105°C	01		8	mA
			+25°C		4.6 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Power supply current and temperature conditions - continued.							
Temperature.							
Ambient temperature range	T_A			01	-55	+105	°C
					+25 typical		
Junction temperature	T_J	Junction temperature above 115°C can degrade performance, but no damage should occur unless the absolute temperature is exceeded.		01		135	°C
Clock input and output dc specifications.							
Clocks inputs (Differential mode).							
Input frequency	f_{IN}	Differential input	-55°C to +105°C	01	0	1200	MHz
Input sensitivity		As measured with a differential probe; jitter performance improves with higher slew rates (greater voltage swing)	-55°C to +105°C	01	360	2200	mV_{PP}
Input common mode voltage	V_{ICM}	Input pins are internally self biased, which enables ac coupling	-55°C to +105°C	01	0.95	1.15	V
			+25°C		1.05 typical		
Input voltage offset	V_{IO}		+25°C	01	30 typical		mV
DC coupled input common mode range	V_{CMR}	Allowable common mode voltage range when dc coupled	-55°C to +105°C	01	0.58	1.67	V
Pulse width low	t_{PWL}		-55°C to +105°C	01	417		ps
Pulse width high	t_{PWH}		-55°C to +105°C	01	417		ps
Input resistance (differential)	R_{IN}		-55°C to +105°C	01	5.0	9	kΩ
			+25°C		7 typical		
Input capacitance	C_{IN}		+25°C	01	2 typical		pF
Input bias current (each pin)	I_{IB}	Full input swing	-55°C to +105°C	01	100	400	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Clock input and output dc specifications – continued.							
CMOS clock mode single ended.							
Input frequency	f_{IN}		-55°C to +105°C	01		250	MHz
Input voltage high	V_{IH}		-55°C to +105°C	01	V_{DD} – 0.4		V
Input voltage low	V_{IL}		-55°C to +105°C	01		0.4	V
Input current high	I_{INH}		+25°C	01	1 typical		µA
Input current low	I_{INL}		+25°C	01	-142 typical		µA
Input capacitance	C_{IN}		+25°C	01	2 typical		pF
LVDS clock inputs. Termination = 100 Ω differential (OUTx, $\overline{OUTx}$).							
Output frequency	f_{OUT}		-55°C to +105°C	01		1200	MHz
Differential output voltage	V_{OD}	V_{OH} – V_{OL} measurement across a differential pair at the default amplitude settling with output driver not toggling; see figure 3 for variation over frequency.	-55°C to +105°C	01	247	454	mV
			+25°C		375 typical		
Delta differential output voltage	ΔV_{OD}	Absolute value of the difference between V_{OD} when the normal output is high versus when the complementary output is high	-55°C to +105°C	01		50	mV
Offset voltage	V_{OS}	(V_{OH} + V_{OL}) / 2 across a differential pair	-55°C to +105°C	01	1.125	1.375	V
			+25°C		1.18 typical		
Delta offset voltage	ΔV_{OS}	Absolute value of the difference between V_{OS} when the normal output is high versus when the complementary output is high.	-55°C to +105°C	01		50	mV
Short circuit current	I_{SA}, I_{SB}	Each pin (output shorted to GND)	-55°C to +105°C	01		24	mA
			+25°C		13.6 typical		
LVDS duty cycle		Up to 750 MHz input	-55°C to +105°C	01	45	55	%
		750 MHz to 1200 MHz input			39	61	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Clock input and output dc specifications – continued.							
HSTL clock inputs. Termination = 100 Ω differential; default amplitude setting.							
Output frequency	f_{OUT}		-55°C to +105°C	01		1200	MHz
Differential output voltage	V_O	$V_{OH} – V_{OL}$ with output driver static	-55°C to +105°C	01	859	978	mV
			+25°C		925 typical		
Common mode output voltage	V_{OCM}	$(V_{OH} + V_{OL})/2$ with output driver static	-55°C to +105°C	01	905	971	mV
			+25°C		940 typical		
HSTL duty cycle		Up to 750 MHz input	-55°C to +105°C	01	45	55	%
		750 MHz to 1200 MHz input			40	60	
CMOS clock outputs. Single ended; termination = open; OUTx and $\overline{\text{OUTx}}$ in phase.							
Output frequency	f_{OUT}	10 pF load per output; see figure 4 for output swing versus frequency	-55°C to +105°C	01		250	MHz
Output voltage	V_{OH}	1 mA load	-55°C to +105°C	01	1.7		V
	V_{OL}					0.1	
	V_{OH}	10 mA load			1.2		
	V_{OL}					0.6	
	V_{OH}	10 mA load (2 x CMOS mode)			1.45		
	V_{OL}					0.35	
CMOS duty cycle		Up to 250 MHz	-55°C to +105°C	01	45	55	%

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Output driver timing characteristics.							
LVDS outputs. Termination = 100 Ω differential, 1 X LVDS.							
Output rise/fall time	t_R, t_F	20% x 80% measured differentially	-55°C to +105°C	01		192	ps
			+25°C		152 typical		
Propagation delay, clock to LVDS output	t_{PD}		-55°C to +105°C	01	1.52	2.49	ns
			+25°C		2.01 typical		
Propagation delay, clock to LVDS output temperature coefficient	t_{PD}		+25°C	01	2.8 typical		ps/°C
Output skew, all LVDS outputs. 3/							
On the same part			-55°C to +105°C	01		48	ps
Across multiple parts		Assumes same temperature and supply; takes into account worst case propagation delay due to worst case process variation	-55°C to +105°C	01		781	ps
HSTL outputs. Termination = 100 Ω differential, 1 X HSTL.							
Output rise/fall time	t_R, t_F	20% x 80% measured differentially	-55°C to +105°C	01		154	ps
			+25°C		118 typical		
Propagation delay, clock to HSTL output	t_{PD}		-55°C to +105°C	01	1.55	2.56	ns
			+25°C		2.05 typical		
Propagation delay, clock to HSTL output temperature coefficient	t_{PD}		+25°C	01	2.9 typical		ps/°C
Output skew, all HSTL outputs. 3/							
On the same part			-55°C to +105°C	01		59	ps
Across multiple parts		Assumes same temperature and supply; takes into account worst case propagation delay due to worst case process variation	-55°C to +105°C	01		825	ps

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Output driver timing characteristics - continued.							
CMOS outputs.							
Output rise/fall time	t_R, t_F	20% x 80%, C_L = 10 pF	-55°C to +105°C	01		1.47	ps
			+25°C		1.18 typical		
Propagation delay, clock to CMOS output	t_{PD}	10 pF load	-55°C to +105°C	01	1.98	3.14	ns
			+25°C		2.56 typical		
Propagation delay, clock to CMOS output temperature coefficient	t_{PD}		+25°C	01	3.3 typical		ps/°C
Output skew, all CMOS outputs. 3/							
On the same part			-55°C to +105°C	01		112	ps
Across multiple parts		Assumes same temperature and supply; takes into account worst case propagation delay due to worst case process variation	-55°C to +105°C	01		965	ps
Output logic skew. 3/ CMOS load = 10 pF and LVDS load = 100 Ω.							
LVDS outputs and HSTL outputs		Outputs on the same device; assumes worst case output combination	-55°C to +105°C	01		119	ps
			+25°C		77 typical		
LVDS outputs and CMOS outputs		Outputs on the same device; assumes worst case output combination	-55°C to +105°C	01		708	ps
			+25°C		497 typical		
HSTL outputs and CMOS outputs		Outputs on the same device; assumes worst case output combination	-55°C to +105°C	01		628	ps
			+25°C		424 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Logic inputs.							
Logic inputs. ($\overline{RESET}$, $\overline{SYNC}$, IN_SEL).							
Input high voltage	V_{IH}	2.5 V supply voltage operation	-55°C to +105°C	01	1.7		V
Input low voltage	V_{IL}	2.5 V supply voltage operation	-55°C to +105°C	01		0.7	V
Input current	I_{INH}, I_{INL}		-55°C to +105°C	01	-300	100	µA
Input capacitance	C_{IN}		+25°C	01	2 typical		pF
Serial port specification. Serial peripheral interface (SPI) mode.							
Chip select ($\overline{CS}$). $\overline{CS}$ has an internal 35 kΩ pull up resistor.							
Input voltage	V_{IN}	Logic 1	-55°C to +105°C	01	V_{DD} – 0.4		V
		Logic 0				0.4	
Input current	I_{IN}	Logic 1	+25°C	01	-4 typical		µA
		Logic 0			-85 typical		
Input capacitance	C_{IN}		+25°C	01	2 typical		pF
Serial clock (SCLK). SCLK has an internal 35 kΩ pull up resistor.							
Input voltage	V_{IN}	Logic 1	-55°C to +105°C	01	V_{DD} – 0.4		V
		Logic 0				0.4	
Input current	I_{IN}	Logic 1	+25°C	01	70 typical		µA
		Logic 0			13 typical		
Input capacitance	C_{IN}		+25°C	01	2 typical		pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Serial port specification – continued. SPI mode.							
Serial data input and output (SDIO) (input).							
Input voltage	V_{IN}	Logic 1	-55°C to +105°C	01	V_{DD} – 0.4		V
		Logic 0				0.4	
Input current	I_{IN}	Logic 1	+25°C	01	-1 typical		µA
		Logic 0			-1 typical		
Input capacitance	C_{IN}		+25°C	01	2 typical		pF
Serial data input and output (SDIO) output.							
Output voltage	V_{OUT}	Logic 1, 1 mA load current	-55°C to +105°C	01	V_{DD} – 0.4		V
		Logic 0, 1 ma load current				0.4	
Serial data output (SDO) output.							
Output voltage	V_{OUT}	Logic 1, 1 mA load current	-55°C to +105°C	01	V_{DD} – 0.4		V
		Logic 0, 1 mA load current				0.4	
Timing.							
SCLK clock rate	$1/t_{CLK}$		-55°C to +105°C	01		30	MHz
SCLK pulse width high	t_{HIGH}		-55°C to +105°C	01	4.6		ns
SCLK pulse width low	t_{LOW}		-55°C to +105°C	01	3.5		ns
SDIO to SCLK setup	t_{DS}		-55°C to +105°C	01	2.9		ns
SCLK to SDIO hold	t_{DH}		-55°C to +105°C	01	0		ns
SCLK to valid SDIO and SDO	t_{DV}		-55°C to +105°C	01		15	ns
$\overline{CS}$ to SCLK setup	tS		-55°C to +105°C	01	3.4		ns
$\overline{CS}$ to SCLK hold	t_C		-55°C to +105°C	01	0		ns
$\overline{CS}$ minimum pulse width high			-55°C to +105°C	01	3.4		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Serial port specifications. Inter-integrated circuit (I^2C) mode.							
Serial data (SDA), serial clock (SCL) inputs. SDA and SCL have internal 80 kΩ pull up resistors.							
Input voltage	V_{IN}	Logic 1	-55°C to +105°C	01	V_{DD} – 0.4		V
		Logic 0				0.4	
Input current	I_{IN}	V_{IN} = 10% to 90%	-55°C to +105°C	01	-40	0	µA
Hysteresis of schmitt trigger inputs			-55°C to +105°C	01	150		mV
SDA output.							
Output logic 0 voltage		I_O = 3 mA	-55°C to +105°C	01		0.4	V
Output fall time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		10 pF ≤ C_b ≤ 400 pF	-55°C to +105°C	01		250	ns
Timing.							
SCL clock rate			-55°C to +105°C	01		400	kHz
Bus free time between a stop and start condition	t_{BUF}		-55°C to +105°C	01	1.3		µs
Repeated start condition setup time	$t_{SU;STA}$		-55°C to +105°C	01		0.6	µs
Repeated start condition hold time	$t_{HD;STA}$	After this period, the first clock pulse is generated	-55°C to +105°C	01	0.6		µs
Stop condition setup time	$t_{SU;STO}$		-55°C to +105°C	01	0.6		µs
Low period of SCL clock	t_{LOW}		-55°C to +105°C	01	1.3		µs
High period of SCL clock	t_{HIGH}		-55°C to +105°C	01	0.6		µs
Data setup time	$t_{SU;DAT}$		-55°C to +105°C	01	100		ns
Data hold time	$t_{HD;DAT}$		-55°C to +105°C	01	0	0.9	µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
External resistor values for pin strapping mode.							
External resistors. Using 10% tolerance resistor.							
Voltage level 0		Pull down to ground	+25°C	01	820 typical		Ω
Voltage level 1		Pull down to ground	+25°C	01	1.8 typical		kΩ
Voltage level 2		Pull down to ground	+25°C	01	3.9 typical		kΩ
Voltage level 3		Pull down to ground	+25°C	01	8.2 typical		kΩ
Voltage level 4		Pull up to V_{DD}	+25°C	01	820 typical		Ω
Voltage level 5		Pull up to V_{DD}	+25°C	01	1.8 typical		kΩ
Voltage level 6		Pull up to V_{DD}	+25°C	01	3.9 typical		kΩ
Voltage level 7		Pull up to V_{DD}	+25°C	01	8.2 typical		kΩ
Clock output additive phase noise.							
Additive phase noise, clock to HSTL or LVDS.							
CLK = 1200 MHz, OUTx = 1200 MHz. Input slew rate > 1 V/ns.							
Divide ratio = 1		10 Hz offset	+25°C	01	-90 typical		dBc/Hz
		100 Hz offset			-101 typical		
		1 kHz offset			-110 typical		
		10 kHz offset			-117 typical		
		100 kHz offset			-135 typical		
		1 MHz offset			-144 typical		
		10 MHz offset			-149 typical		
		100 MHz offset			-150 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Clock output additive phase noise – continued.							
Additive phase noise, clock to HSTL, LVDS or CMOS.							
CLK = 625 MHz, OUTx = 125 MHz. Input slew rate > 1 V/ns.							
Divide ratio = 5		10 Hz offset	+25°C	01	-114 typical		dBc/Hz
		100 Hz offset			-125 typical		
		1 kHz offset			-133 typical		
		10 kHz offset			-141 typical		
		100 kHz offset			-159 typical		
		1 MHz offset			-162 typical		
		10 MHz offset			-163 typical		
		20 MHz offset			-163 typical		
Additive phase noise, clock to HSTL or LVDS.							
CLK = 491.52 MHz, OUTx = 491.52 MHz. Input slew rate > 1 V/ns.							
Divide ratio = 1		10 Hz offset	+25°C	01	-100 typical		dBc/Hz
		100 Hz offset			-111 typical		
		1 kHz offset			-120 typical		
		10 kHz offset			-127 typical		
		100 kHz offset			-146 typical		
		1 MHz offset			-153 typical		
		10 MHz offset			-153 typical		
		20 MHz offset			-153 typical		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits Min	Limits Max	Unit
Clock output additive time jitter.							
LVDS output additive time jitter.							
CLK = 622.08 MHz, Outputs = 622.08 MHZ		BW = 12 kHz to 20 MHz	+25°C	01	41 typical		fs rms
		BW = 20 kHz to 80 MHz			70 typical		
		BW = 50 kHz to 80 MHz			69 typical		
CLK = 622.08 MHz, Outputs = 155.52 MHZ		BW = 12 kHz to 20 MHz	+25°C	01	93 typical		fs rms
		BW = 20 kHz to 80 MHz			144 typical		
		BW = 50 kHz to 80 MHz			142 typical		
CLK = 125 MHz, Outputs = 125 MHZ		BW = 12 kHz to 20 MHz	+25°C	01	105 typical		fs rms
		BW = 20 kHz to 80 MHz			209 typical		
		BW = 50 kHz to 80 MHz			206 typical		
CLK = 400 MHz, Outputs = 50 MHZ		BW = 12 kHz to 20 MHz	+25°C	01	184 typical		fs rms
HSTL output additive time jitter.							
CLK = 622.08 MHz, Outputs = 622.08 MHZ		BW = 12 kHz to 20 MHz	+25°C	01	41 typical		fs rms
		BW = 100 kHz to 20 MHz			56 typical		
		BW = 20 kHz to 80 MHz			72 typical		
		BW = 50 kHz to 80 MHz			70 typical		
CLK = 622.08 MHz, Outputs = 155.52 MHZ		BW = 12 kHz to 20 MHz	+25°C	01	76 typical		fs rms
		BW = 100 kHz to 20 MHz			87 typical		
		BW = 20 kHz to 80 MHz			158 typical		
		BW = 50 kHz to 80 MHz			156 typical		
CMOS output additive time jitter.							
CLK = 100 MHz, Outputs = 100 MHZ		BW = 12 kHz to 20 MHz	+25°C	01	91 typical		fs rms

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, typical values are given for V_S = 2.5 V and T_A = +25°C, minimum and maximum values are given over the full supply voltage range (V_{DD} = 2.5 V ±5 %) and temperature range (T_A = -55°C to +105°C); input slew rate $>$ 1 V/ns.

3/ Output skew is the difference between any two similar delay paths while operating at the same voltage and temperature.

Case X

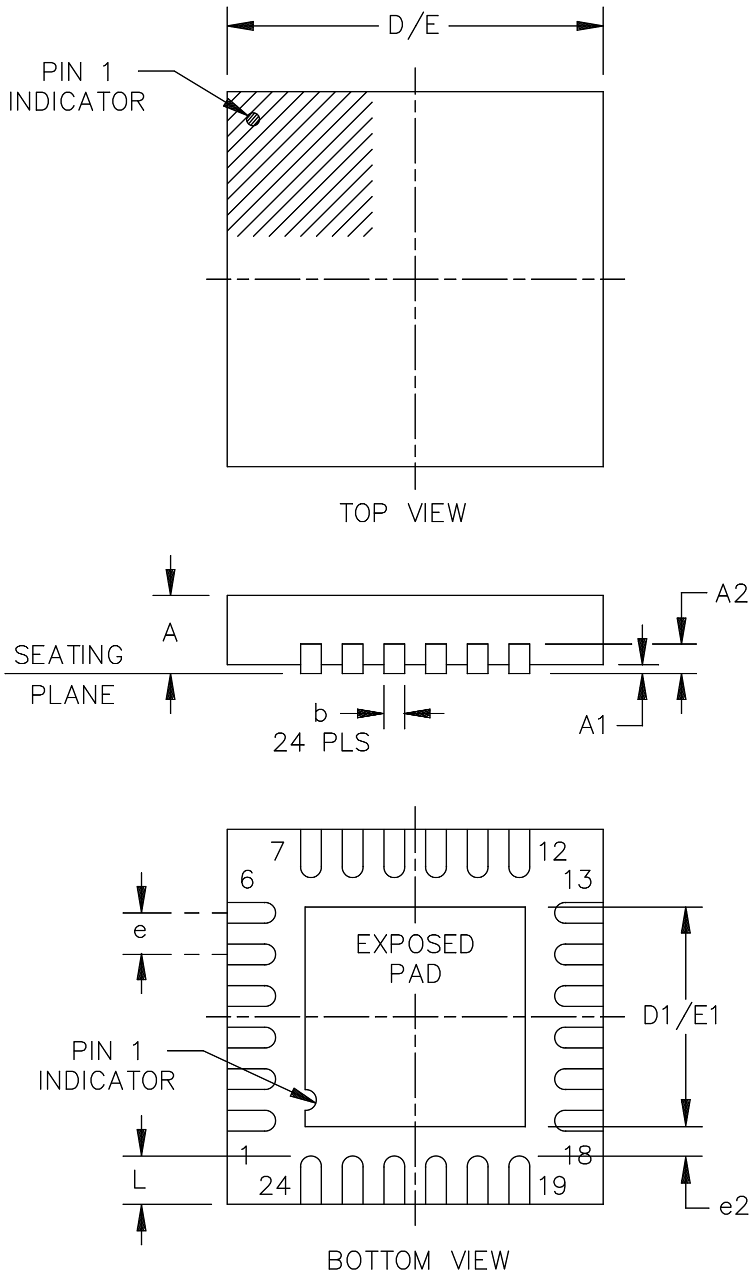

FIGURE 1. Case outline.

Case X – continued.

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Medium	Maximum	Minimum	Medium	Maximum
A	0.027	0.029	0.031	0.70	0.75	0.80
A1	0.0007 NOM	---	0.001	0.02 NOM	---	0.05
A2	0.007 REF			0.20 REF		
b	0.007	0.009	0.011	0.18	0.25	0.30
D/E	0.153	0.157	0.161	3.90	4.00	4.10
D1/E1	0.096	0.098	0.104	2.45	2.50	2.65
e	0.019 BSC			0.50 BSC		
e2	0.009	---	---	0.25	---	---
L	0.011	0.015	0.019	0.30	0.40	0.50

NOTES:
1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-220-WGGD.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	$\overline{CS}$/S2	Chip select ($\overline{CS}$)/pin programming (S2). This dual purpose pin is controlled by the PROG_SEL pin. In SPI mode, $\overline{CS}$ is an active low CMOS input. When programming the device in SPI mode, $\overline{CS}$ must be held low. In systems with two or more subject devices, $\overline{CS}$ enables individual programming of each device. In pin programming mode, S2 is hardwired with a resistor to either V_{DD} or ground. The resistor value biasing determine the channel divider value for the outputs on pin 11 and pin 12.
2	OUT0	LVDS/HSTL differential output or single ended CMOS output.
3	$\overline{OUT0}$	Complementary LVDS/HSTL differential output or single ended CMOS output.
4	SDO/S3	SPI serial data output (SDO)/pin programming (S3). This dual purpose pin is controlled by the PROG_SEL pin. In SPI mode, SDO can be configured as an output to read back the internal register settings. In pin programming mode, S3 is hardwired with a resistor to either V_{DD} or ground. The resistor value and resistor biasing determine the channel divider value for the outputs on pin 16 and pin 17.
5	EXT_CAP0	Node for external decoupling capacitor for low voltage dropout (LDO) regulator. Tie this pin with a 0.47 μF capacitor to ground.
6	V_{DD}	Power supply (2.5 V operation).
7	OUT1	LVDS/HSTL differential output or single ended CMOS output.
8	$\overline{OUT1}$	Complementary LVDS/HSTL differential output or single ended CMOS output.
9	S4	The S4 pin is used in pin programming mode only. (The PROG_SEL pin determines which programming mode is used.) S4 is hardwired with a resistor to either V_{DD} or ground. The resistor value and resistor biasing determine the output logic levels used for the outputs on pin 2, pin 3, pin 7, and pin 8.
10	S5	The S5 pin is used in pin programming mode only. (The PROG_SEL pin determines which programming mode is used.) S5 is hardwired with a resistor to either V_{DD} or ground. The resistor value and resistor biasing determine the output logic levels used for the outputs on pin 11, pin 12, pin 16, and pin 17.

FIGURE 2. Terminal connections.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
11	OUT2	LVDS/HSTL differential output or single ended CMOS output.
12	$\overline{\text{OUT2}}$	Complementary LVDS/HSTL differential output or single ended CMOS output.
13	V_{DD}	Power supply (2.5 V operation).
14	EXT_CAP1	Node for external decoupling capacitor for LDO regulator. Tie this pin with a 0.47 μF capacitor to ground.
15	PROG_SEL	Three state CMOS input. Pin 15 selects the device programming interface used by the device: SPI, I^2C, or pin programming.
16	OUT3	LVDS/HSTL differential output or single ended CMOS output.
17	$\overline{\text{OUT3}}$	Complementary LVDS/HSTL differential output or single ended CMOS output.
18	$\overline{\text{RESET}}$	Device reset (CMOS input, active low). When this pin is asserted, the internal register settings revert to their default state after the $\overline{\text{RESET}}$ pin is released. $\overline{\text{RESET}}$ also powers down the device when an active low signal is applied to the pin. The $\overline{\text{RESET}}$ pin as an internal 24 kΩ pull up resistor.
19	SCLK/SCL/S0	SPI serial clock (SCLK)/I^2C serial clock (SCL)/ Pin programming (SO). This multipurpose pin is controlled by the PROG_SEL pin. In SPI mode, SCLK is the serial clock. In I^2C mode, SCL is the serial clock. In pin programming mode, S0 is hardwired with a resistor to either V_{DD} or ground. The resistor value and resistor biasing determine the channel divider value for the outputs on pin 2 and pin 3.
20	$\overline{\text{SYNC}}$	Clock synchronization (active low). When this pin is asserted, the output drivers are held static and then synchronized on a low to high transition of this pin. The $\overline{\text{SYNC}}$ pin as an internal 24 kΩ pull up resistor.

FIGURE 2. Terminal connections - continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
21	CLK	Differential clock input or single ended CMOS input. This pin serves as a differential clock input or as a single ended CMOS input, depending on the logic state of the IN_SEL pin.
22	$\overline{\text{CLK}}$	Complementary differential clock input.
23	IN_SEL	Input select (CMOS input). A logic high on this pin configures the CLK and $\overline{\text{CLK}}$ inputs for a differential input signal. A logic low configures the CLK input for single ended CMOS; as couple the unused $\overline{\text{CLK}}$ pin to ground with a 0.1 μF capacitor.
24	SDIO/SDA/S1	SPI serial data input and output (SDIO)/I^2C serial data (SDA)/pin programming (S1). This multipurpose pin is contolled by the PROG_SEL pin. In SPI mode, SDIO is the serial input/output pin. In 4 wire SPI mode, data writes occur on this pin, in 3 wire SPI mode, both data reads and writes occur on this pin. This pin has no internal pull up/pull down resistor. In I^2C mode, SDA is the serial data pin. In pin programming mode, S1 is hardwired with a resistor to either V_{DD} or ground. The resistor value and resistor biasing determine the channel divider values for the outputs on pin 7 and pin 8.
	EP	Exposed pad. The exposed die pad must be connected to ground (V_{SS}).

FIGURE 2. Terminal connections - continued.

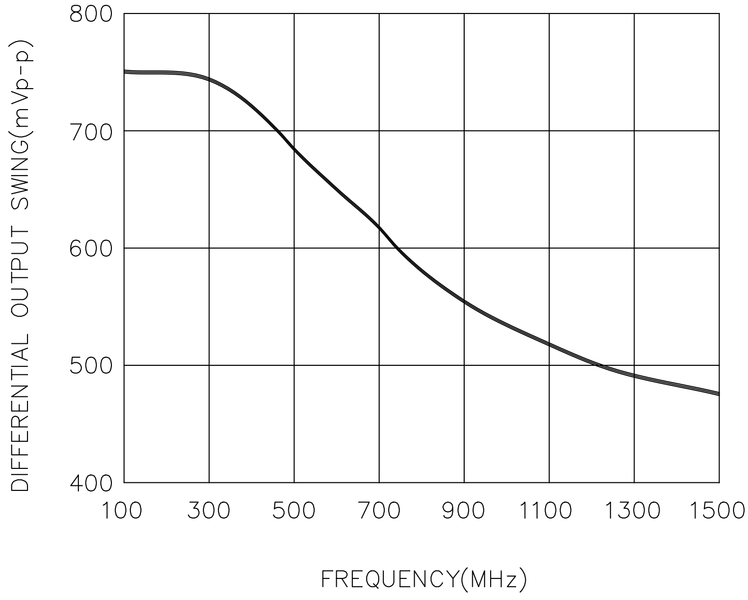

FIGURE 3. LVDS differential output swing versus frequency.

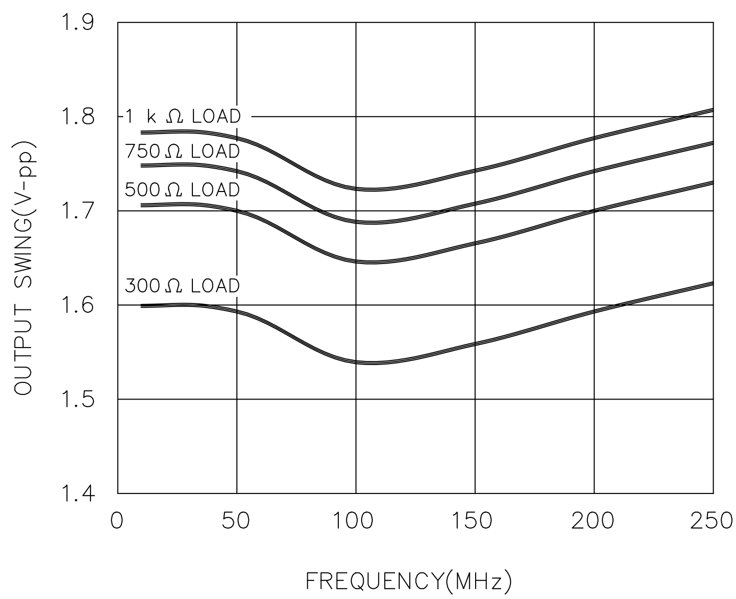

FIGURE 4. CMOS output swing versus frequency and resistive load.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Transportation mode and order quantity	Vendor part number
V62/13626-01XE	24355	Tray, 490	AD9508SCPZ-EP
	24355	7 inch reel, 1500	AD9508SCPZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland