

Reference Design for the AD9552 Oscillator Frequency Upconverter

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INTRODUCTION

The AD9552 is a low cost, programmable device that accepts a low frequency input signal (between approximately 10 MHz and 70 MHz) and upconverts it to a high frequency output signal (up to 900 MHz). This application note provides a reference design for the AD9552 and includes the performance measurements of the output signal. It demonstrates that the AD9552 (and all necessary supporting components) fits within a 9 mm × 14 mm footprint—the same size as some currently available oscillator packages. Refer to AN-0988 for additional information on the features and function of the AD9552.

PRINTED CIRCUIT BOARD

A photograph of the 1" × 1.25" reference design circuit board appears in Figure 1. Note the silkscreened 9 mm × 14 mm rectangle, which contains the following:

- the AD9552
- a crystal resonator
- power supply bypass capacitors
- PLL loop filter components

These constitute all the necessary components to create an oscillator frequency upconverter. The other components on the

PCB are strictly auxiliary. For instance, P1 in the upper left corner serves only to bring power (3.3 V) to the board. Likewise, components J1, T1, C4, C5, R11, and R12 in the lower right corner serve only as a convenient means of measuring the AD9552 output signal. The switch (SST) to the right of P1 is an auxiliary method for resetting the AD9552 (in lieu of cycling the power). The bottom side of the PCB contains no components other than pads for several grounding jumpers (0 Ω resistors) to facilitate pin programming of the AD9552. The reference design includes jumpers only to allow for different crystal types or output frequencies. An end user application typically consists of one crystal type and a fixed output frequency. Thus, jumpers are not required on an end user circuit board. Instead, one would route copper traces directly from the appropriate programming pins to ground to select the desired crystal frequency and output frequency for the specific application.

This particular reference design uses a 19.44 MHz crystal resonator with the AD9552 pin programmed for 625 MHz at OUT1. Note that this demonstrates the ability of the AD9552 to perform noninteger frequency translation (19.44 MHz in, 625 MHz out). Furthermore, the design makes use of the AD9552's default output driver operating mode (LVPECL).

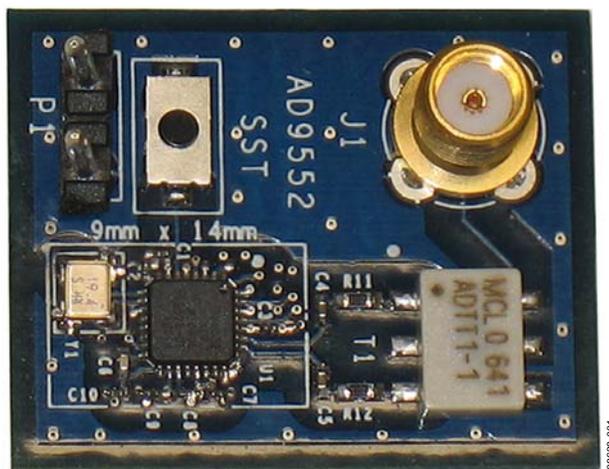


Figure 1. AD9552 Reference Design PCB

The PCB is a 4-layer board using standard FR4 material. The top and bottom layers are for signal routing, whereas the two inner layers are dedicated copper planes for power (VDD) and ground (GND).

To ensure the best possible performance, it is important to place bypass capacitors as close as possible to the AD9552. In addition, it is best to use two vias (through holes), instead of only one, from the grounded pad of each bypass capacitor to the ground plane. This reduces the series inductance from the bypass capacitor to the ground plane, thereby improving high frequency coupling to the ground layer (see Figure 2).

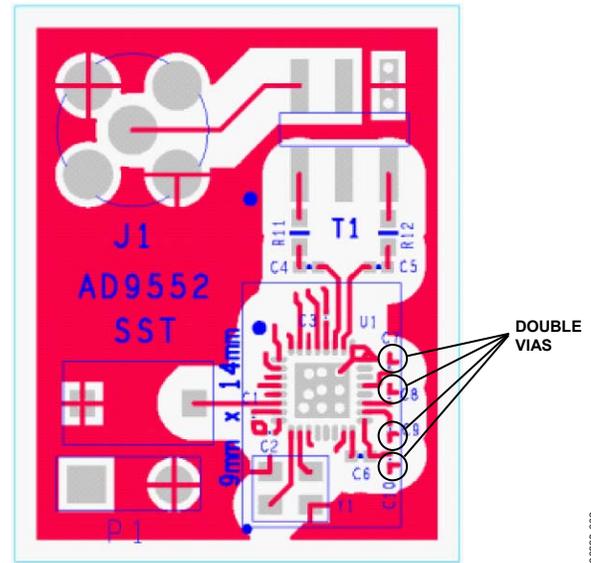


Figure 2. PCB Top Layer Showing Double Vias

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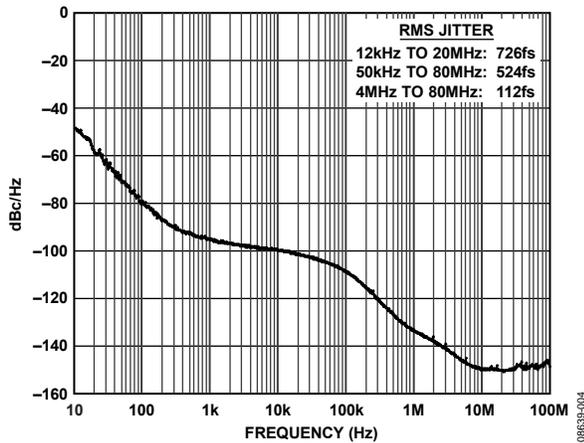


Figure 4. Phase Noise at 625 MHz (Spurious = Off)

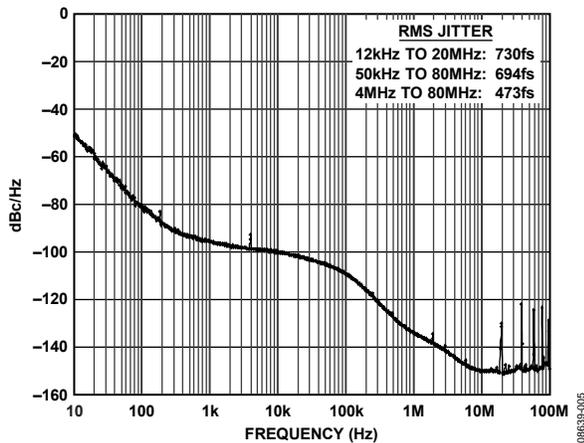


Figure 5. Phase Noise at 625 MHz (Spurious = On)

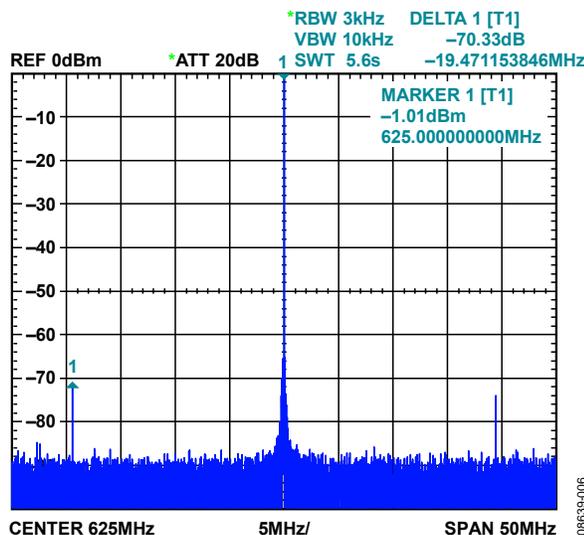


Figure 6. Output Signal Spectrum

ANALYSIS OF THE RESULTS

The phase-noise plot in Figure 5 (spurious = on) indicates spurious artifacts at offset frequencies that are multiples of 19.44 MHz (a consequence of the 19.44 MHz crystal resonator). However, the rms jitter values suggest that the spurious artifacts are sufficiently low in magnitude and, thus, of no concern for applications using the 12 kHz to 20 MHz integration band. This is because Figure 4 and Figure 5 differ by only 4 fs in this band.

The 50 kHz to 80 MHz integration band, however, indicates a degradation of 170 fs in jitter performance for spurious = on, while the 4 MHz to 80 MHz integration band indicates a degradation of 361 fs. The latter shows such a large degradation (an increase in jitter of 322%) because most of the phase-noise energy in the 4 MHz to 80 MHz integration band is spurious rather than random.

The spectral plot (Figure 6) shows the output signal centered at 625 MHz with a measurement span of 50 MHz. Note the relatively low noise floor (near -90 dBm with a resolution bandwidth of 3 kHz) and the two spurs with a magnitude of approximately -70 dBc positioned 19.44 MHz to either side of the 625 MHz carrier.

These are reference spurs due to the 19.44 MHz input frequency of the crystal resonator. These spurs are a normal consequence of the PLL function. The magnitude of the reference spurs directly relates to the bandwidth of the PLL loop filter relative to the reference frequency. The nominal bandwidth of the AD9552 loop filter is 100 kHz, which results in reducing the reference spurs to the -70 dBc range.

Although the reference spurs and their associated harmonics degrade wideband jitter performance, applications requiring low wideband jitter have two options for mitigating this effect. The first option is to provide band-pass filtering of the output signal. In this particular case, a 20 MHz band-pass filter centered at 625 MHz can significantly reduce the wideband spurious content, thus improving wideband jitter performance. The second option is to pass the output signal through a second PLL that has a 1:1 frequency translation ratio and a loop bandwidth that is well below 20 MHz (several hundred kilohertz, for example). The second PLL effectively acts as a jitter cleanup PLL by rejecting the wideband spurious signals (reference spurs in this case) that are outside of its loop bandwidth.