

Designing an Inverting Power Supply Using the ADP2384/ADP2386 Synchronous Step-Down DC-to-DC Regulators

by Ricky Yang

INTRODUCTION

Applications such as bipolar amplifier, optical module, CCD bias, and OLED displays usually require a negative output voltage from a positive input voltage. Designers of power management systems need versatile switching controllers and regulators that allow them to solve these power management challenges. The [ADP2384](#) and [ADP2386](#) switching regulators from Analog Devices, Inc., provide synchronous buck functionality. This ranges from 20 V input voltage down to 0.6 V output voltage at up to 4 A for the [ADP2384](#) and up to 6 A for the [ADP2386](#) of output current at the switching frequency range of from 200 kHz to 1.4 MHz.

Although targeted for synchronous step-down applications, the versatility of the [ADP2384](#) and [ADP2386](#) allows these parts to realize an inverting buck-boost topology, which can generate a negative output voltage from a positive input voltage, without additional cost, component count, or solution size.

In addition, the synchronous topology has certain advantages over the asynchronous topology, such as higher efficiency at low output voltages and lower noise at light load operation. The synchronous topology remains in continuous conduction mode (CCM) in both light load and heavy load operation while the asynchronous topology encounters discontinuous conduction mode (DCM) and pulse skip mode (PSM) with the decrease of the output load current, which can be noisier than CCM.

This application notes describes how to implement the [ADP2384/ADP2386](#) in a synchronous inverting buck-boost topology to generate negative output voltages from positive input power supplies. In addition, some concerns and possible solutions are discussed.

BUCK-BOOST TOPOLOGY BASICS

The simplified buck-boost topology is shown in Figure 1. The topology consists of an inductor, two power switches operating out of phase from one another, and input/output capacitors.

Figure 2 and Figure 3 show the current flow path during the on time and off time, respectively. During the on time, the switch S1 is on, S2 is off, and the current is flowing from the input capacitor, charging the inductor while the output capacitor provides energy to the load. During off time, the switch S1 is off, S2 is on, and the

current is flowing from the inductor to the load and meanwhile charging the output capacitor.

Note that the current is flowing from ground to VOUT, which results in negative output voltage.

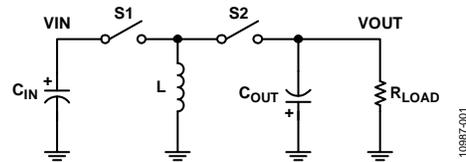


Figure 1. Buck-Boost Topology

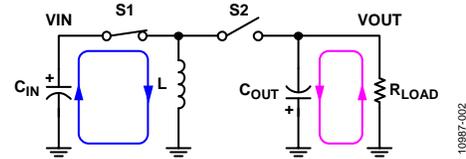


Figure 2. Current Flow Path During On Time

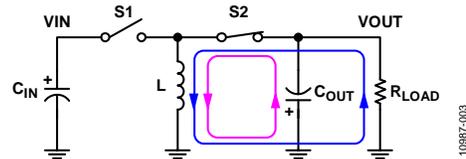


Figure 3. Current Flow Path During Off Time

The steady state conversion ratio can be written as Equation 1 by applying the principles of inductor voltage-second balance and capacitor charge balance on the topology. The dc inductor current value I_L in CCM is specified in Equation 2, and the inductor ripple current ΔI_L is shown in Equation 3.

$$\frac{V_{OUT}}{V_{IN}} = \frac{-D}{1-D} \quad (1)$$

$$I_L = \frac{I_{OUT}}{1-D} \quad (2)$$

$$\Delta I_L = \frac{-V_{OUT} \times (1-D)}{L \times f_{sw}} \quad (3)$$

TABLE OF CONTENTS

Introduction	1	Input Capacitor Selection.....	4
Buck-Boost Topology Basics.....	1	Compensation Selection.....	4
Revision History	2	Enable Signal Level Shifting.....	5
Implementation with the ADP2384/ADP2386	3	Reduce V_{OUT} Ramp Up Before Start Up.....	5
Output Voltage Setting.....	3	Conclusion.....	6
Inductor Selection	3	Related Links.....	6
Output Capacitor Selection.....	4		

REVISION HISTORY

11/12—Revision 0: Initial Version

IMPLEMENTATION WITH THE ADP2384/ADP2386

To implement the buck-boost topology inverting power supply application by using the ADP2384/ADP2386 synchronous buck regulator, some design restrictions must be taken into consideration as listed in Table 1.

Table 1. Design Restrictions

Voltage and Current	Device Parameters	ADP2384/ADP2386
V_{IN_MIN}	V_{UVLO}	4.5 V/4.5 V
$V_{IN_MAX} + V_{OUT} $	V_{MAX}	20 V/20 V
I_{L_PEAK}	I_{OCP}	6.1 A/ 9.6 A

The minimum input voltage of the buck-boost circuit must be higher than the UVLO voltage of the ADP2384/ADP2386, which has the typical value of 4.5 V to get the regulator to work. The sum of the maximum input voltage and the absolute value of the output voltage must be lower than the maximum operation input voltage of the regulators, V_{MAX} which has the typical value of 20 V. In addition, make sure the inductor peak current is smaller than the OCP trigger point of the regulator to get the circuit work normally.

To convert the synchronous buck regulator into the buck-boost topology, the inductor and output capacitor are connected just like in the buck topology. Note that the ground and the output voltage points are reversed as shown in Figure 4.

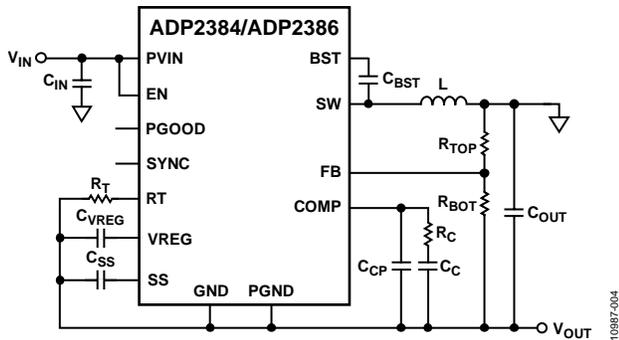


Figure 4. Inverting Buck-Boost Topology Implemented with the ADP2384/ADP2386

OUTPUT VOLTAGE SETTING

The output voltage is set by an external resistive divider. The resistor values are calculated using

$$R_{TOP} = R_{BOT} \times \frac{|V_{OUT}| - 0.6}{0.6}$$

To limit output voltage accuracy degradation due to FB bias current (0.1 μ A maximum) to less than 0.5% (maximum), ensure that $R_{BOT} < 30$ k Ω .

Table 2 lists the recommended resistor divider for various output voltages.

Table 2. Resistor Divider for Difference Output Voltage

V_{OUT} (V)	$R_{TOP} \pm 1\%$ (k Ω)	$R_{BOT} \pm 1\%$ (k Ω)
-1.2	10	10
-1.8	20	10
-2.5	47.5	15
-3.3	10	2.21
-5	22	3
-12	28	1.47
-15	35.7	1.5

INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage and inductor ripple current. Using a small inductor leads to a faster transient response, but degrades efficiency, due to a larger inductor ripple current. Using a large inductor value leads to smaller ripple current and better efficiency, but results in a slower transient response.

As a guideline, the inductor ripple current, ΔI_L , is typically set to 30% of the maximum inductor average current I_{AVG} . The inductor value is calculated using the following equation:

$$L = \frac{V_{IN} \times D}{K_{RP} \times I_{AVG} \times f_{SW}}$$

where:

V_{IN} is the input voltage.

D is the duty cycle:

$$D = \frac{|V_{OUT}|}{|V_{OUT}| + V_{IN}}$$

K_{RP} is the coefficient with a typical value of 30%.

I_{AVG} is the average inductor current.

$$I_{AVG} = \frac{I_{OUT}}{1 - D}$$

f_{SW} is the switching frequency.

The peak inductor current is calculated by adding the dc component and half of the peak-to-peak inductor ripple current.

$$I_{PEAK} = I_{AVG} + \frac{I_{AVG} \times K_{RP}}{2}$$

The peak inductor current is also the peak current in the internal power switch, which is the sense element used to determine whether to induce current limit. To avoid premature current limit, the peak inductor current should not exceed the OCP threshold current, I_{OCP} of the devices.

Taking into account this maximum peak inductor current, the application space of the ADP2384/ADP2386 in the inverting buck-boost topology for common input voltages at 600 kHz switching frequency is shown in Figure 5 with the assumption that the peak-to-peak inductor ripple current is 40% of the inductor average current.

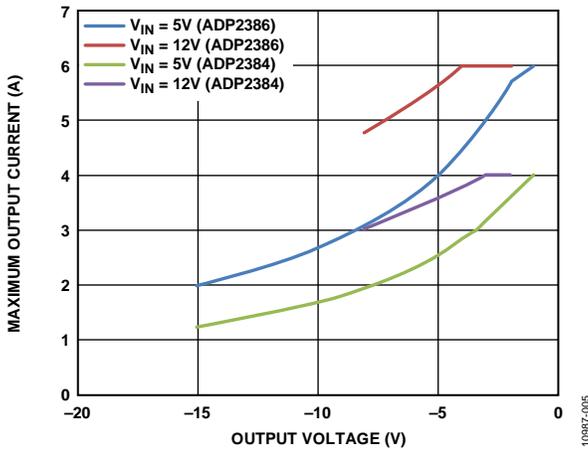


Figure 5. Application Space for Common Input Voltage at $f_{sw} = 600$ kHz

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a quick saturation characteristic, the saturation current rating of the inductor should be higher than the current limit threshold of the switch. This prevents the inductor from saturation through normal operation.

OUTPUT CAPACITOR SELECTION

Note that the output current is discontinuous in the inverting buck-boost topology. The output capacitors supply energy to the load during the on time when energy stored in the inductor is increasing. During the off time, the inductor is delivering energy to both the load and the output capacitors.

One of the major concerns with the capacitance of the output capacitors is the allowable output voltage ripple that is determined by two parameters of the output capacitors. One is the capacitance and the other is the equivalent series resistance (ESR) of the output capacitors. The equation below gives an estimated value of the minimum capacitance required to keep the output voltage ripple within the allowable range.

$$C_{OUT} \approx \frac{I_{OUT} \times D}{f_{SW} \times (\Delta V_{ripple} - I_{PEAK} \times ESR)}$$

where:

ΔV_{ripple} is the allowable output ripple voltage.

ESR is the total equivalent series resistance of the output capacitors.

I_{PEAK} is the inductor peak current.

In order to achieve as low output ripple voltage as possible, the MLCC capacitors that have very low ESR values are recommended. The rms current rating of the selected output

capacitors should be larger than the values calculated using the following equation:

$$I_{RMS_C_{OUT}} = \sqrt{\left(\frac{I_{OUT} \times D}{1-D}\right)^2 \times (1-D) + \frac{\Delta I_L^2}{12} \times (1-D) + I_{OUT}^2 \times D}$$

INPUT CAPACITOR SELECTION

The input current is also discontinuous in the inverting buck-boost topology. Assuming that the input voltage deviation due to the energy depletion of the input capacitor during the on time is lower than 5% of the input voltage, the equation that follows calculates the minimum input capacitance to meet this requirement.

$$C_{IN} = \frac{I_{AVG} \times D}{f_{SW} \times (0.05 \times V_{IN} - I_{PEAK} \times ESR_{C_{IN}})}$$

where:

I_{AVG} is the average inductor current.

$ESR_{C_{IN}}$ is the equivalent series resistance of the input capacitors.

At least one piece of 10 μ F ceramic capacitor is recommended and it should be placed as close to PVIN pin as possible. The rms current of the selected input capacitor should be greater than the value calculated in this equation.

$$I_{RMS_C_{IN}} = \sqrt{\left(I_{OUT}^2 + \frac{\Delta I_L^2}{12}\right) \times D + \frac{D^2 \times I_{OUT}^2}{1-D}}$$

Although the majority of the capacitance on the input voltage rail is referenced to system ground, an additional input decoupling capacitor placed from the input voltage to the GND pin of ADP2384/ADP2386 can reduce the output voltage ripple and improve the transient response as shown in Figure 6.

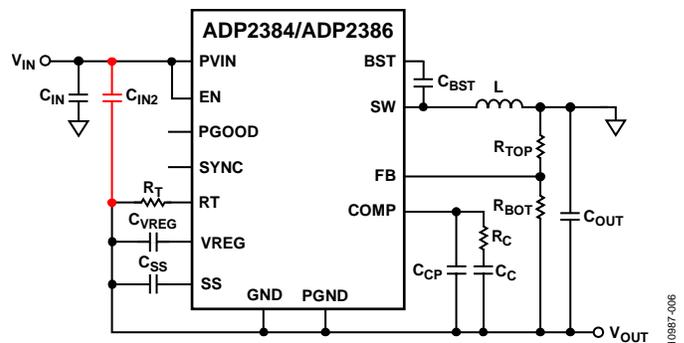


Figure 6. Inverting Buck-Boost Topology with Input Decoupling Capacitor from V_{IN} to GND pin

COMPENSATION SELECTION

When applying the synchronous buck regulator into the inverting buck-boost topology to create a negative output voltage, the power stage transfer function changes because of the difference power circuit topology. In order to get a stable close loop of the system, the values of the compensation network should be redesigned.

The control-to-output transfer function of the power stage in buck-boost topology can be written in the form:

$$G_{VD}(s) = K \times \frac{\left(1 - \frac{s}{2 \times \pi \times f_{Z1}}\right) \times \left(1 + \frac{s}{2 \times \pi \times f_{Z2}}\right)}{\left(1 + \frac{s}{2 \times \pi \times f_p}\right)}$$

where:

$$K = \frac{R \times (1 - D)}{R_i \times (1 + D)}$$

R is the load resistor.

R_i is the current sense gain with a typical value of 0.115 V/A.

The transfer function G_{VD}(s) has one right-half-plane-zero (RHPZ) f_{Z1}, one zero f_{Z2}, and one pole f_p. The values of the zero and pole are:

$$f_{Z1} = \frac{(1 - D)^2 \times R}{2 \times \pi \times L \times D}$$

$$f_{Z2} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

$$f_p = \frac{1 + D}{2 \times \pi \times R \times C_{OUT}}$$

where:

R_{ESR} is the equivalent series resistance of the output capacitor.

Follow the design guideline listed here to calculate the values of the compensation network components.

- Set the cross frequency f_c between f_p and 1/3 of f_{Z1}

$$f_c = \sqrt{f_p \times f_{Z1}}$$

- Calculate the R_c value using the equation:

$$R_c = \frac{f_c \times |V_{OUT}|}{K \times f_p \times g_m \times 0.6}$$

where:

g_m is the transconductance of the internal error amplifier with a typical value of 480 μS.

- Place the compensation zero at 1/2 of the power stage pole f_p

$$C_c = \frac{2 \times R \times C_{OUT}}{(1 + D) \times R_c}$$

- Place the compensation pole at the RHPZ f_{Z1}

$$C_{CP} = \frac{D \times L}{(1 - D)^2 \times R \times R_c}$$

ENABLE SIGNAL LEVEL SHIFTING

The ADP2384/ADP2386 has an EN pin to enable and disable the regulator. However, in the inverting buck-boost application, the IC is referenced to the negative output voltage instead of the system ground. It is entirely possible that if the EN pin is connected to system ground with the intention to disable the regulator, the ADP2384/ADP2386 will still be switching.

One of the possible solutions for this is using NPN and PNP transistors plus several resistors with the proper connection to form an EN level shifting circuit as shown in Figure 7.

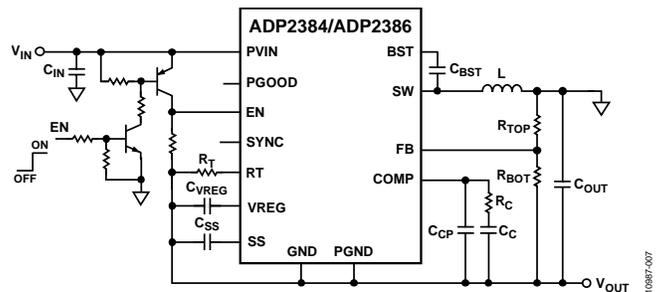


Figure 7. EN Level Shifting Circuit for Inverting Buck-Boost Topology

Note that the precision enable feature of the ADP2384/ADP2386 is lost when the level shifting circuit is used. If the enable function is not needed, simply connect the EN pin to the input voltage as shown in Figure 4.

REDUCE V_{OUT} RAMP UP BEFORE START UP

When using the synchronous buck regulator to achieve the inverting buck-boost topology, one common issue that may be observed is that the output voltage ramps up and becomes positive voltage before the regulator starts to work as shown in Figure 8.

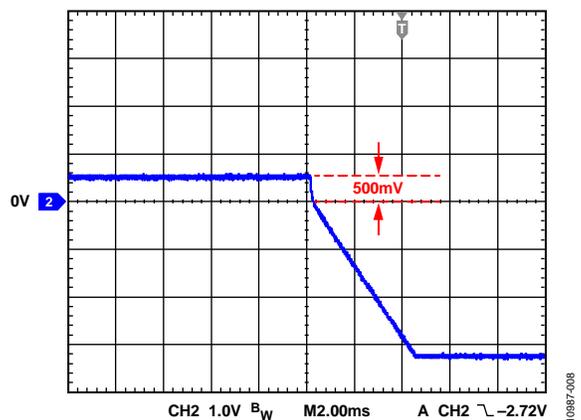


Figure 8. V_{OUT} Ramps Up Before Start Up

This positive output voltage ramping up is caused by the shutdown current of the regulator flowing from PGND pin of the IC through the body diode of the low-side MOSFET and back to the system ground as shown in Figure 9. The body diode of the low-side MOSFET is that which clamps the V_{OUT} at the forward voltage of the body diode with a typical value around 500 mV.

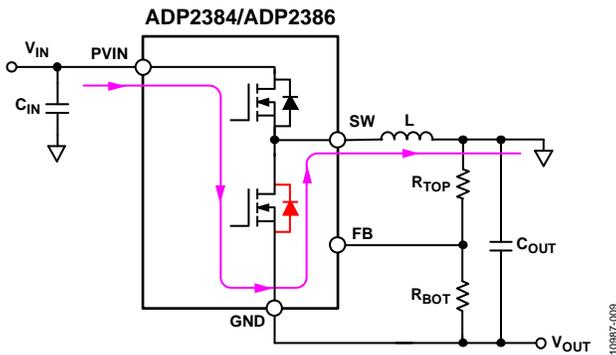


Figure 9. Current Flows Through Body Diode of Low Side MOSFET

As V_{OUT} is connected to the GND pin of the regulator which is actually the reference point for the internal circuits like UVLO, the positive voltage shown in the GND pin decreases the UVLO threshold voltage. The regulator may fail to start up when the input voltage is very close to the UVLO threshold voltage of the regulator, which has a typical value of 4.3 V.

This issue can be seen in almost all the synchronous buck regulators when they are used to perform the inverting buck-boost topology described herein and it is very hard to eliminate the issue thoroughly. One alternative solution is to reduce the resistance of the feedback resistor divider until the voltage drop across the resistor divider is lower than the forward voltage of the body diode of the low-side MOSFET. Then, the shutdown current flows through the resistor divider instead of the body diode as shown in Figure 10 and the positive voltage on the GND pin can be reduced to an acceptable value.

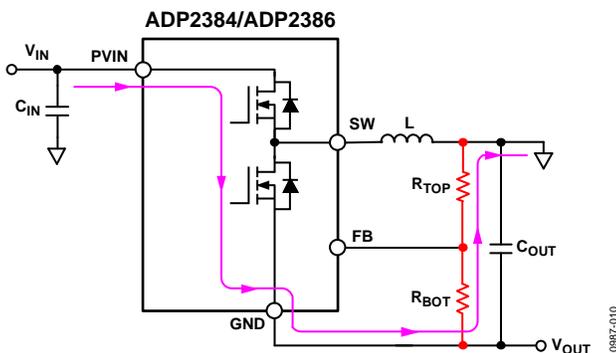


Figure 10. Current Flows Through the Feedback Resistor Divider

Figure 11 shows the result of reducing the resistance of the resistor divider. The positive V_{OUT} voltage decreases from 500 mV to 180 mV.

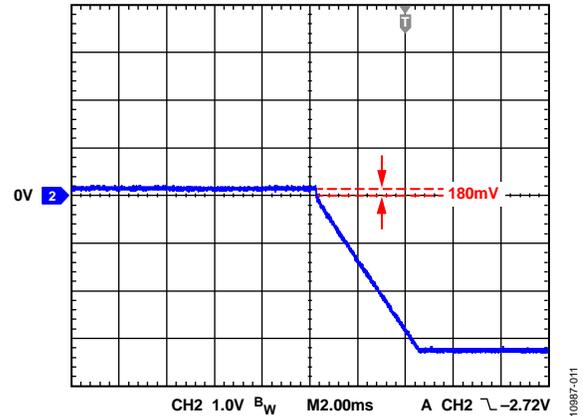


Figure 11. Reduce V_{OUT} Ramp Up by Decreasing the Resistance of the Feedback Resistor Divider

The drawback of this solution is that the quiescent current of the system increases since the current flowing through the feedback resistor divider increases as a result of reducing the resistance of the divider. The efficiency at light load also suffers.

CONCLUSION

Implementation of the ADP2384/ADP2386 in the inverting buck-boost topology can be simple, inexpensive, and small in solution size as the buck implementation. This application note provides a simple EN level shifting circuit when the enable/disable functionality is needed. The V_{OUT} ramping up to positive voltage issue when applying the synchronous buck regulator into the inverting buck-boost topology is discussed in this application note. A possible solutions for this issue is provided.

By following the design equations and suggestions in this application note, the system designer can ensure a robust design that satisfies all the requirements.

RELATED LINKS

Table 3.

Resources	Description
ADP2384	Data sheet, 20 V, 4 A, Synchronous Step-Down DC-to-DC Regulator
ADP2386	Data sheet, 20 V, 6 A, Synchronous Step-Down DC-to-DC Regulator
AN-1083	Application Note, Designing an Inverting Buck-Boost Using the ADP2300 and ADP2301 Switching Regulators
ADP238x Inverting Buck-Boost Regulator Design Tool	ADIsimPower, Excel®-based inverting buck-boost design tool for the ADP238x family.

NOTES

NOTES