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Operating the Mixed Signal Digital Predistortion (MSDPD) Evaluation Platform

FEATURES

High performance RF transmit and observation receive signal chains seamlessly integrated onto one board
RF transmitter design
- **Supports both zero-IF and complex-IF architectures**
- **300 MHz of complex bandwidth**
- **1.2 GSPS, 16-bit quadrature digital-to-analog converter (DAC)**
- **12 dB of fine analog gain control**
- **Up to 17 dBm typical output power**

Observation receiver design
- **IF sampling architecture**
- **500 MSPS, 12-bit analog-to-digital converter (ADC)**
- **24 dB of gain control in 1 dB steps**

Clock cleanup and distribution network
- **SERDES clock cleanup up to 307.2 MHz**
- **Full synthesis for shared or separate Tx/Rx local oscillator (LO)**
- **Optional on-board crystal reference**

Available with either HSMC or FMC connectors to mate to FPGA platforms
USB interface with intuitive user software
Includes RF shielding covers and hardware
On-board power supply regulation

EQUIPMENT SUPPLIED

AD-MSDPD-9434/AD-MSDPD-6641 demonstration board
USB to mini-USB cable
PSU adapter board
Switching power supply (international multiplug)
Custom shielding and associated hardware
Software installation CD

EQUIPMENT NEEDED

USB 2.0 port (USB 1.1 compatible)
FPGA development kit
- **Xilinx ML605 (FMC connector)**
- **Altera Stratix IV GX or Arria II GX (HSMC connector)**

AD-MSDPD-9434/AD-MSDPD-6641 demonstration board
Spectrum analyzer (optional)
PC running Windows® XP (32-bit only) or Windows Vista/Windows 7 (32-bit or 64-bit)

SOFTWARE NEEDED

Analog Devices, Inc., MSDPD Dashboard 1.6
Analog Devices SPIController

EVALUATION BOARD DIGITAL PHOTOGRAPH

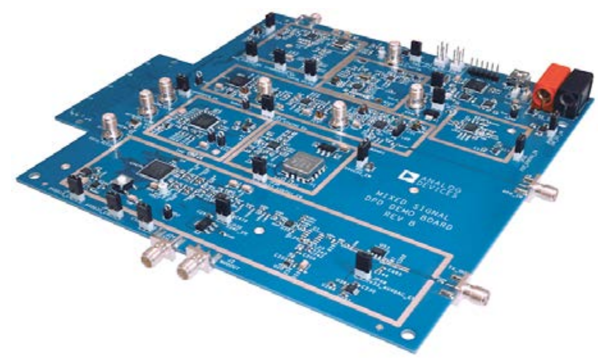

Figure 1.

Table 1. Related Documents

Document	Subject
AD9122, ADL5375, ADL5541, ADL5320, AD9434, AD6641, AD8375, AD5611, ADL5365/ADL5367, AD9516-0, ADF4002, ADF4350, ADF4351, ADCLK905, ADCLK925	Applicable Analog Devices mixed-signal, RF, and analog product data sheets

GENERAL DESCRIPTION

This document describes the operation of Analog Devices mixed-signal digital predistortion (MSDPD) evaluation platform that can be used to develop and to prototype digital predistortion algorithms as well as to demonstrate core Analog Devices technology. The board is designed to provide best-in-class performance for both the RF transmit and observation receive signal paths. The board outputs a power signal at the desired RF carrier frequency that can be used to drive an external power amplifier (PA) directly. Inputs to the board include baseband digital data from the digital processor, optional reference clocks, and the observed RF output from an external RF coupling network.

The end goal of the MSDPD evaluation platform is to enable customers to develop their digital predistortion strategy by using state-of-the-art Tx/Rx signal chains, including a 1.2 GSPS dual DAC and a 500 MHz 12-bit ADC. Depending on the methods employed, this could allow for a corrected Tx bandwidth of greater than 40 MHz.

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REVISION HISTORY

8/12—Revision 0: Initial Version

SYSTEM OVERVIEW

The diagram in Figure 2 shows the overall topology of the MSDPD board.

The board accepts baseband I data and Q data from the FPGA into the AD9122, a 16-bit, 1.2 GSPS dual DAC. The analog output is then modulated up to the desired RF output frequency and amplified to generate a maximum of between 16 dBm and 24 dBm full-scale depending on frequency. This signal can then be passed directly to an external PA for transmit.

The transmit path can be configured for zero IF or complex IF. Complex IF is preferred because the local oscillator (LO) feedthrough and RF image fall out-of-band and can be attenuated with the gain, phase, and offset compensation features of the AD9122 DAC.

A full observation path is included to accept the coupled and attenuated RF output. This input is mixed down to a suitable IF frequency and digitized with a 12-bit, 500 MSPS ADC, either the AD9434 or the AD6641.

The board can accept a recovered SERDES network clock of either N × 30.72 MHz or N × 38.4 MHz up to a maximum of 307.2 MHz. If no external reference is available, an on-board 30.72 MHz crystal reference is available and provides standalone operation. Regardless of the reference used, the MSDPD board provides dual-loop PLL clock clean-up and full synthesis of the ADC, DAC, and network clocks. The board also synthesizes local oscillators for the RF mixers in both the transmit and observation receive paths.

Control of the board is via the USB using an intuitive PC-based user interface or by direct access from the FPGA. Power is 5.3 V at up to 3 A, depending on the exact configuration.

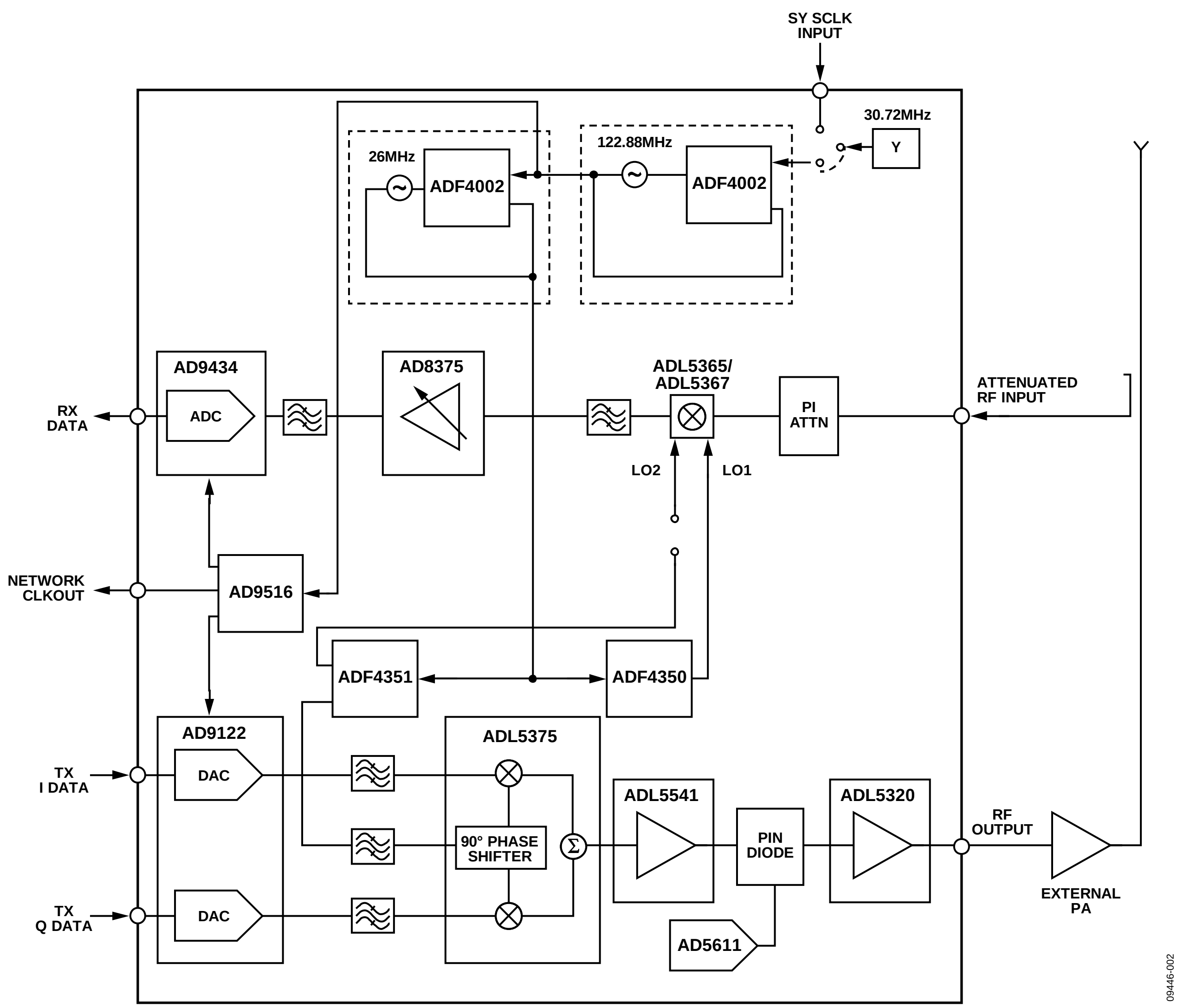

Figure 2. MSDPD Board Block Diagram

A typical closed-loop setup is shown in Figure 3. The MSDPD board connects to a suitable FPGA development board through a connector as shown. The MSDPD board is available with either the Xilinx FMC or the Altera HSMC connectors.

Through the connector, all FPGA resources are appropriately routed to the mixed signal resources. The MSDPD board is configured via the USB using an intuitive PC-based user interface or by direct access from the FPGA interface when needed.

Included with the board is a wall mount switching power supply that converts any input from 100 V ac to 240 V ac to 6 V dc at up to 3 A maximum. This switching power supply is used in conjunction with the PSU adapter board to form a complete power supply solution for the MSDPD board.

The source for the external clock can be either the on-board 30.72 MHz crystal reference or the data clock derived from the CPRI, OBSAI, or other data source.

In development, an external RF power amplifier, directional coupler, and dummy load are needed to complete the RF path, as shown in Figure 3.

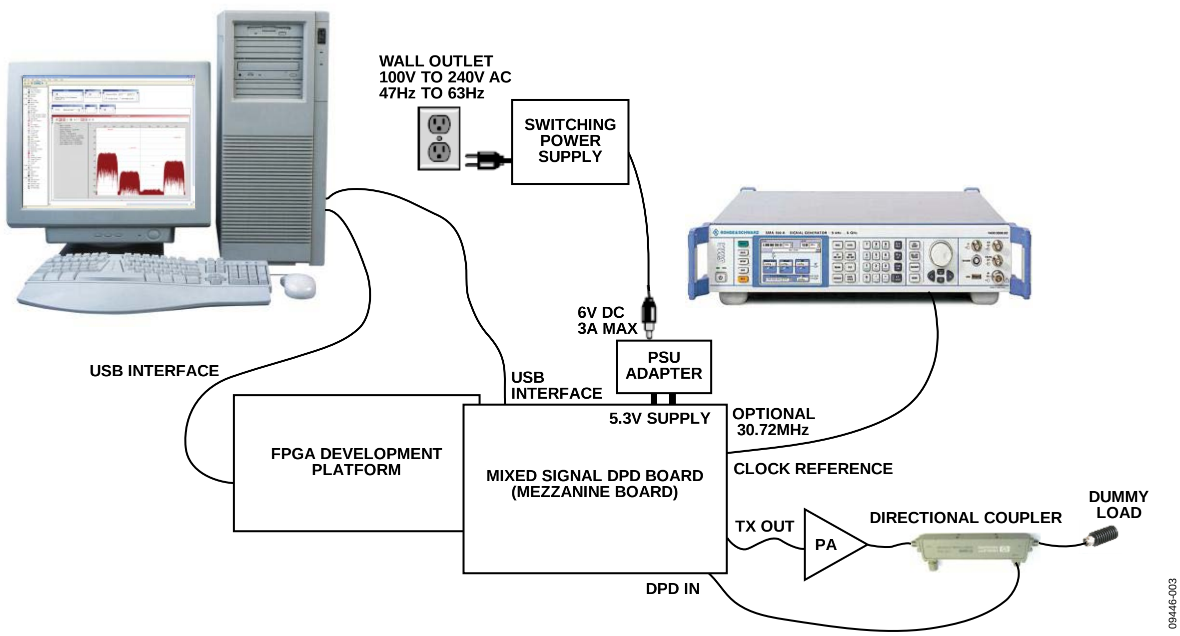

Figure 3. Application of the MSDPD Evaluation Platform

EVALUATION BOARD QUICK START GUIDE

The necessary steps to get the MSDPD board up and running quickly are provided in this section. The quick start guide includes software and hardware installation instructions as well as a simple configuration example. For additional information on the hardware and the software, refer to the Detailed Hardware Description section and Detailed Software Description section.

REQUIREMENTS

The following lists the requirements for the MSDPD board:

- AD-MSDPD-EVB board, 6 V power supply, PSU adapter board, and USB cable
- FPGA development kit, USB cable, and power supply for FPGA board
- PC running Windows XP (32-bit only) or Windows Vista/Windows 7 (32-bit or 64-bit) with all necessary FPGA software installed

SOFTWARE INSTALL

The MSDPD kit includes a CD with all of the necessary software installation files to get the MSDPD board up and running as well as instructions on installing the software. The two software packages included are the SPIController and the MSDPD Dashboard 1.6.

Note that this software is always available from Analog Devices FTP site at: ftp://ftp.analog.com/pub/HSSP_SW/MSDPD.

The software packages must be installed in the order listed. In addition, when a software update of SPIController is performed, reinstall the MSDPD Dashboard. This is because the MSDPD Dashboard overwrites two files that enable a TCP connection between the MSDPD Dashboard and SPIController.

Required prerequisites for these software packages are included in the full install. Prerequisites include National Instrument's VISA program as well as Microsoft's .NET Framework 3.5 with Service Pack (SP) 1. For any subsequent updates to the MSDPD Dashboard software, a lite-install can be completed.

If desired (not necessary), an update to the SPIController software can be completed from the SPIController GUI if an internet connection is available on the target machine. To perform an update, follow these steps:

1. From the **SPIController** window, select **File/Cfg Open** and open any configuration file that does not have the **eng** string, such as **AD6642_11Bit_200MSspiR03.cfg**. Ignore any error or warning messages.
2. Once the new configuration file opens, select **File/Download Files From FTP Site**. Note that the SPIController restarts as part of this process.
3. Once the download is complete and the SPIController relaunches, close both the SPIController and MSDPD Dashboard programs.
4. Reinstall the MSDPD Dashboard.
5. Launch the MSDPD Dashboard program, and the SPIController also opens with the correct configuration file: **ADMSDPDspiengR03.cfg**.

HARDWARE SETUP

For this quick start, on-board 30.72 MHz reference was used. The Tx IF is configured for 184.32 MHz, and the Rx IF is configured for 368.64 MHz. The DAC sample rate is 737.28 MSPS, and the ADC sample rate is 491.52 MSPS. The RF band center frequency is set to an appropriate value within the range of the chosen board model.

Complete the software install steps in the Software Install section before continuing with the following:

1. Connect the MSDPD board to the FPGA development board.
2. Connect the provided USB cable to the MSDPD board and to an available USB port on the computer.
3. Connect the USB cable included with the FPGA development kit to the JTAG port of the FPGA board and to an available USB port on the computer.
4. Connect the power supply included with the FPGA development kit to an ac wall outlet and to the FPGA board. Then, power on the FPGA board.
5. The MSDPD board is supplied with a wall mount switching power supply and a PSU adapter board. Connect the supply end to an ac wall outlet rated for 100 V ac to 240 V ac at 47 Hz to 63 Hz. The other end is a 2.1 mm inner diameter jack that connects to the PSU adapter board. The PSU adapter board then attaches to the MSDPD board through banana jack connectors. Ensure that the 5.3 V terminal on the PSU adapter board mates with the red banana plug terminal on the MSDPD board (see Figure 4).

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Figure 4. PSU Adapter Board

6. Once the USB cable is connected to both the computer and the MSDPD board, and power is applied, the USB driver starts to install. The **Found New Hardware Wizard** opens and prompts users through the automated install process.

7. Connect the MSDPD board to the FPGA host board:
   a. If the Xilinx ML605 development kit is being used, connect two matched length short SMA cables from J7 and J8 on the MSDPD board (NETWORK_CLKP/ NETWORK_CLKN) to J58 and J55 on the ML605 board (USER CLK P/USER CLK N), respectively. Next, connect the Xilinx board to the AD-MSDPDX-9434/ AD-MSDPDX-6641 board via the FMC connectors (see Figure 5).

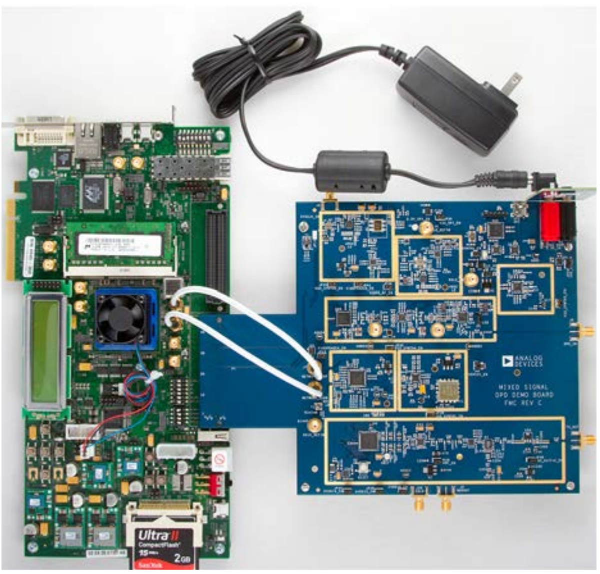

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Figure 5. Xilinx ML605 and AD-MSDPDX-9434/AD-MSDPDX-6641

   b. If the Altera Stratix IV development kit is being used, connect the Altera board to the AD-MSDPDA-9434/ AD-MSDPDA-6641 board via the HSMC connectors (see Figure 6).

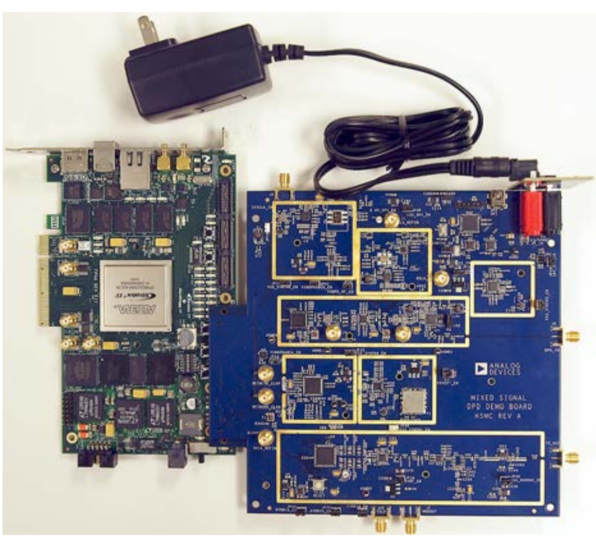

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Figure 6. Altera Stratix IV and AD-MSDPDA-9434/AD-MSDPDA-6641

8. Launch the MSDPD Dashboard program. A **SPIController** window also launches, this can take up to 30 seconds. At startup, an error message may appear. If so, click **OK**. The **SPIController** window must launch before the board can be programmed. Once the **SPIController** window opens, it can be minimized; however, do not exit the **SPIController** window. Ensure that the correct MSDPD Dashboard is installed by checking that the title refers to the **MSDPD Gen1.6 Dashboard**. When the software is ready, there is a green ready signal in the lower left corner of the MSDPD Dashboard program (see Figure 7).

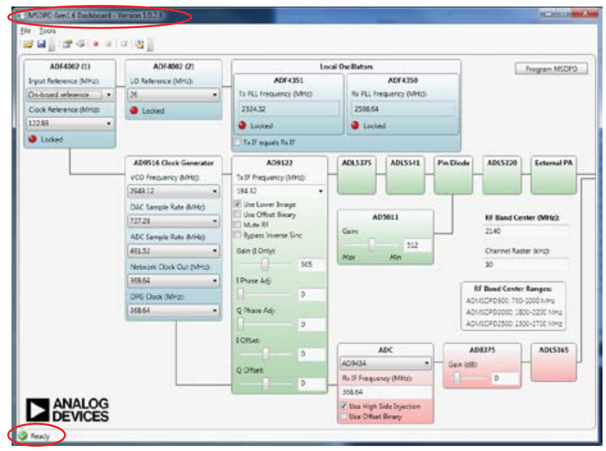

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Figure 7. MSDPD Dashboard Software Ready

USING MACROS

Note that for future reference, the MSDPD Dashboard software has a macro feature that can record any sequence of actions made while using the software. The changes are recorded in the order that they are made so that the MSDPD board can be provided with the same setup every time. The **Record Macro** button is a red circle near the top of the MSDPD Dashboard (see Figure 8).

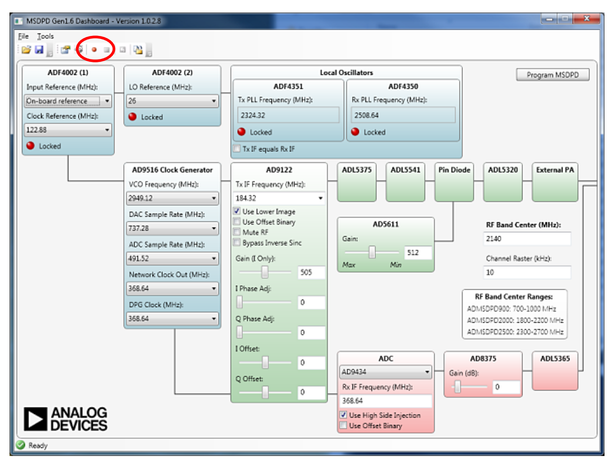

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Figure 8. ***Record Macro***

To record and save a macro, take the following steps:

1. Click the **Record Macro** button prior to making any changes to save these changes. Clicking **Record Macro** grays out the button to indicate that a macro is currently being recorded.
2. Push **Program MSDPD** to have any changes made show up in the macro.
3. Click the **Stop** button to the right of the **Record Macro** button to stop the macro.
4. Once the macro recording has been stopped, click **Save Macro As…**to save the macro (see Figure 9). The macro can then be saved as a .mgp (SPIController Macro Group) file.

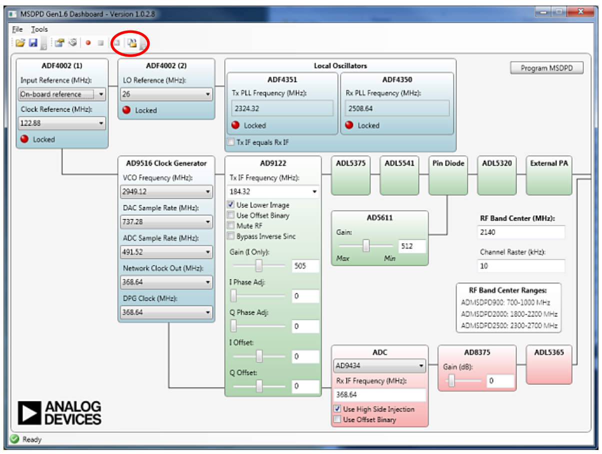

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Figure 9. ***Save Macro As…***

To use the macro once it has been saved, take the following steps:

1. Click **Reset Macro**, which is located to the immediate left of the **Save Macro As…** button, to ensure that the macro recording is reset. This macro file can now be loaded into the SPIController, which reduces setup time.
2. Load the macro file into the SPIController. Go to **File/ MacroGroup Open** and select the saved file.
3. Run the macro. Go to **Config/Launch Macro Editor**. A list of all the registers that were set in the macro is then seen.
4. Click the red lightning bolt button in the pop-up **MacroEditor** to write to these registers.

LOCKING PLLS

Once the MSDPD Dashboard and SPIController programs are open, the first step in running the board is to generate all of the clocks for the devices.

1. Ensure that the RF band center frequency falls within the range of the board model being used (see Figure 10). Note that changes made to the RF band center frequency automatically update the local oscillator frequencies.

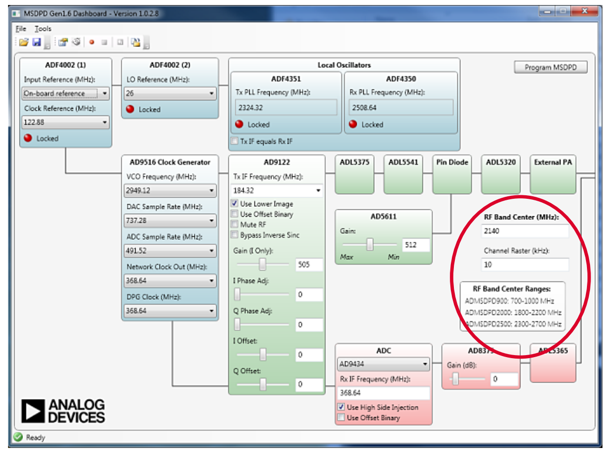

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Figure 10. Select RF Band Center Frequency

2. Ensure that the **Input Reference (MHz)** selection is set to **On-board reference** and that the **Tx IF equals Rx IF** option is not selected. Set the **Network Clock Out (MHz)** parameter in the AD9516 **Clock Generator** block to 368.64 MHz. Note that the **DPG Clock (MHz)** and the **Network Clock Out (MHz)** track.

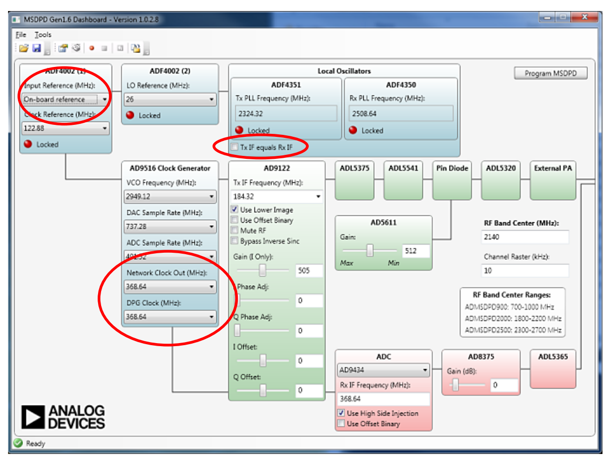

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Figure 11. Clock Control

3. Select **Program MSDPD**.

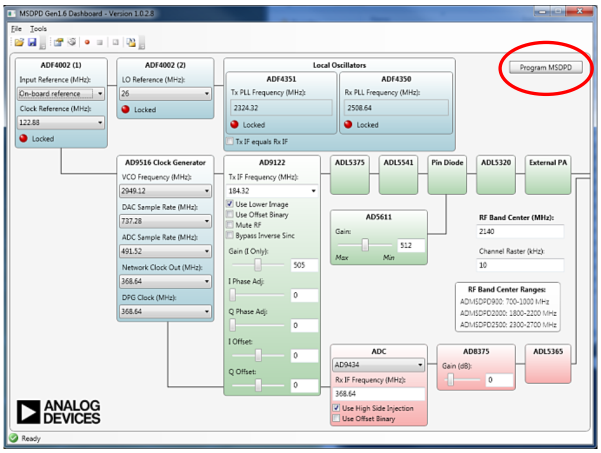

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Figure 12. ***Program MSDPD***

4. At this point, observe the five LEDs (CR1 to CR4 and CR6) near each of the PLL chips lighting up, signifying that all PLLs are locked (see Figure 13).

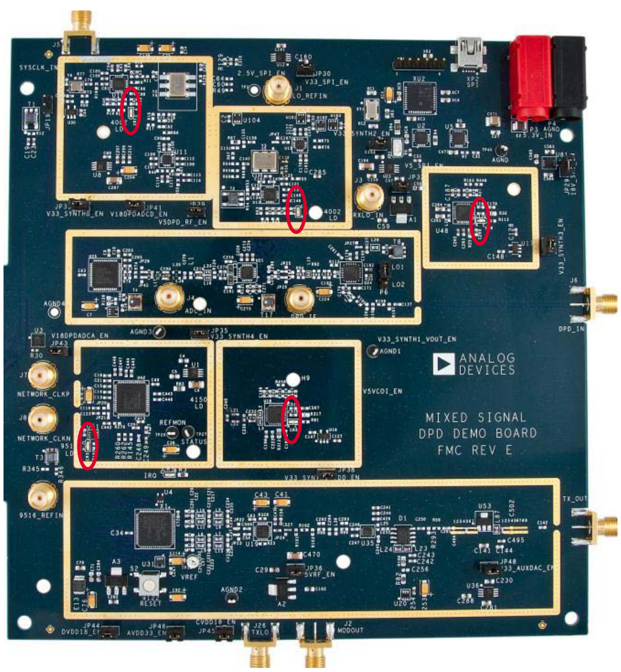

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Figure 13. LEDs on MSDPD Board

TRANSMIT OUTPUT

The next step is to download a digital baseband waveform to the FPGA board and begin sending the digital data to the MSDPD board. A spectrum analyzer can then be used to measure the performance of the transmit output.

1. If the data vector is in offset binary data format, check the **Use Offset Binary** option in the **AD9122** block on the MSDPD Dashboard and select **Program MSDPD**.
2. Connect the TX_OUT SMA to a spectrum analyzer and set the center frequency to be the same as the **RF Band Center (MHz)** listed in the MSDPD Dashboard.
3. Referring to the appropriate FPGA demonstration guide, download a digital baseband waveform to the FPGA and begin playing the waveform.
4. To change the RF output power, adjust the **AD5611 Gain** on the MSDPD Dashboard. This can be done by moving the slider or by entering a value between 0 and 1023 in the text box. Note that the gain value is updated automatically and does not require the selection of **Program MSDPD**. However, if a value is entered in the text box, click on some other text field for the value to be entered.
5. To optimize the image rejection and LO cancellation at the TX output, enter the **Gain (I Only)**, **I Phase Adj:**, **Q Phase Adj:**, **I Offset:**, and **Q Offset:** values included on the board into the appropriate fields in the **AD9122** block on the MSDPD Dashboard front panel (see Figure 14).

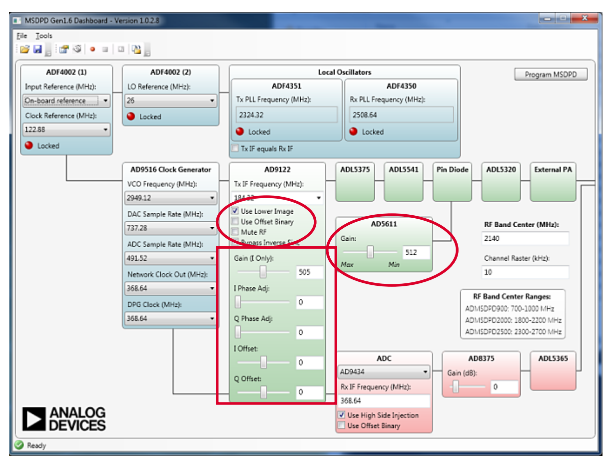

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Figure 14. Tx Control

LOOPBACK TESTING

Once the transmit output is verified, the observation receiver can be tested by looping the Tx output back to the DPD input.

1. Select the appropriate ADC from the drop-down menu. Note that, for China, this is typically the AD6641, whereas for other areas, this is typically the AD9434. Set the appropriate data format (offset binary or twos complement) for the AD9434/ AD6641 digital output. This is specified in the FPGA demonstration guide.
2. Set the gain of the AD8375 amplifier in the Rx path to 0 dB. This can be done by moving the slider or by entering a value of 0 in the text box. Note that the gain value is updated automatically and does not require the selection of **Program MSDPD**. However, if a value is entered in the text box, click on some other text field for the value to be entered.
3. Set the gain of the Tx path by entering a value of 750 in the **AD5611** text box control.
4. Disconnect the Tx output from the spectrum analyzer and connect it to the DPD input (J6).
5. The FFT of the data received from the MSDPD board must match the transmitted waveform. The expected SNR is approximately −60 dBFS.

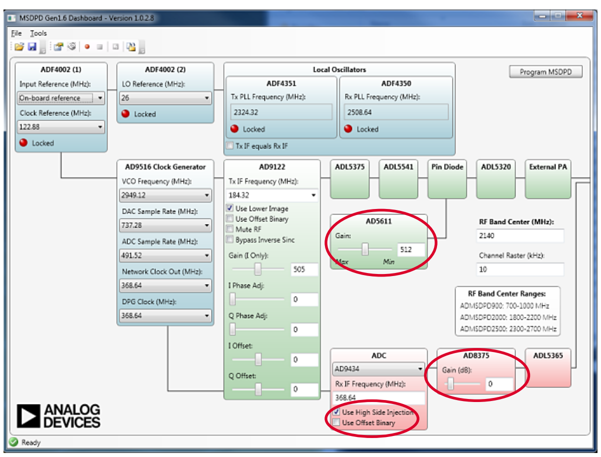

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Figure 15. Rx Control

CONNECTING THE PA

Before connecting the MSDPD board to a PA, install the shields included with the MSDPD kit. The EMI/RFI shielding ensures optimal performance in the presence of the high fields associated with RF power technology. The shielding is brass, and it must be held in place with supplied screws.

The Tx output from the MSDPD board can be directly connected to the PA; however, the Tx output must be muted until the PA is powered up. Select **Mute RF** in the **AD9122** box on the MSDPD Dashboard to mute the Tx output (see Figure 16). This is an asynchronous control; therefore, pressing **Program MSDPD** is not required.

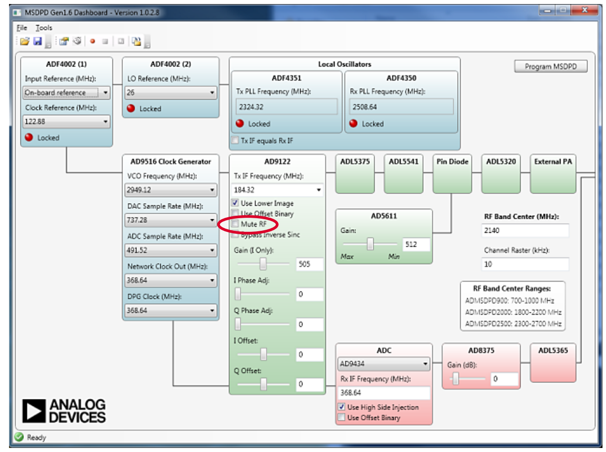

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Figure 16. Mute RF

The PA output can be connected to a directional coupler where the coupled port is connected to the DPD input on the MSDPD Dashboard. Caution: Peak input power to the MSDPD Dashboard is limited to 20 dBm. Signals beyond this level can result in permanent damage.

It is recommended that the coupled RF output be attenuated to provide an input power that preserves ac performance. For optimal IMD performance, DPD input levels less than 0 dBm are recommended. Therefore, the high power output of the directional coupler can be attenuated with a power attenuator. The PA output can also be attenuated and viewed on a spectrum analyzer (see Figure 17) or connected to a high power 50 Ω dummy load (see Figure 3).

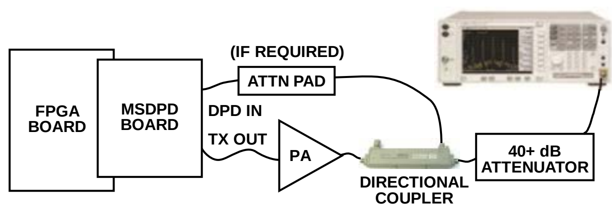

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Figure 17. Typical DPD Test Setup with PA and Spectrum Analyzer

An alternative setup for the PA output can consist of a high power attenuator and a splitter where one output can be further attenuated (if required) and looped back to the DPD input. The other output can be viewed on a spectrum analyzer (see Figure 18).

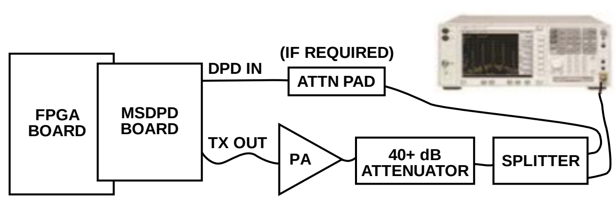

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Figure 18. Alternate DPD Test Setup with PA and Spectrum Analyzer

DETAILED HARDWARE DESCRIPTION

POWER

The MSDPD Dashboard was designed to operate off a 5.3 V dc power source supplied through banana connectors. To form a complete power supply solution for the MSDPD Dashboard, the power supply unit (PSU) adapter board was designed to interface between a 6 V, 3 A wall mount switching power supply and the banana jacks on the MSDPD Dashboard.

There are many active devices included on the MSDPD Dashboard that require various supply voltages. The 5.3 V dc input is distributed across the MSDPD Dashboard and locally regulated with linear regulators (LDOs) to the appropriate devices (see Table 2 for a list of the supply domains). Each supply domain can be disconnected by removing the associated enable jumper.

Table 2. Supply Domains List

Supply Domain	Device(s)	Jumper
CVDD18	AD9122	JP45
DVDD18	AD9122	JP44
AVDD33	AD9122	JP46
V33_SYNTH1	ADF4351	JP38
V33_AUXDAC	AD5611	JP48
V5RF	ADL5375, ADL5541, ADL5320	JP36
V5DPDRF	ADL5365, AD8375	JP39
V33_SYNTH3	ADF4350	JP40
V18DPDADCD	AD9434/AD6641	JP41
V18DPDADCA	AD9434/AD6641	JP43
V33_SYNTH2	ADCLK905	JP34
V33_SYNTH4	AD9516-0, SY89833LMG	JP35
V33_SYNTH0	ADF4002, ADCLK925	JP33
V33_XO	30.72 MHz reference	Not applicable
18V_SPI	Control signal level translation	JP29
V33_SPI	Control signal level translation	JP30
5V_SPI	Control signal level translation	JP32
FPGA_2.5V	Control signal level translation	JP31

The switching power supply includes interchangeable input blades to support international ac wall outlets. The switching power supply can take inputs of 100 V ac to 240 V ac at 47 Hz to 63 Hz and outputs 6 V dc up to 3 A.

The PSU adapter board was designed to mate to the switching power supply plug, step down the dc voltage to 5.3 V, and connect to the banana jack inputs of the MSDPD Dashboard. The PSU adapter board consists of a high current diode, resettable polyfuse, common-mode choke coil, and power supply filtering.

A block diagram of the full clock path is shown in Figure 19. The 122.88 MHz output from the clock clean-up PLL (ADF4002 [1]) is passed to the AD9516-0 for converter and network clock generation. This output is also passed to a second PLL (ADF4002 [2]) used to set up a 26.0 MHz reference for the local oscillators. This permits a channel raster of 10 kHz to be realized.

CLOCK

The MSDPD Dashboard includes full clock synthesis capability and multiloop clock clean up facilities.

An on-board reference of 30.72 MHz is available or an external reference of N × 30.72 MHz or N × 38.4 MHz either can be provided from a signal generator or recovered SERDES data clock based off either CPRI or OBSAI. Many different configurations are possible.

Using a VCXO of 122.88 MHz, Table 3 shows possible input frequency rates and typical divider values for proper operation of the ADF4002 clock clean-up PLL.

Table 3. Usable Reference Input Frequencies

Reference Input (MHz)	VCXO Frequency (MHz)	R divider	N divider
30.72	122.88	1	4
38.4	122.88	5	16
61.44	122.88	1	2
76.8	122.88	5	8
122.88	122.88	2	2
153.6	122.88	5	4
245.76	122.88	4	2
307.2	122.88	5	2

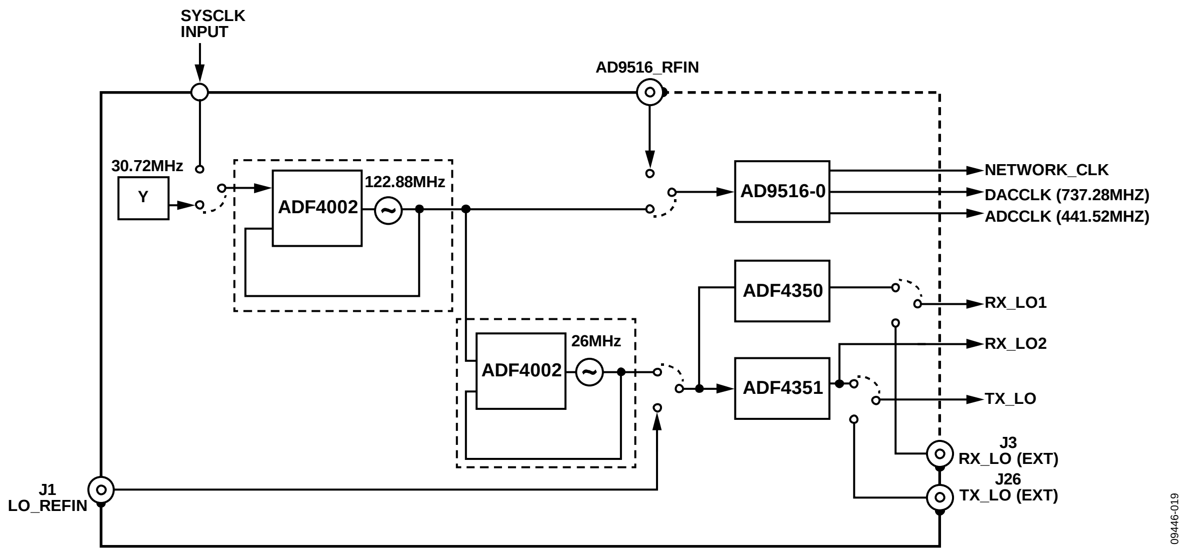

Figure 19. Block Diagram of Clock Path

The AD9516-0 clock generator and distribution chip accepts the clean 122.88 MHz source and synthesizes the DAC clock, the ADC clock, and the network clock output. The AD9516-0 is configured for one primary internal frequency of operation, 2949.12 MHz. Other frequencies are possible; however, this one hits a number of common sample rates for the data converters as well as various network clock rates used for the SERDES Tx clock.

Table 4 shows the clock rates that are possible with this frequency of operation. Other configurations are possible with another AD9516-0 primary frequency. Still others are possible by substituting a different VCXO frequency and/or replacing the AD9516-0 with a different speed option. The frequencies listed provide solutions to common configurations. While the board as built can support any of the required SERDES input clocks with a fixed MSDPD frequency plan, different frequency plans are required between 153.6 MHz and 122.88 MHz.

Table 4. AD9516-0 Clock Output Rates

AD9516-0 VCO (MHz)	ADCCLK (MHz)	DACCLK (MHz)	NETWORK_CLK (MHz)
2949.12	245.76, 368.64, 491.52	491.52, 737.28	368.64

Under these operating conditions, a typical phase noise curve is shown in Figure 20 for the ADC clock. Integrated out, this is approximately 550 f_S of clock jitter and, for the observation path, this yields an SNR of about 69 dB for a full-scale CW tone. For modulated waveforms, however, SNR is limited by the thermal noise of the mixer and drive amplifier.

For the DAC, the SNR impact is much smaller by the ratio of jitter to the DAC clock period.

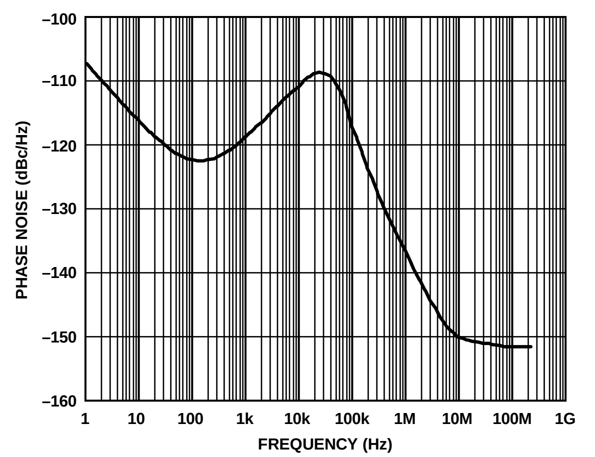

Figure 20. Typical Phase Noise of ADC Clock at 491.52 MHz

To synthesize both the Tx and Rx local oscillators, the clean 122.88 MHz reference is used to generate a second 26.0 MHz reference. This is the purpose of the second ADF4002. The output drives both the ADF4350 and ADF4351 PLLs. The 26.0 MHz reference permits a proper raster and a wide range of oscillator frequencies is possible for both up conversion and down conversion.

Two separate LOs are required because the Tx and Rx paths operate with different IF frequencies. The transmit path LO is produced by the ADF4351, and the observation receive LO is produced by the ADF4350.

For the observation path, the IF is nominally chosen to sit in the middle of the ADC Nyquist zone. With a sample rate of 491.76 MSPS, a nominal IF of 368.64 MHz is possible because it is in the middle of the second Nyquist zone. The DAC operates with an IF frequency of 184.32 MHz.

ADF4002 (1) Placement

A photo of the ADF4002 (1) placement is shown in Figure 21. The input reference can come from the on-board 30.72 MHz crystal (Y6) or the SMA connector, SYSCLK_IN (J5). It can also be passed from the FPGA through the FMC or HSMC connector. The synthesized 122.88 MHz output of the ADF4002 (1) is buffered with the ADCLK925 (U11) and distributed to the AD9516 and the second ADF4002 (2). When the PLL is locked, CR1 is illuminated.

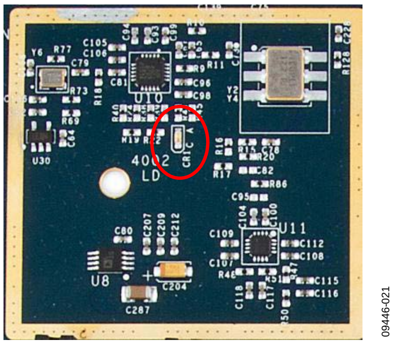

Figure 21. ADF4002 (1) Placement

The loop filter for this clock clean-up PLL is designed with a cutoff frequency of 832 Hz and a charge pump current of 5.11 mA. Figure 22, Table 5, and Figure 23 show the loop filter design and frequency response.

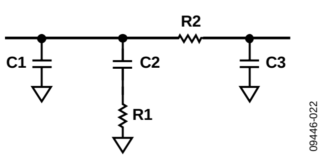

Figure 22. ADF4002 (1) Loop Filter Design

Table 5. ADF4002 (1) Loop Filter Design Values

Component	Value
C1	5.6 nF
C2	0.68 µF
R1	620 Ω
R2	1.3 kΩ
C3	0.022 µF

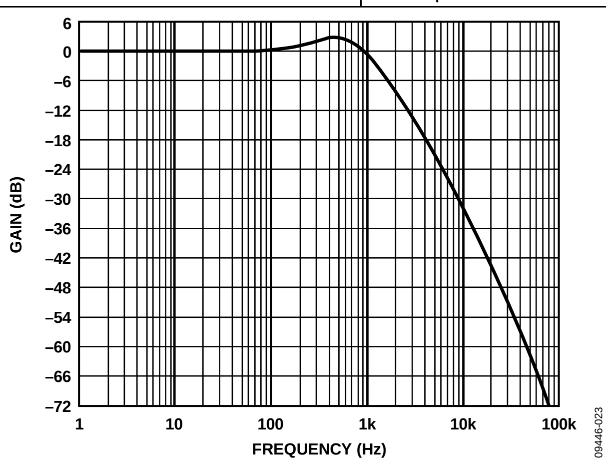

Figure 23. ADF4002 (1) Loop Filter Frequency Response

ADF4002 (2) Placement

A photo of the ADF4002 (2) placement is shown in Figure 24. The reference input for the second ADF4002 (2) is a buffered version of the synthesized 122.88 MHz reference from the first ADF4002 cleanup stage. JP47 can be shorted to provide a 26.0 MHz external reference out of J1 to be used for instrument synchronization. The 26.0 MHz output of the second ADF4002 (2) is buffered with the ADCLK905 and distributed to both the ADF4350 and ADF4351 for Rx/Tx LO generation. When this PLL is locked, CR2 is illuminated.

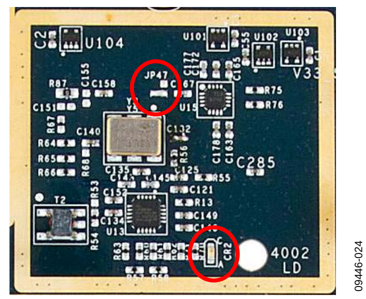

Figure 24. ADF4002 (2) Placement

The loop filter for this second clean-up PLL is designed with a cutoff frequency of 22.1 Hz and a charge pump current of 5.11 mA. Figure 25, Table 6, and Figure 26 show the loop filter design and frequency response.

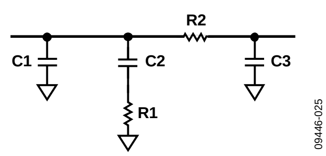

Figure 25. ADF4002 (2) Loop Filter Design

Table 6. ADF4002 (2) Loop Filter Design Values

Component	Value
C1	5.6 nF
C2	2.2 µF
R1	4.99 kΩ
R2	1.3 kΩ
C3	0.022 µF

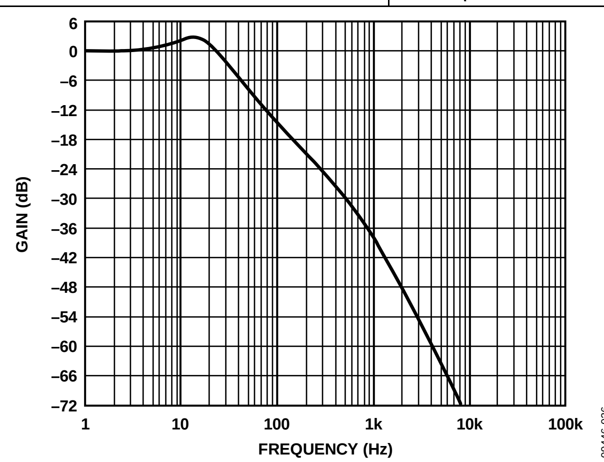

Figure 26. ADF4002 (2) Loop Filter Frequency Response

AD9516-0 Placement

A photo of the AD9516-0 placement is shown in Figure 27. The input reference for the AD9516-0 is a buffered version of the synthesized 122.88 MHz clock from the clock clean-up PLL. Alternatively, solder jumpers, JP20 and JP21, can be changed to accept an external reference input of N × 30.72 MHz at the SMA connector, 9516_REFIN. The DAC and ADC clocks are LVPECL outputs and are directly routed differentially to the DAC and ADC on internal layers of the board. The network clock output is LVDS and can be passed back to the FPGA either over the HSMC or FMC connector or through two SMA connectors, J7 and J8. When the AD9516-0 is locked, CR3 is illuminated.

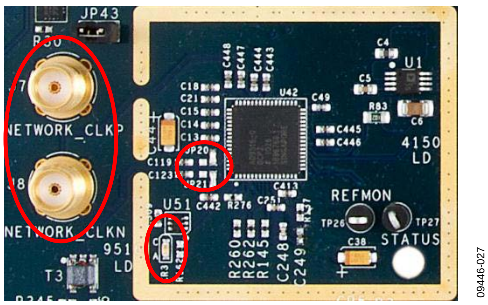

Figure 27. AD9516-0 Placement

The loop filter design and frequency response for the AD9516-0 are shown in the Figure 28, Table 7, and Figure 29. The loop filter for this part is designed with a cutoff frequency of 30 kHz with a maximum charge pump current of 4.8 mA.

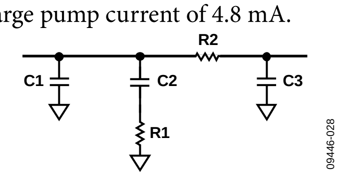

Figure 28. AD9516-0 Loop Filter Design

Table 7. AD9516-0 Loop Filter Design Values

Component	Value
C1	12 nF
C2	220 nF
R1	52.3 Ω
R2	107 Ω
C3	5.6 nF

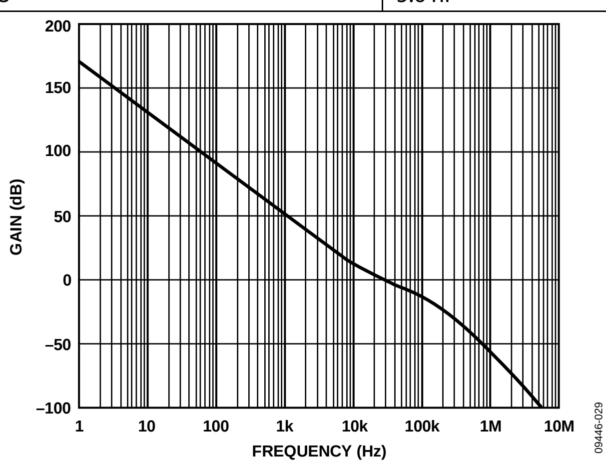

Figure 29. AD9516-0 Loop Filter Frequency Response

ADF4351 Placement

A photo of the ADF4351 placement is shown in Figure 30. The input to the ADF4351 is the 26.0 MHz output from the second ADF4002 (2) PLL. The ADF4351 has an integrated VCO and can produce outputs from 35 MHz to 4400 MHz. The primary output of the ADF4351 is routed to the Rx passive mixer (LO2); however, it is configured as an open on the printed circuit board (PCB). The auxiliary output of the ADF4351 is routed to the Tx quadrature modulator. When the ADF4351 is locked, CR4 is illuminated.

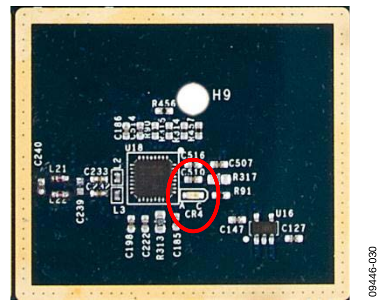

Figure 30. ADF4351 Placement

The loop filter design and frequency response for the ADF4351 are shown in the Figure 31, Table 8, and Figure 32. The loop filter for this part is designed with a cutoff frequency of 7.5 kHz with a maximum charge pump current of 2.5 mA.

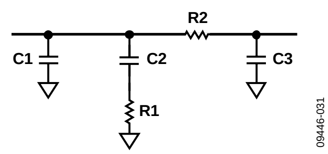

Figure 31. ADF4351 Loop Filter Design

Table 8. ADF4351 Loop Filter Design Values

Component	Value
C1	10 nF
C2	1 µF
R1	32.4 Ω
R2	64.9 Ω
C3	10 nF

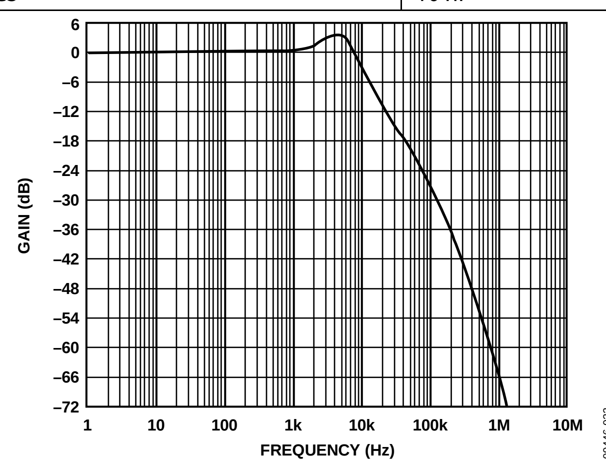

Figure 32. ADF4351 Loop Filter Frequency Response

ADF4350 Placement

A photo of the ADF4350 placement is shown in Figure 33. The input to the ADF4350 is the 26.0 MHz output from the second ADF4002 (2) PLL. The ADF4350 has an integrated VCO and can produce outputs from 137.5 MHz to 4400 MHz. The primary output of the ADF4350 goes to the Rx passive mixer (LO input 1). When the ADF4350 is locked, CR6 is illuminated.

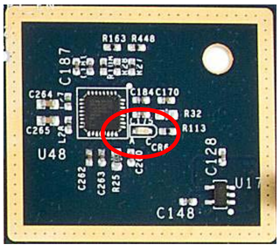

Figure 33. ADF4350 Placement

If the ADF4350 is not being used to generate the Rx LO, the output can be connected to an SMA connector (J3) to produce higher frequency network clock outputs. This can be done by installing a 0 Ω resistor at R52 on the backside of the board near the passive mixer.

The loop filter design for the ADF4350 is the same as the ADF4351; however, the maximum charge pump current is 3.75 mA. Therefore, there is a slightly different frequency response (see Figure 34).

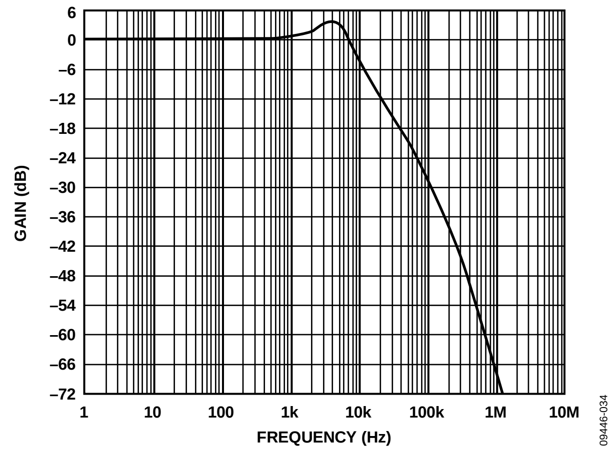

Figure 34. ADF4350 Loop Filter Frequency Response

TRANSMIT

A block diagram of the transmit path of the MSDPD Dashboard is shown in Figure 35.

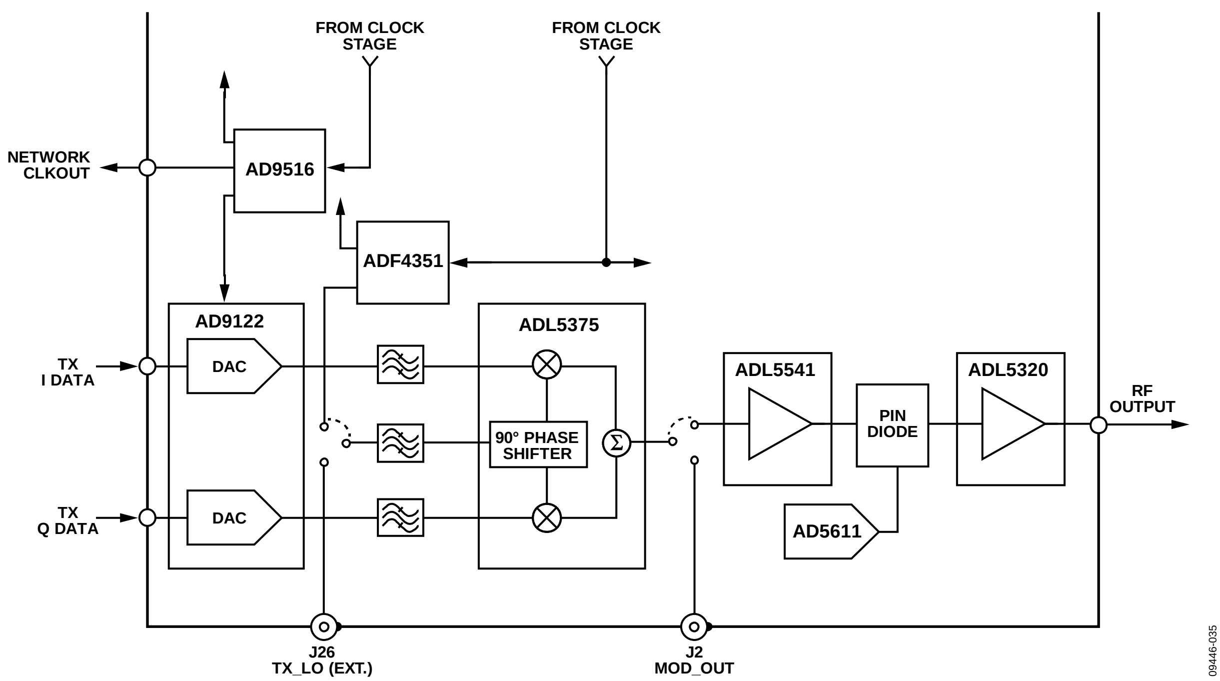

Figure 35. Block Diagram of Transmit Path

The AD9122 dual DAC takes data in at a baseband data rate of 368.64 MSPS and interpolates it by 2 to an end rate of 737.28 MSPS. Two modes of operation are possible: zero IF (ZIF) and complex IF (CIF). For CIF, the on-chip complex modulation is used to shift the output up to 184.32 MHz, which separates the image and dc offset from the desired signal for ease of filtering. For both ZIF and CIF architectures, the phase, gain, and offset compensation included in the AD9122 can be used for image and LO leakage suppression.

The AD9122 is followed by a fifth-order, low-pass filter with a cutoff frequency of 320 MHz. This filter removes the unwanted DAC images and attenuates any clock related spurs.

The ADL5375 is then used to combine the LO and the DAC output data to form the RF output. The operation can be run as a direct up conversion or as a complex IF up conversion. This is configured by using the modulation in the DAC or not. In addition, the ADL5375 supports a disable function that allows the output to be disabled during the Rx portion of a TDD burst. This feature is supported through the FPGA resource connector.

The ADL5375 is followed by a 3 dB PI attenuator network designed for an input/output impedance of 50 Ω. The PI attenuator is necessary to use the maximum dynamic range through the DAC and modulator and still achieve optimal IMD performance through the amplification stages that follow.

The ADL5541 is used to provide 15 dB power gain to the modulated output so that the RF drive amplifier can adequately drive the PA.

The MA4VAT2007-1061T (optimized for 1.5 GHz to 2.5 GHz) or the MA4VAT907-1061 (optimized for 0.6 GHz to 1.2 GHz) PIN diode attenuators are used to control the gain of the Tx path and provide ~15 dB of Tx gain control. An analog control voltage generated by a 10-bit AD5611 nanoDAC controls the PIN diode. These diodes have a roughly 15 dB range controlled by a 0 V to 3 V signal that the DAC provides.

The ADL5320 is used to drive the external RF power amplifier and provides about 14 dB of gain at 2150 MHz. Output drive level should be 17 dBm with a full-scale sine wave input. The ADL5320 serves frequencies between 400 MHz and 2.7 GHz.

Gain Analysis (Transmit)

The expected full-scale CW output power of the transmitter with maximum and minimum gain varies depending on the RF band of the board and the IF chosen. The gain analysis at an RF frequency of 2150 MHz with an IF of 184.32 MHz is shown in Table 9. For this gain analysis, a full-scale single-tone baseband waveform was loaded into the DAC, where it was then modulated up to an IF of 184.32 MHz. The ADL5375 then modulates the IF up to the final RF of 2150 MHz.

The output of the ADL5375 was measured directly at an SMA test point. The PI attenuator provides approximately 3 dB of attenuation, and the ADL5541 provides approximately 14.5 dB of gain at 2150 MHz. The PIN diode was adjusted to provide the minimum and maximum attenuation. The least amount of attenuation corresponds to an AD5611 nanoDAC input code of 0; however, the maximum attenuation point is variable depending on the operating frequency. The ADL5320 provides approximately 14 dB at 2150 MHz.

Table 9. Transmit Gain Analysis for 2150 MHz, CIF = 184.32 MHz

		Output Power (dBm)			
Attenuation	Input (dBFS)	ADL5375	ADL5541	P_{IN} Diode	ADL5320
Maximum	0	−4.3	+7.4	−9.1	+4.1
Median	0	−4.3	+7.4	−3.7	+9.6
Minimum	0	−4.3	+7.4	+3.7	+16.9

The typical maximum full-scale output power is 17 dBm and the gain control range is approximately 13 dB for the 2150 RF operating frequency. Further gain control can be implemented in the digital domain.

For all other board models, refer to Table 10 for the typical maximum and minimum output powers using a full-scale CW.

Table 10. Typical Output Power and Gain Range per Board Model

	Output Power (Typ)			
RF Band (MHz)	Maximum (dBm)	Minimum (dBm)	Gain Control Range (dB)	Board Model
900	24	2.5	21.5	1
1850	20	3.5	16.5	2
2000	18.5	4	14.5	2
2150	17	4	13.0	2
2350	17	4.5	12.5	3
2500	16.5	6.5	10.0	3
2600	16	5.5	10.5	3

AD9122 Placement

A photo of the placement of the AD9122 is shown in Figure 36. The AD9122 is set up by default to accept 16-bit I/Q data at 368.64 MSPS double data rate (DDR) and interpolate by 2× to a final DAC update rate of 737.28 MSPS. The DAC sample rates can be altered; however, this may have implications on the input signal bandwidth and the low-pass filter design. The NCO of the DAC, which has a maximum speed of 550 MHz, is not supported in the Gen1.6 Dashboard.

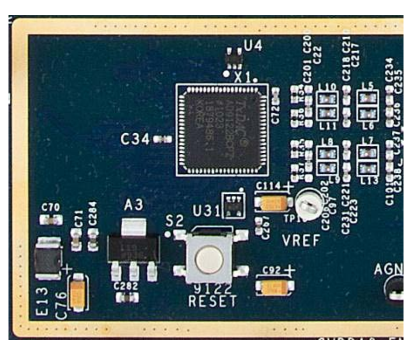

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Figure 36. AD9122 Placement

The AD9122 is connected to the ADL5375 quadrature modulator through a fifth-order, low-pass Butterworth filter. The filter design is shown in Figure 37, and the measured frequency response of the DAC + the LPF + the modulator is shown in Figure 38. With the inverse sinc roll-off calibrated out from the frequency response for optimal performance, the flatness from dc to 250 MHz is within ±0.7 dB.

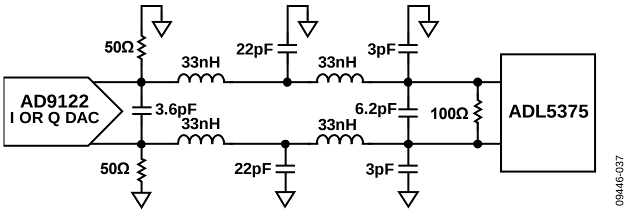


Figure 37. Low-Pass Filter Design

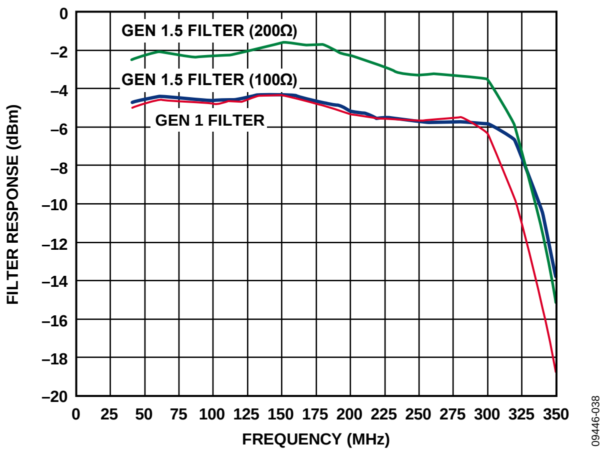


Figure 38. Frequency Response of the DAC + the Filter + the Modulator

ADL5375 Placement

A photo of the placement of the ADL5375 is shown in Figure 39. The filtered I and Q outputs from the AD9122 are routed to the ADL5375 inputs with matched length 100 Ω differential traces. The ADL5375 single-ended RF output is routed on a 50 Ω single-ended trace through an image rejection filter to the ADL5541 gain block.

For testing, the ADL5375 RF output can also be jumped to an SMA test point (J2) by adjusting the JP24 solder jumper. In addition, the LO input to the ADL5375 can either come from the ADF4351 (default) or can be supplied by an external source to an SMA connector (J26) by configuring the JP22 and JP23 solder jumpers.

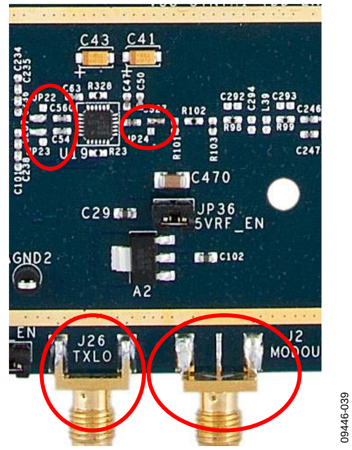


Figure 39. ADL5375 Placement

A 3 dB PI attenuator follows the quadrature modulator, as shown in Figure 40. The PI attenuator permits using the maximum dynamic range through the DAC and modulator and still achieves optimal IMD performance through the amplification stages that follow the modulator.

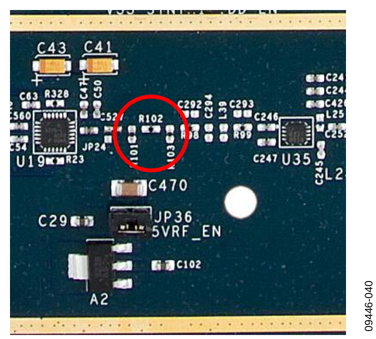


Figure 40. PI Attenuator

If desired, there is space to include an image rejection filter. The structure of the image rejection filter is shown in Figure 41. It is not populated on the MSDPD by default. Instead the image rejection and LO leakage can be attenuated by using the gain, phase, and offset compensation features in the AD9122. Refer to the factory calibration settings located on the inventory label for the MSDPD board for these values.

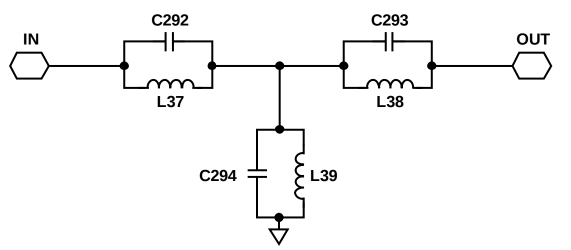


Figure 41. Topology of Tx Image Rejection Filter

ADL5541, ADL5320, and PIN Diode Placement

A photo of the placement of the RF amplifiers and PIN diode gain block is shown in Figure 42.

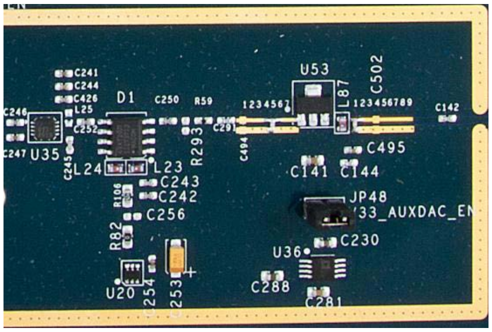


Figure 42. ADL5541, ADL5320, and PIN Diode Placement

Following the ADL5375 quadrature modulator is the ADL5541 fixed gain RF amplifier that provides close to 15 dB of gain across the frequency bands that the MSDPD Dash board supports. The input/output of this amplifier is internally matched to 50 Ω.

The next block in the transmit gain lineup is the PIN diode attenuator. The M/A-Com MA4VAT2007-1061T (or the Skyworks AV102-12) PIN diode is suitable for operation in all of the RF frequency bands of interest with the exception of the 900 MHz band. For the 900 MHz band, the pin compatible M/A-Com MA4VAT907-1061T (or Skyworks AV101-12) PIN diode is installed. The typical insertion loss for these PIN diodes is 1.5 dB, and the attenuation range is not constant over frequency (see Table 10).

The PIN diode's control voltage and therefore its attenuation come from the AD5611 10-bit nanoDAC with a useful output voltage range of 0 V to 3.3 V. Maximum attenuation, however, is achieved with a PIN diode control voltage from between 2.7 V to 3.3 V, depending on frequency and vendor. Therefore, the useful range of the nanoDAC input codes can be reduced from the full 1024 values.

Following the PIN diode attenuator is the PA driver amplifier, the ADL5320. The ADL5320 covers the entire frequency range of the board; however, the gain is not flat over frequency. The typical gain per RF band is listed in Table 11.

Table 11. Typical ADL5320 Gain vs. RF Band

RF Band (MHz)	ADL5320 Gain (dB)
900	17
1850	13.5
2000	13
2150	13
2350	12.5
2500	12
2600	12.5

The input and output matching networks for the ADL5320 also change over frequency. The capacitor and inductor values change as well as the matching component spacing to allow for amplifier tuning. See Figure 43 for the location of these input/output matching components. Based on the MSDPD Dashboard model selected, the appropriate values and component spacing is assembled as listed in Table 12.

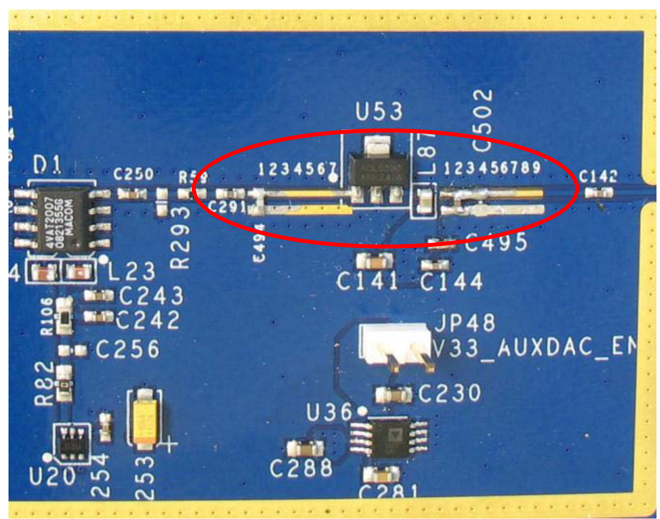


Figure 43. Location of ADL5320 Tuning Components

Table 12. Tuning the ADL5320

				C494		C502		
Board Model	**C142 (pF)**	**C144 (pF)**	**C291 (pF)**	**Value (pF)**	**Position**	**Value (pF)**	**Position**	**L87 (nH)**
1	47	100	47	6.8	3	2.2	2	68
2	10	22	22	0.5	1	2.2	4	15
3	10	12	12	1.0	3	1.0	2	15

The full transmitter frequency response for each RF band was measured using a wide band input signal placed in the center of the RF band. Table 13 reports the Tx flatness across 30 MHz, 60 MHz, 120 MHz, and 250 MHz bandwidths. This data was taken using the inverse sinc compensation features in the AD9122 DAC.

RECEIVE

A block diagram of the observation receive signal path is shown in Figure 44.

The intent is to lightly couple this circuit to the PA output through a directional coupler that drops the power to a level suitable for observation. The input is initially attenuated before being sent to the ADL5365/ADL5367 mixer that is responsible for directly mixing down the observed RF signal to a suitable IF. The typical IF frequency is 368.64 MHz; however, it can be changed based on application requirements. The IF signal is then filtered and passed onto an AD8375 DVGA that provides 20 dB of optional gain. The DVGA ensures that the full dynamic range of the ADC can be used. An antialias filter removes harmonics and other out-of-band signals before the signal is digitized with an AD9434 or AD6641 12-bit ADC.

Table 13. Typical Tx Pass Band Flatness vs. RF Band Center

		Tx Flatness (dB)			
Board Model	**RF Band Center (MHz)**	**30 MHz Bandwidth**	**60 MHz Bandwidth**	**120 MHz Bandwidth**	**250 MHz Bandwidth**
1	900	±0.20	±0.25	±0.35	±0.35
2	1850	±0.25	±0.40	±0.70	±0.70
2	2000	±0.30	±0.30	±0.60	±0.60
2	2150	±0.25	±0.30	±0.50	±0.50
3	2350	±0.20	±0.35	±0.55	±0.55
3	2500	±0.30	±0.30	±0.30	±0.30
3	2600	±0.15	±0.50	±0.60	±0.60

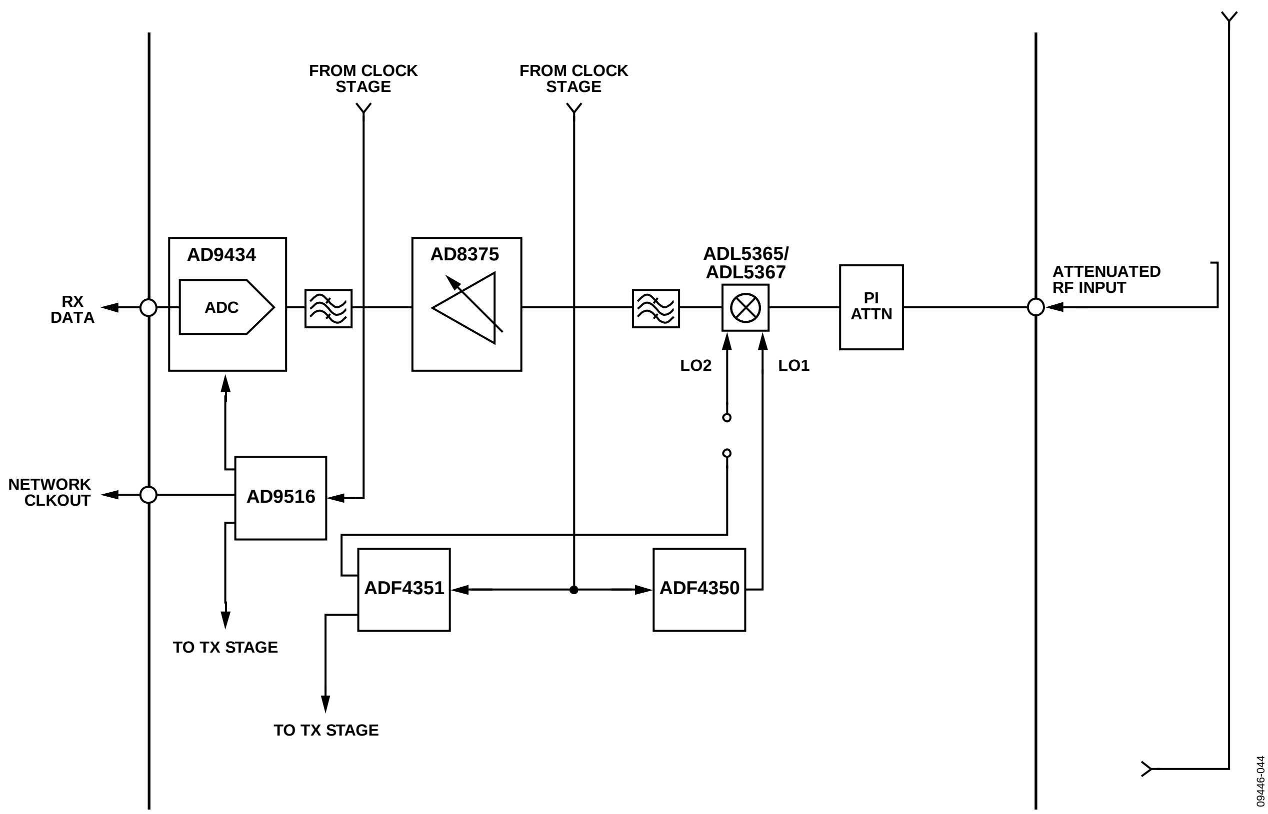


Figure 44. Observation Receiver Block Diagram

Gain Analysis (Receive)

With the AD8375 set for unity gain (0 dB), there appears to be a 22.5 dB of loss through the observation receive signal path from RF input to ADC output. There is first 15 dB of physical loss. This consists of 3 dB through the PI attenuator, 7.5 dB of conversion loss across the ADL5365/ADL5367 mixer, and 4.5 dB through the two filters.

In addition to the physical loss, however, consideration must be given to the fact that the ADC requires a 7.5 dBm input to produce a full-scale digital output (0 dBFS). Said another way, the ADC always produces an output (in dBFS) that is 7.5 dB less than its input (in dBm, 50 Ω). This 7.5 dB therefore adds to the 15 dB of physical loss. As an example, consider a 0 dBm signal applied to the RF input. This signal undergoes loses and results in −15 dBm at the input to the ADC. In addition, this input produces an ADC output of −22.5 dBFS.

This is important when attempting to optimize the input level to the observation receive signal chain. Optimizing the level applied to the RF input is critical to optimizing algorithm performance. Digital predistortion algorithms depend on good IMD performance, and this depends on a careful mix of attenuation and amplification at each stage in the signal path.

Figure 45 shows the IMD performance of the signal path for different values of AD8375 DVGA gain. For different amplifier settings, there is a small range of input power levels that result in optimal IMD performance (see Figure 45). In addition, the highest IMD performance is realized with the highest amplifier gain. This is because the ADL5365/ADL5367 balanced mixer dominates the IMD performance. In general, it is best to drive the mixer with lower input levels and then use the DVGA to boost the signal ahead of the ADC.

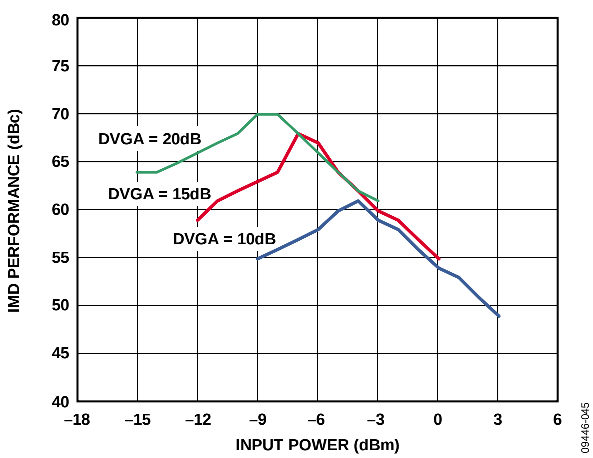


Figure 45. Rx IMD Performance vs. Input Power Level at 2140 MHz

According to Figure 45, an optimal input power level of −8 dBm and a DVGA gain setting of 20 dB produces the least amount of intermodulation distortion. This input undergoes the previously detailed 22.5 dB of loss; however, this is mostly offset by the 20 dB of gain in the amplifier. Thus, an optimal input under these conditions yields −10.5 dBFS of signal at the output of the ADC.

Higher levels at the RF input use more of the dynamic range of the ADC, and this can be useful to optimize SNR. Figure 46 shows how input power levels affect signal-to-noise (SNR) performance.

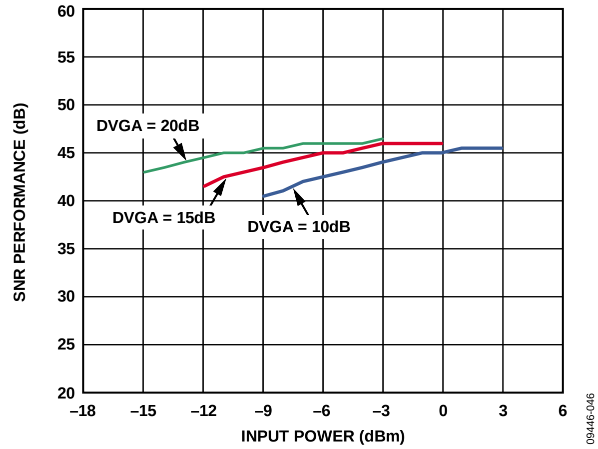


Figure 46. Rx SNR Performance vs. Input Power Level at 2140 MHz

ADL5365/ADL5367 Placement

A photo of the placement of the ADL5365/ADL5367 is shown in Figure 47. The ADL5367 is installed for 900 MHz evaluation platforms, and the ADL5365 is installed for all other frequency ranges. The ADL5365/ADL5367 support an enable feature that allows functionality to be suspended during the Rx portion of a TDD timeslot. The enable signal is passed to the FPGA host board for fast control.

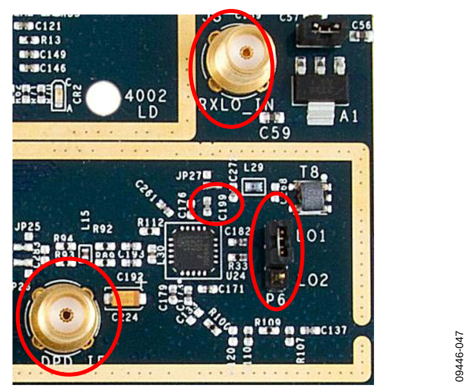


Figure 47. ADL5365/ADL5367 Placement

The ADL5365/ADL5367 receive the PA output in a highly attenuated form and mix the RF frequency down by the LO frequency. The PI attenuator that precedes the mixer was designed for 50 Ω input/output impedance and provides approximately 3 dB of attenuation across the 700 MHz to 2700 MHz band.

The ADL5365/ADL5367 have two LO inputs, and the MSDPD Dashboard provides two LO options. In addition, there is an option to use an external LO. The user can switch between LO1 and LO2 on the mixer by setting Jumper P6. By default, the board uses LO1, generated from the ADF4350, and this allows the Rx path to use a different IF frequency than the Tx path. If LO2 is selected, the Rx and Tx LO both come from the ADF4351 and, therefore, must use the same IF.

To use LO2, set Jumper P6, populate L4 (3.3 nH near T7 on the back side of the board), and depopulate C199 (next to the ADL5365/ADL5367) to physically isolate the mixer from LO1. To use an externally provided LO, make sure L4 is not installed and modify Solder Jumper JP27. Connect the LO source to J3, RXLO_IN.

The IF output from the ADL5365/ADL5367 is filtered using a third-order, high-pass Butterworth filter and is provided to the ADC drive amplifier, the AD8375, as shown in Figure 48. The pass band for this filter begins at 140 MHz.

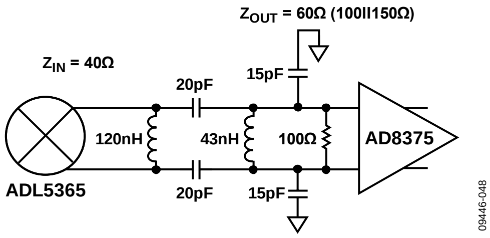


Figure 48. Receive Chain, ADL5365 to AD8375

Optionally, solder jumpers, JP25 and JP26, can be modified to observe a transformer-coupled version of the mixer output at the connector, DPD_IF. Using this SMA connection, the power conversion gain can be measured from the RF input to the IF output.

AD8375 Placement

A photo of the placement of the AD8375 DVGA is shown in Figure 49. The AD8375 is used to buffer the input to the observation ADC, to provide isolation and constant output impedance to the passive mixer, and to provide any required gain control or conditioning to the IF signal. There is a 5-bit digital word input used to set the gain of the device. The gain for the AD8375 is 20 dB (Code = 00000) to −4 dB (Code ≥11000) in 1 dB steps. The output of the DVGA is matched to the ADC input through the antialiasing filter.

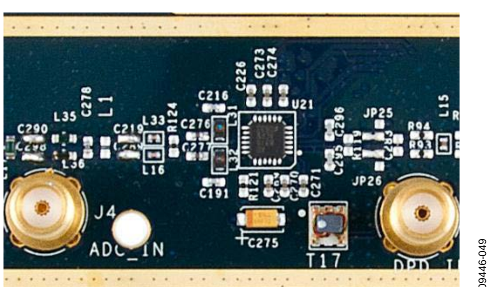


Figure 49. AD8375 Placement

ADC Options

One of two possible ADC options is populated on the MSDPD Dashboard evaluation platform. See the AD6641 or AD9434 section for full details and slight circuit differences regarding these two choices. The remainder of this section is common to either device.

A photo of the ADC placement is shown in Figure 50. To evaluate the ADC in standalone mode, modify Solder Jumper JP28 and Solder Jumper JP42 and connect an analog input directly to SMA Connector J4.

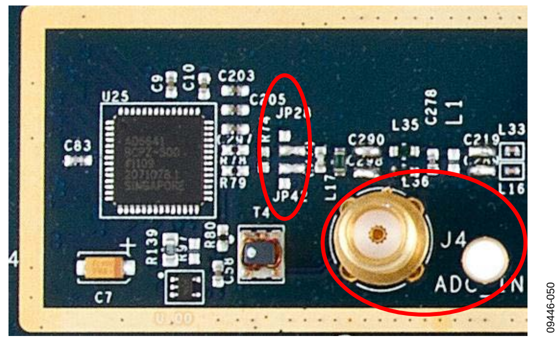


Figure 50. ADC Placement

For the MSDPD Dashboard evaluation platform, the default ADC clock rate is 491.52 MSPS. At this sample rate, the IF can be configured to be in the middle of the second Nyquist zone at 368.64 MHz giving better than 100 MHz above and below for usable bandwidth.

The analog input of the ADC is from the AD8375 DVGA after passing through an antialiasing filter. The filter was designed as a band-pass filter for the frequencies from 115 MHz to 600 MHz and provides 150 Ω load impedance to the DVGA. The filter structure and filter simulated frequency response is shown in Figure 51 and Figure 52, respectively. The complete frequency response of the observation path was measured at the ADC output by inputting a single-tone RF signal at DPD_IN. The frequency response vs. IF is shown in Figure 53.

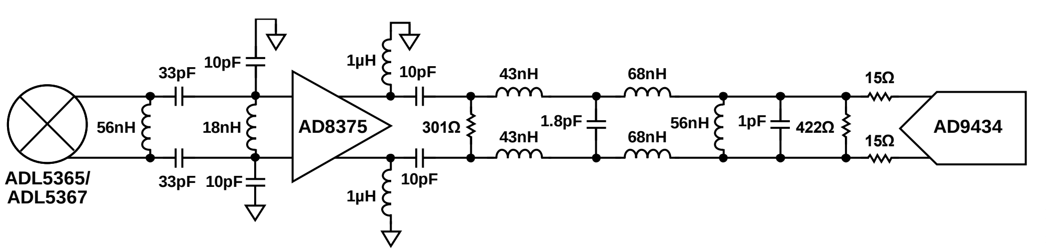


Figure 51. Antialiasing Filter Structure

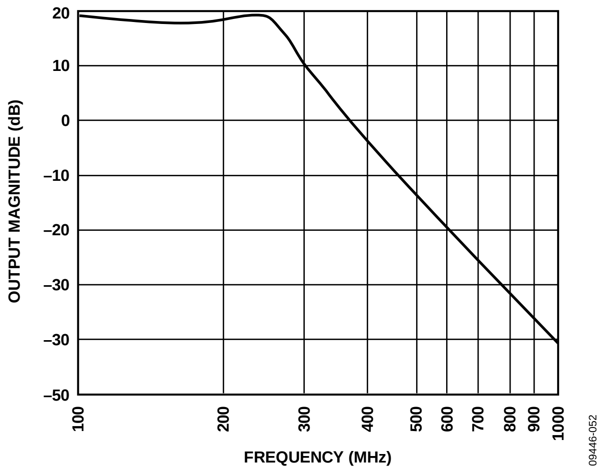


Figure 52. Antialiasing Filter Simulated Frequency Response

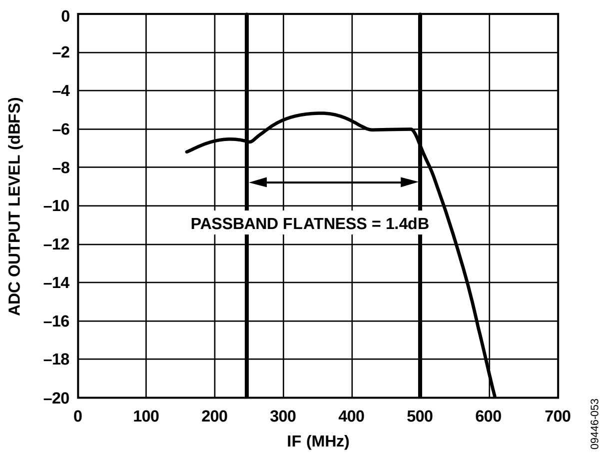


Figure 53. Observation Path Frequency Response vs. IF

AD6641 or AD9434 (ADC Choices)

The AD6641 or the AD9434 are the two possible choices for the ADC. Both devices are high performance 12-bit ADCs featuring internal 500 MSPS sampling cores; however, interfacing to output data is significantly different in each case. Refer to the ADC Bus section for full details.

The AD6641 is optimized for use in DPD observation receiver applications in China. It contains an internal 16K deep FIFO. ADC samples are retrieved via one of several low speed bus options with a maximum readback rate of $f_{ADC}/8$. The AD9434 is deployed for observation receiver applications in areas of the world outside of China. It features a DDR LVDS output bus operating at the 491.52 MSPS sample rate.

Both ADCs are pin similar and interchangeable on the PCB with minor circuit changes, as noted in Table 14 and Table 15.

Table 14 Component Values AD6641 vs. AD9434 for MSDPD X (Xilinx)

Component	AD6641	AD9434
R84	0 Ω	Do not install
R85	Do not install	0 Ω
R97	Do not install	0 Ω

Table 15. Component Values AD6641 vs. AD9434 for MSDPD A (Altera)

Component	AD6641	AD9434
R86	0 Ω	Do not install
R87	Do not install	0 Ω
R97	Do not install	0 Ω

FPGA INTERFACE

The FPGA interface definition provides details of the connector responsible for passing data between the FPGA resource and the MSDPD active devices. This includes the primary data paths between the data converters and the FPGA as well as all control channels. In addition, certain timing and clock signals are available for data timing, clock clean up, and other related functions. RF signals are not passed through this port.

Two FPGA interfaces are supported, Altera and Xilinx. Each has evaluation boards, and MSDPD Dashboard evaluation platform kits are available with compatible connectors. Both vendors also have DPD framework software available to shorten development time. In terms of data retrieval from the Rx path of the MSDPD dashboard evaluation platform, Altera's framework supports the AD9434 ADC only. To evaluate the Altera system using the AD6641, users are responsible for creating their own FPGA code for this interface. See the ADC Bus section for full details. The Xilinx framework is available for both the AD9434 and AD6641 ADCs.

ALTERA HSMC CONNECTOR DETAILS

The AD-MSDPDA-9434/AD-MSDPDA-6641 board supports a Class II High Speed Mezzanine Card (HSMC) interface as defined by the HSMC specification. The Altera Stratix IV GX FPGA development kit includes HSMC connectors (see Figure 54).

Table 16 describes in detail how the HSMC is mapped to mixed signal resources. Note that although the AD6641 signal pins are included in this description, Altera's framework software does not support the data interface of this ADC.

09446-054

Figure 54. Altera Stratix IV GX Development Board with HSMC Interface

Table 16. HSMC Mapping to Mixed Signal Resources

HSMC Pin	HSMC Signal	MSDPD Signal
1 bank1	XCVR_TXp7	
2	XCVR_RXp7	
3	XCVR_TXn7	
4	XCVR_RXn7	
5	XCVR_TXp6	
6	XCVR_RXp6	
7	XCVR_TXn6	
8	XCVR_RXn6	
9	XCVR_TXp5	
10	XCVR_RXp5	
11	XCVR_TXn5	
12	XCVR_RXn5	
13	XCVR_TXp4	
14	XCVR_RXp4	
15	XCVR_TXn4	
16	XCVR_RXn4	
17	XCVR_TXp3	
18	XCVR_RXp3	

HSMC Pin	HSMC Signal	MSDPD Signal
19	XCVR_TXn3	
20	XCVR_RXn3	
21	XCVR_TXp2	
22	XCVR_RXp2	
23	XCVR_TXn2	
24	XCVR_RXn2	
25	XCVR_TXp1	
26	XCVR_RXp1	
27	XCVR_TXn1	
28	XCVR_RXn1	
29	XCVR_TXp0	
30	XCVR_RXp0	
31	XCVR_TXn0	
32	XCVR_RXn0	
33	SDA	SCLK_MAIN
34	SCL	SDO_MAIN
35	JTAG_TCK	
36	JTAG_TMS	
37	JTAG_TDO	Connect to Pin 38, JTAG_TDI
38	JTAG_TDI	Connect to Pin 37, JTAG_TDO
39	CLKOUT0	
40 bank1	CLKIN0	
41 bank2	D0	Q2_P
42	D1	Q2_N
43	D2	ADL5365_EN_25 (2.5 V)
44	D3	ADL5375_EN_25 (2.5 V)
45	3.3V	
46	12V	
47	LVDS_TXp0	P15, 1.8 V LVDS DAC data (MSB)
48	LVDS_RXp0	AD9434_0 LVDS ADC data (LSB)
49	LVDS_TXn0	P15, 1.8 V LVDS DAC data
50	LVDS_RXn0	AD9434_0B LVDS ADC data
51	3.3V	
52	12v	
53	LVDS_TXp1	P14, 1.8 V LVDS DAC data
54	LVDS_RXp1	AD9434_1 LVDS ADC data
55	LVDS_TXn1	P14, 1.8 V LVDS DAC data
56	LVDS_RXn1	AD9434_1B LVDS ADC data
57	3.3V	
58	12V	
59	LVDS_TXp2	P13, 1.8 V LVDS DAC data
60	LVDS_RXp2	AD9434_2 LVDS ADC data
61	LVDS_TXn2	P13, 1.8 V LVDS DAC data
62	LVDS_RXn2	AD9434_2B LVDS ADC data
63	3.3V	
64	12V	
65	LVDS_TXp3	P12, 1.8 V LVDS DAC data
66	LVDS_RXp3	AD9434_3 LVDS ADC data
67	LVDS_TXn3	P12, 1.8 V LVDS DAC data
68	LVDS_TXn3	AD9434_3B LVDS ADC data
69	3.3V	
70	12V	
71	LVDS_TXp4	P11, 1.8 V LVDS DAC data (MSB)

HSMC Pin	HSMC Signal	MSDPD Signal
72	LVDS_RXp4	AD9434_4 LVDS ADC data
73	LVDS_TXn4	P11, 1.8 V LVDS DAC data
74	LVDS_RXn4	AD9434_4B LVDS ADC data
75	3.3V	
76	12V	
77	LVDS_TXp5	P10, 1.8 V LVDS DAC data
78	LVDS_RXp5	AD9434_5 LVDS ADC data
79	LVDS_TXn5	P10, 1.8 V LVDS DAC data
80	LVDS_RXn5	AD9434_5B LVDS ADC data
81	3.3V	
82	12V	
83	LVDS_TXp6	P9, 1.8 V LVDS DAC data
84	LVDS_RXp6	AD9434_6 LVDS ADC data
85	LVDS_TXn6	P9, 1.8 V LVDS DAC data
86	LVDS_RXn6	AD9434_6B LVDS ADC data
87	3,3V	
88	12V	
89	LVDS_TXp7	P8, 1.8 V LVDS DAC data
90	LVDS_RXp7	AD9434_7 LVDS ADC data
91	LVDS_TXn7	P8, 1.8 V LVDS DAC data
92	LVDS_RXn7	AD9434_7B LVDS ADC data
93	3.3V	
94	12V	
95	CLKOUT1p	DAC_DCI_P (1.8 V LVDS)
96	CLKIN1p	DAC_DCO_P (LVDS)
97	CLKOUT1n	DAC_DCI_N (1.8 V LVDS)
98	CLKIN1n	DAC_DCO_N (LVDS)
99	3.3V	
100 bank2	12V	
101 bank3	LVDS_TXp8	P7, 1.8 V LVDS DAC data (MSB)
102	LVDS_RXp8	AD9434_8 LVDS ADC data
103	LVDS_TXn8	P7, 1.8 V LVDS DAC data
104	LVDS_RXn8	AD9434_8B LVDS ADC data
105	3.3V	
106	12V	
107	LVDS_TXp9	P6, 1.8 V LVDS DAC data
108	LVDS_RXp9	AD9434_9 LVDS ADC data
109	LVDS_TXn9	P6, 1.8 V LVDS DAC data
110	LVDS_RXn9	AD9434_9B LVDS ADC data
111	3.3V	
112	12V	
113	LVDS_TXp10	P5, 1.8 V LVDS DAC data
114	LVDS_RXp10	AD9434_10 LVDS ADC data
115	LVDS_TXn10	P5, 1.8 V LVDS DAC data
116	LVDS_RXn10	AD9434_10B LVDS ADC data
117	3.3V	
118	12V	
119	LVDS_TXp11	P4, 1.8 V LVDS DAC data
120	LVDS_RXp11	AD9434_11 LVDS ADC data
121	LVDS_TXn11	P4, 1.8 V LVDS DAC data
122	LVDS_RXn11	AD9434_11B LVDS ADC data
123	3.3V	
124	12V	

HSMC Pin	HSMC Signal	MSDPD Signal
125	LVDS_TXp12	P3, 1.8 V LVDS DAC data
126	LVDS_RXp12	AD9434_OR LVDS (overflow)
127	LVDS_TXn12	P3, 1.8 V LVDS DAC data
128	LVDS_RXn12	AD9434_ORB LVDS (overflow)
129	3.3V	
130	12V	
131	LVDS_TXp13	P2, 1.8 V LVDS DAC data
132	LVDS_RXp13	SDIO_MAIN
133	LVDS_TXn13	P2, 1.8 V LVDS DAC data
134	LVDS_RXn13	AD5611CSB
135	3.3V	
136	12V	
137	LVDS_TXp14	P1, 1.8 V LVDS DAC data
138	LVDS_TXp14	PORTCSB
139	LVDS_TXn14	P1, 1.8 V LVDS DAC data
140	LVDS_RXn14	ADF4350CSB
141	3.3V	
142	12V	
143	LVDS_TXp15	P0, 1.8 V LVDS DAC data
144	LVDS_RXp15	ADF4150CSB
145	LVDS_TXn15	P0, 1.8 V LVDS DAC data
146	LVDS_RXn15	AD9516CSB
147	3.3V	
148	12V	
149	LVDS_TXp16	ADF4002_LO_CSB
150	LVDS_RXp16	ADF4002_CLK_CSB
151	LVDS_TXn16	AD9434CSB
152	LVDS_RXn16	AD9122CSB
153	3.3V	
154	12V	
155	CLKOUT2p	NETWORK_CLKP (CLK to be cleaned up)
156	CLKIN2p	AD9434_DCO LVDS data clock out
157	CLKOUT2n	NETWORK_CLKN (CLK to be cleaned up)
158	CLKIN2n	AD9434_DCOB LVDS data clock out
159	3.3V	
160 bank3	PSNTn	Connects to ground on mezzanine card

XILINX FMC CONNECTOR DETAILS

The AD-MSDPDX-9434/AD-MSDPDX-6641 board supports an FMC interface as defined by Xilinx and the Vita-57 standard. The Xilinx ML605 FPGA development kit includes a FPGA mezzanine card (FMC) connector set.

Note that Xilinx has developed IP for DPD and/or peak cancellation crest factor reduction (PC-CFR) that can be made available to qualified customers. Contact Xilinx for further details.

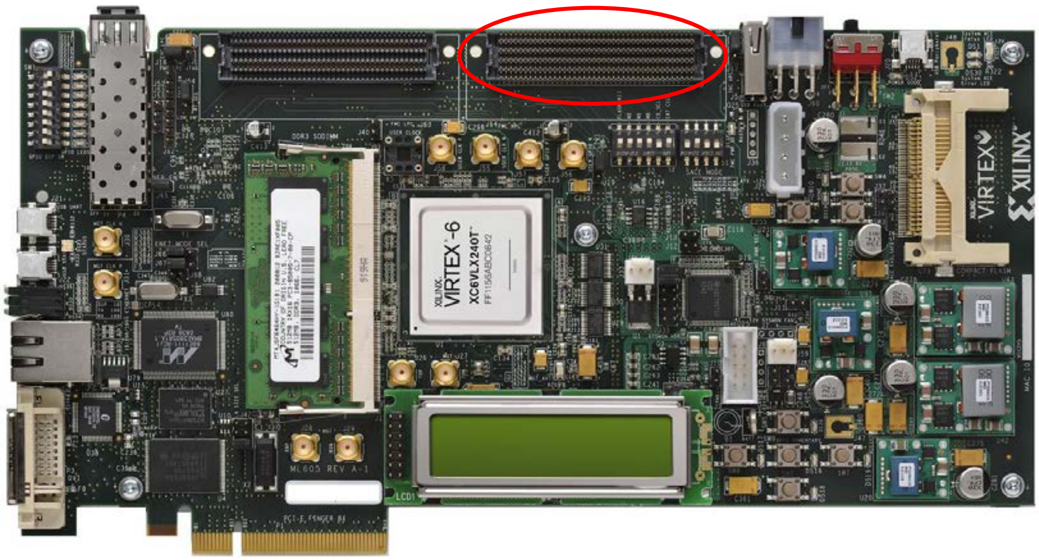


Figure 55. Xilinx ML605 Development Platform

Table 17 describes in detail how the FMC is mapped to mixed signal resources.

Table 17. FMC Mapping of Mixed Signal Resources

Group	Name	Signal Direction	FMC-HPC Pin	ML605 FMC-HPC Signal	FPGA Bank
ADC	AD9434_11/AD6641_DNC	To FPGA	G21	FMC_HPC_LA20_P	23
ADC	AD9434_11B/AD6641_DNC	To FPGA	G22	FMC_HPC_LA20_N	23
ADC	AD9434_10/AD6641_DNC	To FPGA	H22	FMC_HPC_LA19_P	23
ADC	AD9434_10B/AD6641_SPSDO	To FPGA	H23	FMC_HPC_LA19_N	23
ADC	AD9434_9/AD6641_PDOR	To FPGA	G24	FMC_HPC_LA22_P	23
ADC	AD9434_9B/AD6641_PDORB	To FPGA	G25	FMC_HPC_LA22_N	23
ADC	AD9434_8/AD6641_PD5	To FPGA	H25	FMC_HPC_LA21_P	23
ADC	AD9434_8B/AD6641_PD5B	To FPGA	H26	FMC_HPC_LA21_N	23
ADC	AD9434_7/AD6641_PD4	To FPGA	G27	FMC_HPC_LA25_P	23
ADC	AD9434_7B/AD6641_PD4B	To FPGA	G28	FMC_HPC_LA25_N	23
ADC	AD9434_6/AD6641_PD3	To FPGA	H28	FMC_HPC_LA24_P	23
ADC	AD9434_6B/AD6641_PD3B	To FPGA	H29	FMC_HPC_LA24_N	23
ADC	AD9434_5/AD6641_PD2	To FPGA	G30	FMC_HPC_LA29_P	23
ADC	AD9434_5B/AD6641_PD2B	To FPGA	G31	FMC_HPC_LA29_N	23
ADC	AD9434_4/AD6641_PD1	To FPGA	H31	FMC_HPC_LA28_P	23
ADC	AD9434_4B/AD6641_PD1B	To FPGA	H32	FMC_HPC_LA28_N	23
ADC	AD9434_3/AD6641_PD0	To FPGA	G33	FMC_HPC_LA31_P	23
ADC	AD9434_3B/AD6641_PD0B	To FPGA	G34	FMC_HPC_LA31_N	23
ADC	AD9434_2/AD6641_PCLK	To FPGA	H34	FMC_HPC_LA30_P	23
ADC	AD9434_2B/AD6641_PCLKB	To FPGA	H35	FMC_HPC_LA30_N	23
ADC	AD9434_1/AD6641_DNC	To FPGA	G36	FMC_HPC_LA33_P	23
ADC	AD9434_1B/AD6641_DUMP	To FPGA	G37	FMC_HPC_LA33_N	23
ADC	AD9434_0/AD6641_EMPTY	To FPGA	H37	FMC_HPC_LA32_P	23

Group	Name	Signal Direction	FMC-HPC Pin	ML605 FMC-HPC Signal	FPGA Bank
ADC	AD9434_0B/AD6641_FULL	To FPGA	H38	FMC_HPC_LA32_N	23
ADC	AD9434_OR/AD6641_SPSCLK	To FPGA	D26	FMC_HPC_LA26_P	23
ADC	AD9434_ORB/AD6641_SPSDFS	To FPGA	D27	FMC_HPC_LA26_N	23
ADC	AD9434_DCO/AD6641_FILLB	To FPGA	D20	FMC_HPC_LA17_CC_P	23
ADC	AD9434_DCOB/AD6641_FILL	To FPGA	D21	FMC_HPC_LA17_CC_N	23
TX	ADL5375_EN_25	From FPGA	C26	FMC_HPC_LA27_P	23
RX	ADL5365_EN_25	From FPGA	C27	FMC_HPC_LA27_N	23
CLK	NETWORK_CLKP	From FPGA	D23		23
CLK	NETWORK_CLKN	From FPGA	D24		23
CLK	NETWORK_CLKOUTP	To FPGA	SMA J7	FMC_LPC_GBTCLK0_P	MGT_115
CLK	NETWORK_CLKOUTN	To FPGA	SMA J8	FMC_LPC_GBTCLK0_N	MGT_115
DAC	AD9122_D15	From FPGA	F22	FMC_HPC_HB02_P	12
DAC	AD9122_D15N	From FPGA	F23	FMC_HPC_HB02_N	12
DAC	AD9122_D14	From FPGA	J24	FMC_HPC_HB01_P	12
DAC	AD9122_D14N	From FPGA	J25	FMC_HPC_HB01_N	12
DAC	AD9122_D13	From FPGA	E24	FMC_HPC_HB05_P	12
DAC	AD9122_D13N	From FPGA	E25	FMC_HPC_HB05_N	12
DAC	AD9122_D12	From FPGA	F25	FMC_HPC_HB04_P	12
DAC	AD9122_D12N	From FPGA	F26	FMC_HPC_HB04_N	12
DAC	AD9122_D11	From FPGA	J27	FMC_HPC_HB07_P	12
DAC	AD9122_D11N	From FPGA	J28	FMC_HPC_HB07_N	12
DAC	AD9122_D10	From FPGA	E27	FMC_HPC_HB09_P	12
DAC	AD9122_D10N	From FPGA	E28	FMC_HPC_HB09_N	12
DAC	AD9122_D9	From FPGA	F28	FMC_HPC_HB08_P	12
DAC	AD9122_D9N	From FPGA	F29	FMC_HPC_HB08_N	12
DAC	AD9122_D8	From FPGA	J30	FMC_HPC_HB11_P	12
DAC	AD9122_D8N	From FPGA	J31	FMC_HPC_HB11_N	12
DAC	AD9122_D7	From FPGA	E30	FMC_HPC_HB13_P	12
DAC	AD9122_D7N	From FPGA	E31	FMC_HPC_HB13_N	12
DAC	AD9122_D6	From FPGA	F31	FMC_HPC_HB12_P	12
DAC	AD9122_D6N	From FPGA	F32	FMC_HPC_HB12_N	12
DAC	AD9122_D5	From FPGA	K31	FMC_HPC_HB10_P	12
DAC	AD9122_D5N	From FPGA	K32	FMC_HPC_HB10_N	12
DAC	AD9122_D4	From FPGA	J33	FMC_HPC_HB15_P	12
DAC	AD9122_D4N	From FPGA	J34	FMC_HPC_HB15_N	12
DAC	AD9122_D3	From FPGA	E33	FMC_HPC_HB19_P	12
DAC	AD9122_D3N	From FPGA	E34	FMC_HPC_HB19_N	12
DAC	AD9122_D2	From FPGA	F34	FMC_HPC_HB16_P	12
DAC	AD9122_D2N	From FPGA	F35	FMC_HPC_HB16_N	12
DAC	AD9122_D1	From FPGA	K34	FMC_HPC_HB14_P	12
DAC	AD9122_D1N	From FPGA	K35	FMC_HPC_HB14_N	12
DAC	AD9122_D0	From FPGA	J36	FMC_HPC_HB18_P	12
DAC	AD9122_D0N	From FPGA	J37	FMC_HPC_HB18_N	12
DAC	AD9122_FRAME_P	From FPGA	E21	FMC_HPC_HB03_P	12
DAC	AD9122_FRAME_N	From FPGA	E22	FMC_HPC_HB03_N	12
DAC	AD9122_DCIP	From FPGA	K25	FMC_HPC_HB00_CC_P	12
DAC	AD9122_DCIN	From FPGA	K26	FMC_HPC_HB00_CC_N	12
CLK	Q1_P	To FPGA	K28	FMC_HPC_HB06_CC_P	12
CLK	Q1_N	To FPGA	K29	FMC_HPC_HB06_CC_N	12
CLK	Q2_P	To FPGA	K37	FMC_HPC_HB17_CC_P	12

Group	Name	Signal Direction	FMC-HPC Pin	ML605 FMC-HPC Signal	FPGA Bank
Clock	Q2_N	To FPGA	K38	FMC_HPC_HB17_CC_N	12
SPI	SCLK_MAIN	From FPGA	E18	FMC_HPC_IIC_SCL	14
SPI	SDIO_MAIN	From FPGA	E19	FMC_HPC_IIC_SDA	14
SPI	SDO_MAIN	To FPGA	K16	FMC_HPC_HA17_CC_P	14
SPI	AD5611CSB	From FPGA	K17	FMC_HPC_HA17_CC_N	14
SPI	AD9122CSB	From FPGA	J18	FMC_HPC_HA18_P	14
SPI	AD9434CSB	From FPGA	J19	FMC_HPC_HA18_N	14
SPI	AD9516CSB	From FPGA	K19	FMC_HPC_HA21_P	14
SPI	ADF4002_LO_CSB	From FPGA	K20	FMC_HPC_HA21_N	14
SPI	ADF4002_CLK_CSB	From FPGA	J21	FMC_HPC_HA22_P	14
SPI	ADF4150CSB	From FPGA	J22	FMC_HPC_HA22_N	14
SPI	ADF4350CSB	From FPGA	K22	FMC_HPC_HA22_P	14
SPI	PORTCSB	From FPGA	K23	FMC_HPC_HA22_N	14

DAC BUS

Baseband Tx data (DAC data) must be provided from the FPGA across the interface in the form of 1.8 V differential LVDS data pairs. The data format is 368.64 MSPS DDR, containing I and Q data pairs. The DAC can support other modes of data transfer, including byte and nibble modes; however, these are not the intended modes of operation.

In addition to data, the FPGA must also provide a 1.8 V differential LVDS data pair that indicates the data clock input (DCI). This clock is aligned with the data, and a high level indicates I data, while a low level indicates Q data. A timing diagram for the data and DCI signals is shown in Figure 56. Minimum setup and hold times are listed in Table 18. See the AD9122 data sheet for more detailed information.

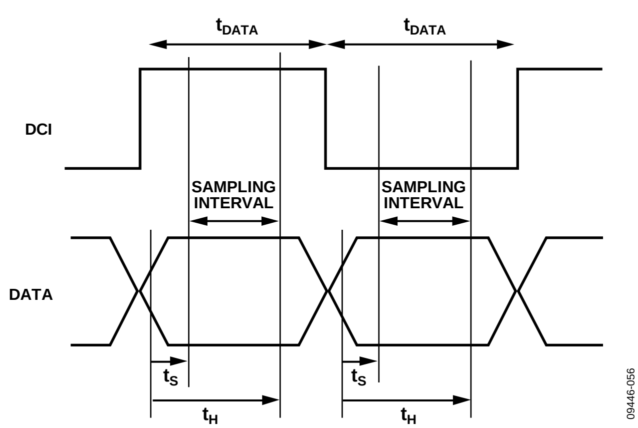


Figure 56. Tx Data Timing Diagram

Table 18. Tx Data Setup and Hold Time

Minimum Setup Time (t_S)	Minimum Hold Time (t_H)
−0.05 ns	+0.65 ns

ADC BUS

IF sampled observation receive data (ADC data) is provided to the FPGA interface in different formats depending on the ADC in use.

The AD9434 provides 12 differential LVDS data pairs to the FPGA at the converter sample rate in single data rate (SDR) format. For example, at a sample rate of 491.52 MHz, the AD9434 delivers data at 491.52 MSPS. This ADC also supports a double data rate (DDR) with a 6-bit high word and a 6-bit low word format; however, this is not the intended mode of operation.

The AD9434 provides an overrange bit pair (OR and ORB) that indicates when the input signal has exceeded the input range, and a data clock output pair (DCO and DCOB) that indicates when output data is valid.

A timing diagram is provided in Figure 57. DCO skew specifications are listed in Table 19. See the AD9434 data sheet for detailed information.

Table 19. Rx Data to DCO Skew

Data to DCO Skew (t_{SKEW})		
Min	**Typ**	**Max**
−0.3 ns	0.1 ns	0.5 ns

In contrast to the AD9434, the AD6641 ADC has several output options and an internal 16k deep FIFO. All the output modes for the AD6641 are at reduced rates relative to the sampling rate. The MSDPD evaluation platform uses a 12-bit parallel CMOS output mode that runs at ⅛ the sampling rate. For example, at a sample rate of 491.52 MHz, the AD6641 delivers data at 61.44 MSPS.

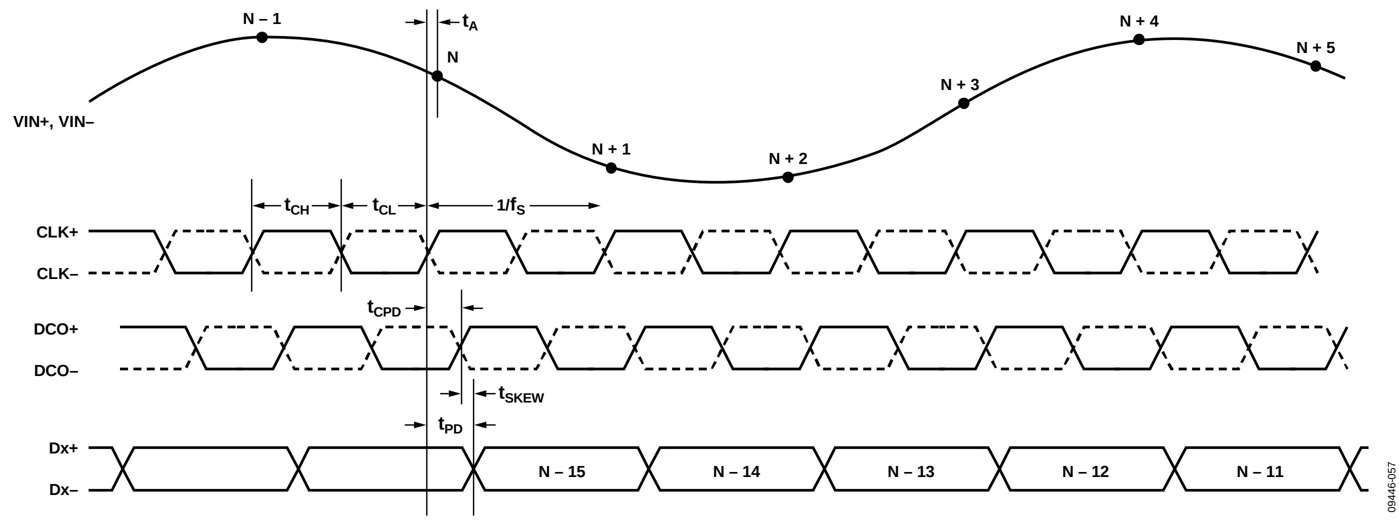


Figure 57. AD9434 Output Data Timing

The FIFO inside the AD6641 can be used in two ways, single capture or continuous capture. In single capture mode, the ADC waits for a signal from the controller to begin acquiring data and then asserts an indicator when the FIFO has filled. The controller then retrieves the data. In continuous capture mode, the FIFO is constantly being filled and updated. In this mode, the ADC waits for a signal from the controller to cease acquisition. This permits the controller to retrieve the data.

See the AD6641 data sheet for complete details on how to implement optional modes and interfaces.

SPI BRIDGE

The SPI bridge serves the purpose of allowing either the USB microcontroller or the FPGA to program and control the mixed signal resources on the MSDPD Dashboard. Only one can be selected at a time for the system. The bridge consists of solder jumpers and level translators.

The solder jumpers are responsible for shifting the PCB routing between the two sources, and the level translators are responsible for interfacing between different voltage domains.

The USB microcontroller is primarily a 5 V device, while the logic level of the FPGA outputs is currently 2.5 V. Note that the FPGA voltage levels are subject to change as the development platform evolves. A simplified version of the SPI bridge is shown in Figure 58.

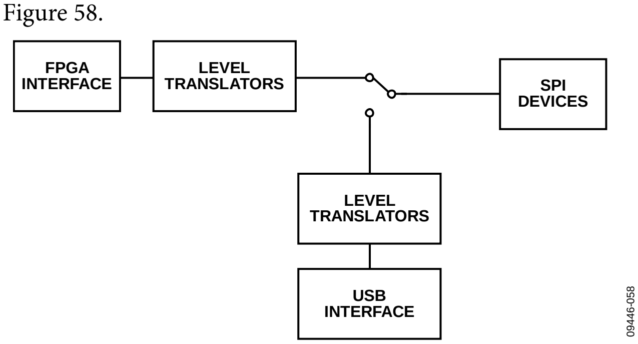


Figure 58. SPI Bridge Block Diagram

There are three SPI control voltage domains on the MSDPD Dashboard, 5 V, 3.3 V, and 1.8 V. Table 20 and Table 21 list the input control signals to the level translators (from the USB microcontroller and the FPGA) and the output control signals from the level translators with their respective voltage levels (to the SPI devices).

The voltage supplies for the level translators are all regulated down from the main 5.3 V board supply with the exception of the 2.5 V supply on the AD-MSDPDX-9434/AD-MSDPDX-6641 board. For this board, the 2.5 V is supplied over the FMC connector.

The ADL5375_EN and ADL5365_EN signals are always supplied by the FPGA host board. This is to allow for fast TDD control of the Tx modulator and the Rx mixer.

An MCP23S17, 16-bit, SPI controlled port expander is included on the MSDPD Dashboard to support more control I/Os. The port expander controls the 5-bit gain word for the AD8375 DVGA as well as the AD8375 enable signal. The port expander also controls the enable signals for the on-board 30.72 MHz reference, both ADF4002 PLLs, and the ADF4351 and ADF4350 PLLs. The mux outputs from these PLLs are routed to the port expander for optional readback. By default, the mux output reports back the PLL lock detector.

Table 20. Control Signal Level Translation for USB Microcontroller Board Control

Microcontroller Control Signals			
Microcontroller (5 V)	**5 V**	**3.3 V**	**1.8 V**
INTERNAL_MOSI	5V_SDIO	3.3V_SDIO	1.8V_SDIO
INTERNAL_MISO	5V_SDO	3.3V_SDO	1.8V_SDO
INTERNAL_SCLK	5V_SCLK	3.3V_SCLK	1.8V_SCLK
CSB0		3.3V_9516CSB	
CSB1		3.3V_4150CSB	
CSB2		3.3V_4350CSB	
CSB3			1.8V_9122CSB
CSB4			1.8V_9434CSB
CSB5		3.3V_5611CSB	
CSB6		ADF4002_CSB1	
CSB7		ADF4002_CSB2	
CSB8	5V_PORTEX_CSB		

Table 21. Control Signal Level Translation for FPGA Board Control

FPGA Control Signals			
HSMC/FMC (2.5 V)	**5 V**	**3.3 V**	**1.8 V**
SCLK_MAIN	5V_SDIO	3.3V_SDIO	1.8V_SDIO
SDIO_MAIN	5V_SDO	3.3V_SDO	1.8V_SDO
SDO_MAIN	5V_SCLK	3.3V_SCLK	1.8V_SCLK
AD9122CSB			1.8V_9122CSB
AD9434CSB			1.8V_9434CSB
ADF4002_CLK_CSB		ADF4002_CSB1	
ADF4002_LO_CSB		ADF4002_CSB2	
AD9516CSB		3.3V_9516CSB	
ADF4150CSB		3.3V_4150CSB	
ADF4350CSB		3.3V_4350CSB	
PortCSB	5V_PortEx_CSB		
AD5611CSB		3.3V_5611CSB	
ADL5375_EN_25		ADL5375_EN	
ADL5365_EN_25		ADL5365_EN	

DETAILED SOFTWARE DESCRIPTION

Virtually all of the integrated circuits used on the MSDPD evaluation platform are programmable. Individual devices typically offer a serial peripheral interface (SPI) bus to access internal registers. High level access to these control buses can come over the USB port to an on-board USB microcontroller or access can come directly from an FPGA.

When using the USB microcontroller for control, the MSDPD evaluation platform includes two accessory software interfaces. The primary interface is a simplified GUI called the MSDPD Dashboard that provides programmability based upon familiar system parameters, such as frequency and gain.

This GUI takes high level input from the user and computes the required low level register values. The user is prevented from having to solve equations to determine register values. In addition, this GUI simplifies control of analog functions, such as those related to LO feedthrough rejection and image rejection.

The secondary interface is the SPIController, which contains a more complete interface to the low level register maps of each device on the board. This interface sits below or behind the MSDPD Dashboard. It is required for the MSDPD Dashboard to work; although, its use is strictly optional. The SPIController window, when it appears, can simply be minimized. Users may want to use it to adjust low level settings to optimize performance for their particular application.

SPI DEVICE MAPPING

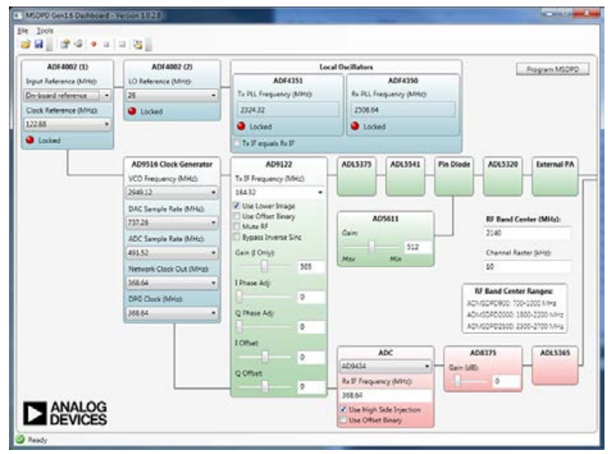
Each device on the MSDPD evaluation platform is given an address offset to distinguish the base addresses of its registers from those of another device. In this way, each device may be addressed according to the published data sheet register addresses, plus the appropriate offset. For example, the address offset for the AD9122 is 0x800. Therefore, to access an AD9122 register located at Address 0x001 of the data sheet, issue a value of 0x801. Device register addresses beyond 0x0FF are treated in the same way. For example, to access Address 0x230 on the AD9516, use an address of 0x730 (0x500 + 0x230). Table 22 lists addressable devices and their corresponding base address.

Table 22. SPI Address Offsets

Device	Base Address
MCP23S17 Port Expander (Controls AD8375, PLL enable, PLL readback)	0x000
ADF4350	0x100
ADF4351	0x200
ADF4002 (1) Clock Clean-Up	0x300
ADF4002 (2) LO Reference	0x400
AD9516	0x500
AD9122	0x800
AD9434/AD6641	0x900
AD5611	0xB00

MSDPD GEN1.6 DASHBOARD

A screenshot of the **MSDPD Gen1.6 Dashboard** software is shown in Figure 59.



09446-059

*Figure 59. **MSDPD Gen1.6 Dashboard***

The **MSDPD Gen1.6 Dashboard** software is organized in signal chain groups. The clock generation and distribution devices are represented in blocks of blue. The transmit path is in green blocks, and the observation receive path is in red blocks. For many of the blocks, the most useful controls are displayed.

Some blocks contain frequency values that are based on information in other blocks. When a user updates information in a block, dependent values in other blocks automatically update. In many cases, the user must then click **Program MSDPD** to communicate these updated values to the board.

There are three AD-MSDPD-9434/AD-MSDPD-6641 board model numbers based on the RF range. Table 23 lists the board models, the usable RF frequency range, and recommended selections for transmit and receive operation.

Table 23. MSDPD Recommended Defaults

Board Model	RF Band Range (MHz)	Use Lower Image(Tx)	Use High Side Injection(Rx)
1	700 to 1000	Yes	Yes
2	1800 to 2200	Yes	No
3	2300 to 2700	Yes	Yes

ADF4002 (1) Controls

The ADF4002 (1) controls include drop-down menus for the **Input Reference (MHz)** and **Clock Reference (MHz)**, as shown in Figure 60. The input reference frequency can be supplied externally at one of the rates listed in the drop-down menu or the on-board 30.72 MHz crystal reference can be chosen. Choosing one of the external frequency rates disables the on-board crystal.

The clock reference is chosen to indicate which VCXO is installed on the board. By default, the MSDPD Dashboard uses the 122.88 MHz VCXO. There is also a PLL lock indicator for the ADF4002 (1).

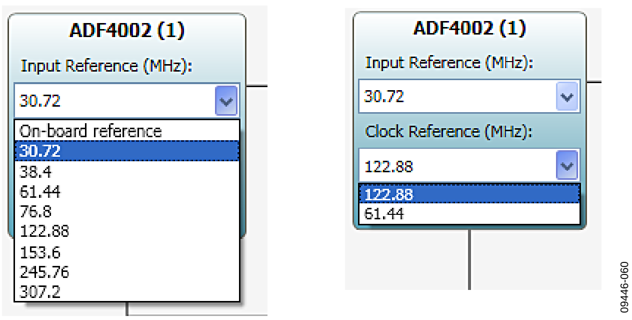


Figure 60. ADF4002 Controls

ADF4002 (2) Control

The ADF4002 (2) control, shown in Figure 61, includes a drop-down menu for the **LO Reference (MHz)**. This is chosen to indicate which VCXO is installed on the board. By default, the MSDPD Dashboard uses the 26 MHz VCXO. There is also a PLL lock indicator for the ADF4002 (2).

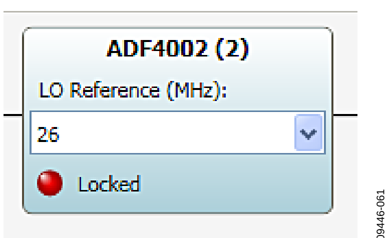


Figure 61. ADF4002 (2) Control

AD9516 Clock Generator Controls

The AD9516 control block allows the user to select a VCO frequency and then choose converter sample rates and network clock rates accordingly. The MSDPD Dashboard permits selection of only one VCO frequency, 2949.12 MHz. All DAC, ADC, DPG, and network clocks must be divisible from this master frequency by 2^n.

The **Network Clock Out (MHz)** and the **DPG Clock (MHz)** are linked and always equal the same frequency. The network clock out is available on SMA connectors, J7/J8, and is used by the Xilinx development platform. The DPG clock (Q1_P/Q1_N and Q2_P/Q2_N) is passed over the HSMC connector and used by the Altera development platform. The AD9516 block is shown in Figure 62.

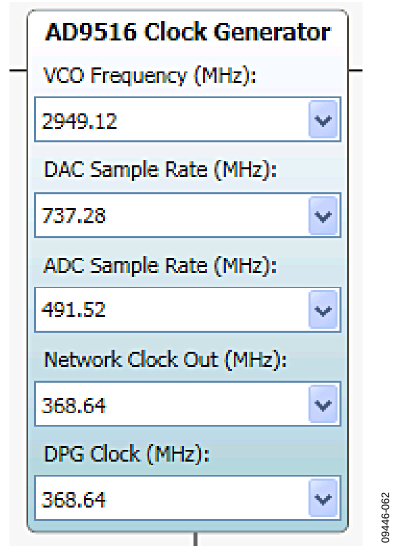


Figure 62. AD9516 Clock Generator Controls

Local Oscillators Controls

The ADF4351/ADF4350 PLL frequencies are indicated in the **Local Oscillators** block, as shown in Figure 63.The PLL frequencies are calculated based upon several variables, including user input of RF band center, IF for both Tx and Rx, Tx lower image selection, and Rx high side injection selection:

- When lower image = 1, TX_PLL = RF + TX_IF.
- When lower image = 0, TX_PLL = RF − TX_IF.
- When high side injection = 1, RX_PLL = RF + RX_IF.
- When high side injection = 0, RX_PLL = RF − RX_IF.

It is important to choose the RF band center frequencies that lie within the operating frequency range of the board model.

The only user control in the **Local Oscillators** block is the **Tx IF equals Rx IF** check box. When this is selected, the ADF4350 box will be grayed out as well as the **Rx IF Frequency (MHz)** control in the **ADC** control block. Typically, IF frequencies for the transmit and receive paths are different, and this option will be unchecked (also LO Switch Jumper P6 will be set to LO1). To use this option, check the box, set Jumper P6 to LO2, and populate L4 (near T7 on the back side of the PCB).

There are PLL lock indicators for the ADF4351 and ADF4350.

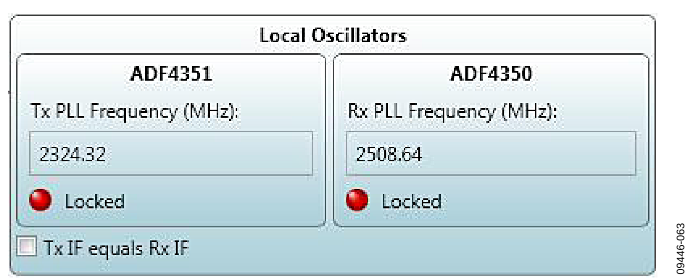


*Figure 63. **Local Oscillators** Controls*

AD9122 Controls

The AD9122 control block allows the user to enter the desired **Tx IF Frequency (MHz)** and chose either the lower or upper sideband image. Other controls include the input data format (offset binary or twos complement), muting of the Tx RF output, and inverse sinc roll-off compensation. Gain, phase, and offset control for enhanced LO nulling and image rejection are also included. The AD9122 control block is shown in Figure 64.

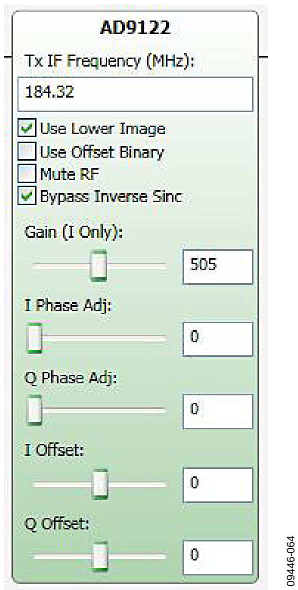


Figure 64. AD9122 Controls

AD5611 Control

The AD5611 sets the analog gain of the transmit path by controlling the analog voltage at the pin diode input. The AD5611 is a 10-bit nanoDAC where the minimum code of 0 results in the maximum gain and the maximum code of 1023 results in the minimum gain through the Tx path. The AD5611 control block is shown in Figure 65.

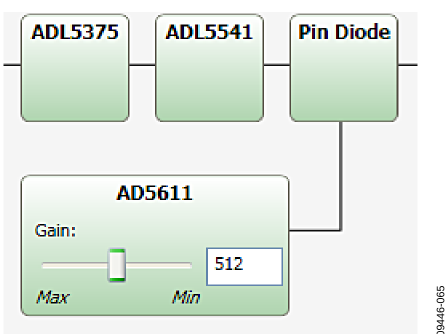


Figure 65. AD5611 Control

RF Band Center Control

The **RF Band Center (MHz)** is the user controlled input shown in Figure 66. The adjustment of the RF band center directly affects the Tx and Rx PLL frequencies. It is important to choose RF frequencies that lie within the operating range of the board model. Furthermore, the RF band center frequency is dependent on the channel raster frequency and the divide ratios available for the Tx LO.

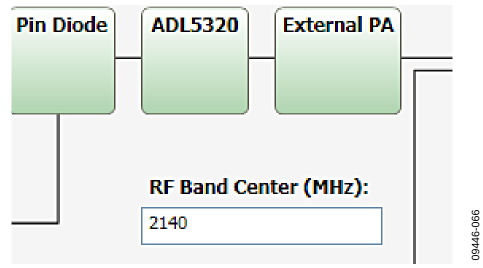


Figure 66. RF Band Center Control

Channel Raster Control

The **Channel Raster (kHz)**, or frequency step size, is the user controlled input shown in Figure 67. The adjustment of the channel raster affects the divide ratios chosen for the ADF4351 and ADF4350 PLLs. This affects the output frequency of the PLL and therefore affects the RF band center and ADC IF frequencies.

The RF and Rx IF frequencies may need to change slightly to meet a specific channel raster frequency.

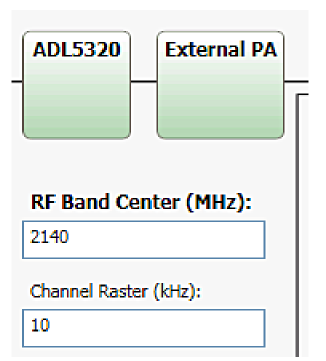


Figure 67. Channel Raster Control

AD8375 Control

The AD8375 sets the analog gain of the observation receive path. The gain control is in 1 dB steps from −4 dB to +20 dB. The AD8375 control block is shown in Figure 68.

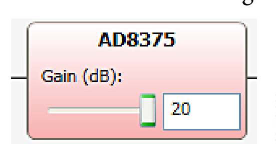


Figure 68. AD8375 Control

ADC Controls

The ADC control block allows users to specify which ADC is populated on the MSDPD Dashboard (typically the AD6641 for inside of China and the AD9434 for outside of China). The user can also specify the **Rx IF Frequency (MHz)**, assuming it differs from the Tx IF frequency controlled by the **Local Oscillators** block. In addition, users can select whether they want to use high side or low side injection on the receiver. The default is dependent on the board model. Users can also set the output data format from the ADC to be either offset binary or twos complement. The **ADC** control block is shown in Figure 69.

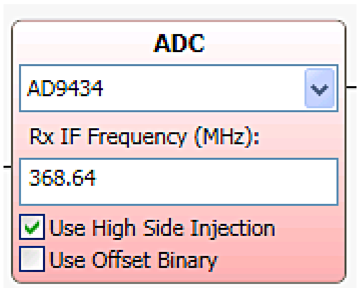


Figure 69. ***ADC*** *Controls*

SPICONTROLLER

If further programmability is needed beyond what is provided on the MSDPD Dashboard, a second software interface, the SPIController, can be used to access all the individual register settings for all the SPI programmable devices on the board. SPIController is always opened when MSDPD Dashboard is launched. This is because the MSDPD Dashboard is a wrapper to SPIController. The SPIController window can be minimized, if desired.

All register writes that occur in the MSDPD Dashboard are reflected and updated in the SPIController. However, individual writes made in the SPIController are not updated in the MSDPD Dashboard window. Furthermore, any register writes from the SPIController risk being overwritten the next time the MSDPD Dashboard programs the board.

A screenshot of the SPIController program is shown in Figure 70. Note that there are individual tabs for all programmable devices on the MSDPD Dashboard (AD9122 and AD5611 share the first tab). For complete register descriptions for each programmable device on the MSDPD Dashboard, refer to the individual product data sheets.

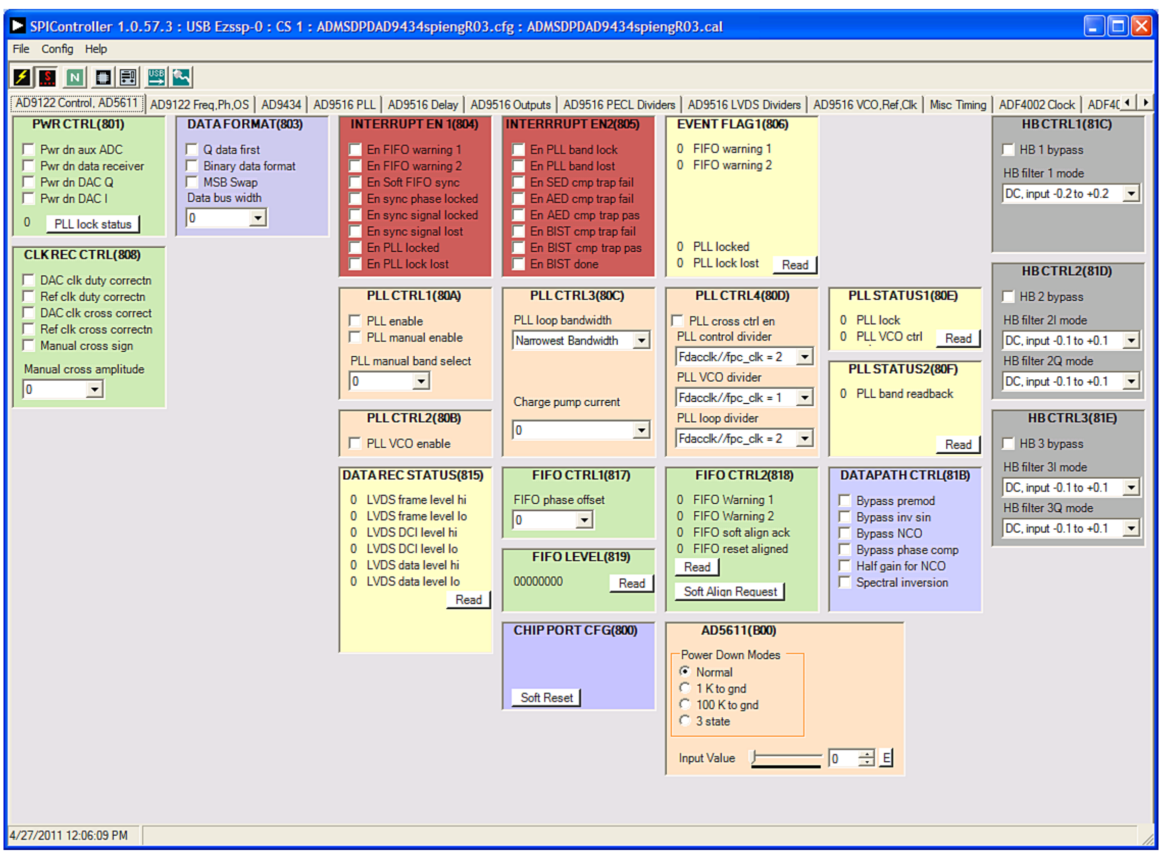


Figure 70. SPIController Software Interface for the MSDPD Evaluation Platform

APPENDIX A—SOFTWARE AUTOMATION

Analog Devices has released a component object model (COM) DLL to interface to the MSDPD Dashboard application. This enables users to control the MSDPD Dashboard through a standardized interface from any application layer that supports COM (for example, MATLAB, Visual Basic 6.0, and LabVIEW).

OVERVIEW

The MSDPD Dashboard exposes a subset of the visible controls on the dashboard through the COM shown in Figure 71 (see the highlighted in red boxes).

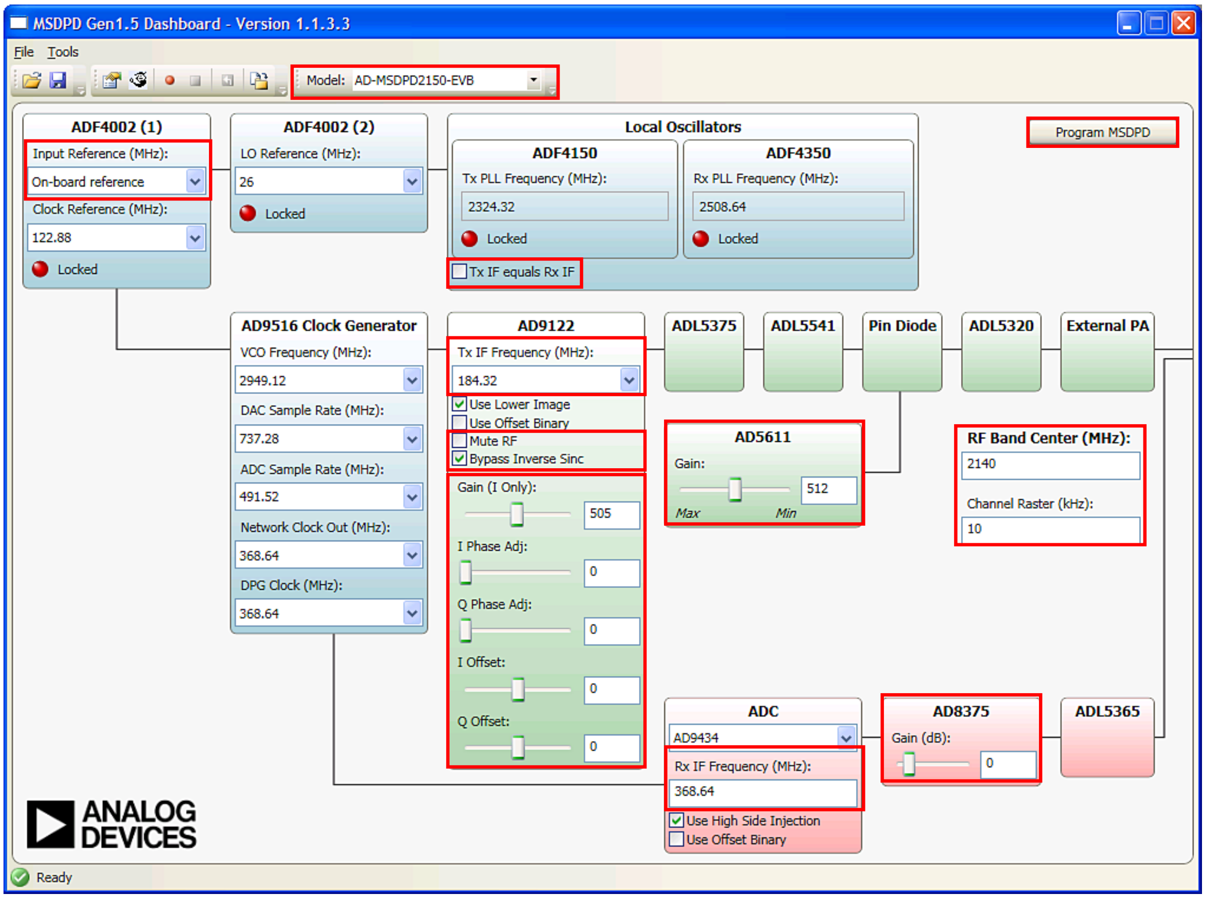


Figure 71. MSDPD Dashboard Controls Available for Automation Through COM

Table 24 shows the exposed properties and methods with their descriptions.

Table 24. COM Properties

Property	Description
BoardModel	Sets/gets the MSDPD board model
RFBandCenter[1]	Sets/gets the RF band center (in MHz)
ChannelRaster[1]	Sets/gets the channel raster frequency (in kHz)
TxEqualsRx[1]	Sets/gets the Tx IF equals Rx IF switch state
ADF4002_1.InputReference[1]	Sets/gets the ADF4002 (1) input reference frequency (MHz)
ADF4002_1.UseOnBoardReference[1]	Sets/gets whether to use the on-board reference
AD9122.TxIFFrequency[1]	Sets/gets the AD9122 Tx IF frequency (in MHz)
AD9122.Gain	Sets/gets the AD9122 gain
AD9122.IPhase	Sets/gets the AD9122 I phase
AD9122.QPhase	Sets/gets the AD9122 Q phase
AD9122.IOffset	Sets/gets the AD9122 I offset
AD9122.QOffset	Sets/gets the AD9122 Q offset
AD9122.BypassInvSinc[1]	Sets/gets the AD9122 bypass inverse sinc switch state
AD9122.MuteRF	Sets/gets the AD9122 mute RF switch state
AD5611.Gain	Sets/gets the AD5611 gain
AD9434.RxIFFrequency[1]	Sets/gets the AD9434 Rx IF frequency (in MHz)
AD8375.Gain	Sets/gets the AD8375 gain

[1] These properties require a subsequent call to the program method to update the board.

Table 25. COM Methods

Method	Description
Open()	Opens the MSDPD Dashboard
Program()	Programs the current MSDPD Dashboard settings to the MSDPD board
Close()	Closes the MSDPD Dashboard

The MSDPD Dashboard user interface is updated in real-time as property values are set.

The COM object is registered with the Windows Registry so that it is accessible regardless of where the application is running. The following are some properties of the COM object that may be required in the implementation:

- GUID: 705EE820-5B67-4B4D-A15A-2A3751CAB101
- Product ID: MSDPDDashboard1p5.COM.Dashboard

RELATED FILES

The COM assembly and dependencies are installed into the MSDPD Dashboard application directory, including the following:

- MSDPDDashboard.Com.dll
- MSDPDDashboard.dll (dependency)
- AnalogDevices.Common.dll (dependency)
- ADI.Scripting.dll (dependency)

In addition, included are samples that use the MSDPD Dashboard COM object to provide further help. Samples for the following languages are located in the **Samples** subfolder in the MSDPD application directory (**C:\Program Files\Analog Devices\MSDPD Dashboard\Samples**):

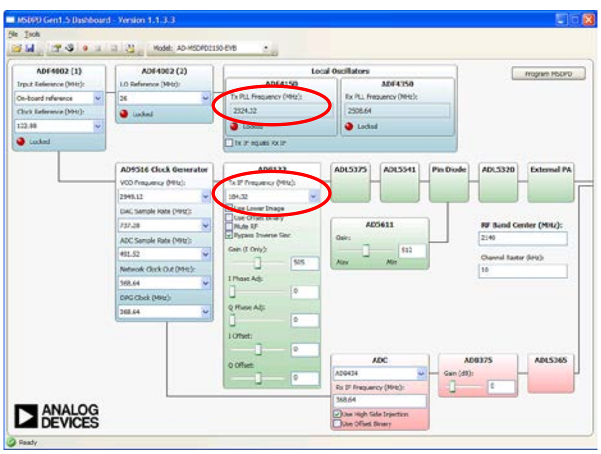
- Visual Basic 6.0
- MATLAB

APPENDIX B—Tx LO AND IMAGE SUPRESSION CALIBRATION ROUTINE

Quadrature modulators can introduce unwanted signals at the LO frequency due to dc offset voltages in the I and Q baseband inputs as well as feedthrough paths from the LO input to the output. The LO feedthrough can be nulled by applying the correct dc offset voltages at the DAC output. This can be done by using the digital dc offset adjustment features included in the AD9122 DAC. Good sideband suppression requires both gain and phase matching of the I and Q signals. The phase adjust and the gain control features included in the AD9122 DAC can be used to calibrate I and Q transmit paths to optimize the sideband suppression.

At factory test, a one-time factory calibration was completed to optimize the LO feedthrough and image rejection for a single frequency. The gain, phase and offset correction coefficients from this factory calibration are located on the backside of the board. For additional tuning of the LO feedthrough and/or image rejection, the following procedure can be followed:

1. Connect the Tx output to a spectrum analyzer (SA) to monitor the single sideband spectrum. Set the center frequency on the spectrum analyzer to the Tx PLL frequency. Set the span to >2 × Tx IF frequency. See Figure 72.



09446-072

Figure 72. Controls Used to Choose SA Settings and Correct for Image + LO

2. Configure the FPGA + MSDPD Dashboard to output a single-tone or multitone signal. On the spectrum analyzer, a single sideband spectrum should be visible: Desired sideband (strongest signal), undesired LO leakage, and undesired sideband.
3. Calibrate the undesired sideband first:
   a. Start with Gain (I Only) = 505, **I Phase Adj** = 0, and **Q Phase Adj** = 0.
   b. Find optimal **I Phase Adj** setting:
      i. Increase from 0, if image grows, stop and follow the next step. If image shrinks, continue increasing **I Phase Adj** until the image begins to grow again. Do not move beyond Code 511 because this control is twos complement encoded. Record the optimal **I Phase Adj** value.
      ii. Decrease **I Phase Adj** starting from 1023 until the image begins to grow again. Do not move beyond 512 because this control is twos complement encoded. Record the optimal **I Phase Adj** value.
   c. Find optimal **Q Phase Adj** setting:
      i. If the optimal **I Phase Adj** value was not 511 or 512, the optimal **Q Phase Adj** value is 0.
      ii. If the optimal **I Phase Adj** value was 511, increase **Q Phase Adj** from 0 until the image begins to grow again. Do not move beyond Code 511 because this control is twos complement encoded. Record the optimal **Q Phase Adj** value.
      iii. If the optimal **I Phase Adj** value was 512, decrease **Q Phase Adj** starting from 1023 until the image begins to grow again. Do not move beyond 512 because this control is twos complement encoded. Record the optimal **Q Phase Adj** value.
   d. Find the optimal **Gain** setting:
      i. Increase **Gain** from 505, if image grows, stop and follow the next step. If image shrinks, continue increasing **Gain** until the image begins to grow again. Record the optimal **Gain** value.
      ii. Decrease **Gain** from 505; continue until the image begins to grow again. Record the optimal **Gain** value.
   e. Ensure that the optimal **Gain**, **I Phase Adj**, and **Q Phase Adj** values are entered into the corresponding fields on MSDPD Dashboard.

4. Calibrate the undesired LO leakage:
   a. Start with **I Offset** = 0 and **Q Offset** = 0.
   b. Find the optimal **I Offset** settings:
      i. Increase **I Offset** from 0, if LO grows, stop and follow the next step. If LO shrinks, continue increasing **I Offset** until the LO begins to grow again. Record the optimal **I Offset** value.
      ii. Decrease **I Offset** from 0; continue until the image begins to grow again. Record the optimal **I Offset** value.
   c. Find the optimal **Q Offset** settings:
      i. Increase **Q Offset** from 0, if LO grows, stop and follow the next step. If LO shrinks, continue increasing **Q Offset** until the LO begins to grow again. Record the optimal **Q Offset** value.
      ii. Decrease **Q Offset** from 0; continue until the image begins to grow again. Record the optimal **Q Offset** value.
   d. Ensure that the optimal **I Offset** and **Q Offset** values are entered into the corresponding fields on MSDPD Dashboard.

This concludes the calibration procedure for nulling out the unwanted LO feedthrough and image. For additional information, refer to Application Note AN-1039, *Correcting Imperfections in IQ Modulators to Improve RF Signal Fidelity*.

APPENDIX C—DEBUG GUIDE

LOW Rx POWER

Ensure that the position of the LO switch jumper, P6, is set correctly (see Figure 47). Set the jumper to LO1 to use the ADF4350.

HIGH NOISE FLOOR AT Tx OUTPUT

Check the state of the data format bit in the **AD9122** control block on the MSDPD Dashboard. If the **Use Offset Binary** box is checked, the digital input data is in unsigned binary data format, where:

- 0x0000 is negative full scale.
- 0x8000 is midscale.
- 0xFFFF is positive full scale.

If the **Use Offset Binary** box is not checked, the digital input data is in twos complement data format where:

- 0x8000 is negative full scale.
- 0x0000 is midscale.
- 0x7FFF is positive full scale.

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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UG09446-0-8/12(0)

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