

Evaluating the **AD5693R** Single-Channel, 16-Bit, Serial, Voltage Output DAC

FEATURES

Full featured evaluation board for the **AD5693R**
 On-board reference
 Various link options
 PC control in conjunction with the Analog Devices, Inc., **SDP**
 PC software for control of DACs
 On-board ADC for voltage readback

EVALUATION KIT CONTENTS

EVAL-AD5693RSDZ evaluation board
AD5693R device

HARDWARE REQUIRED

EVAL-SDP-CB1Z (SDP-B) board or **EVAL-SDP-CS1Z (SDP-S)**
 board, must be ordered separately

SOFTWARE REQUIRED

ACE evaluation software, available for download from the
EVAL-AD5693RSDZ product page

GENERAL DESCRIPTION

This user guide details the operation of the **EVAL-AD5693RSDZ** evaluation board for the **AD5693R** single-channel, serial, voltage output, digital-to-analog converter (DAC).

The **EVAL-AD5693RSDZ** is designed to help customers quickly prototype **AD5693R** circuits and reduce design time. The **AD5693R** operates from a single 2.7 V to 5.5 V supply. The **AD5693R** incorporates an internal 2.5 V on-board reference to give an output voltage span of 2.5 V or 5 V.

The **EVAL-AD5693RSDZ** evaluation board interfaces to the USB port via the **SDP** board. The analysis control evaluation (**ACE**) software is available for download from the **EVAL-AD5693RSDZ** product page to use with the evaluation board to allow the user to program the **AD5693R**. The **EVAL-AD5693RSDZ** evaluation board requires the purchase of the **EVAL-SDP-CB1Z (SDP-B)** board or the **EVAL-SDP-CS1Z (SDP-S)** board.

For full details, consult the **AD5693R** data sheet, which must be used in conjunction with this user guide when using the evaluation board.

EVAL-AD5693RSDZ EVALUATION BOARD CONNECTED TO THE **SDP-S** BOARD

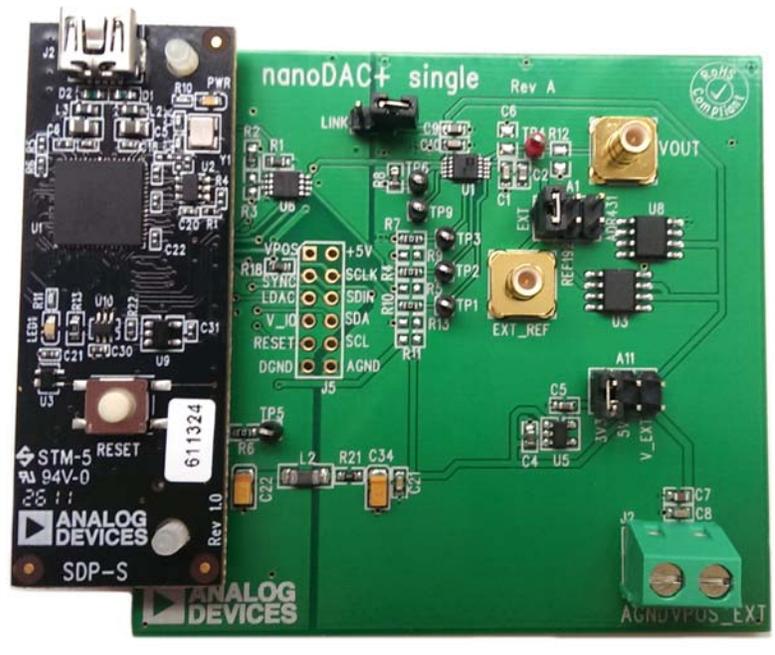


Figure 1.

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REVISION HISTORY

7/2017—Rev. 0 to Rev. A

Reorganized Layout..... Universal
 Deleted Additional Equipment Needed Section 1
 Added Hardware Required Section and Software Required Section..... 1
 Changes to Title, Evaluation Kit Contents Section, General Description Section, EVAL-AD5693RSDZ Evaluation Board Connected to the SDP-S Board Section, and Figure 1 Caption . 1
 Deleted Getting Started Section 3
 Added Evaluation Board Quick Start Procedures Section, Initial Setup Section, and Figure 2; Renumbered Sequentially .. 3
 Changes to Installing the Software Section..... 3
 Added Figure 3..... 4
 Deleted How to Use the Software Section, Running the Software Section, Figure 2, and Figure 3, and Figure 4; Renumbered Sequentially 5

Added Block Diagram and Description Section, Figure 4, Table 1; Renumbered Sequentially5
 Deleted Software Operation Section and Figure 5.....6
 Added Memory Map Section, Figure 5, and Figure 66
 Moved Evaluation Board Hardware Section.....7
 Changes to Power Supplies Section, Table 2, Link Options Section, and Table 4.....7
 Changes to Figure 7 Caption.....8
 Changes to Figure 8 Caption.....9
 Changes to Figure 9 Caption, Figure 10 Caption, and Figure 11 Caption 10
 Deleted Components List Section..... 11
 Added Bill of Materials Section 11
 Changes to Table 5..... 11

3/2014—Revision 0: Initial Version

EVALUATION BOARD QUICK START PROCEDURES

INSTALLING THE SOFTWARE

The [EVAL-AD5693RSDZ](#) evaluation board uses the [ACE](#) software, a desktop software application that allows the evaluation and control of multiple evaluation systems.

The [ACE](#) installer installs necessary SDP drivers and the Microsoft® .NET Framework 4 by default. The [ACE](#) software is available for download from the [EVAL-AD5693RSDZ](#) product page and must be installed before connecting the SDP board to the USB port of the PC, to ensure that the SDP board is recognized when it connects to the PC. For full instructions on how to install and use this software, see the [ACE](#) software page on the Analog Devices website.

After the installation is finished, the [EVAL-AD5693RSDZ](#) evaluation board plug in appears when the [ACE](#) software is opened.

INITIAL SETUP

To set up the evaluation board, take the following steps:

1. Connect the evaluation board to the SDP board, and then connect a USB cable between the SDP board and the PC.
2. Run the [ACE](#) application. The [EVAL-AD5693RSDZ](#) board plug ins appear in the attached hardware section of the **Start** tab.
3. Double click the board plug in to open the board view, shown in Figure 2.
4. Double click the **AD5693R** chip to access the chip block diagram. This view provides a basic representation of functionality of the board. The main function blocks of the board are labeled in Figure 3.

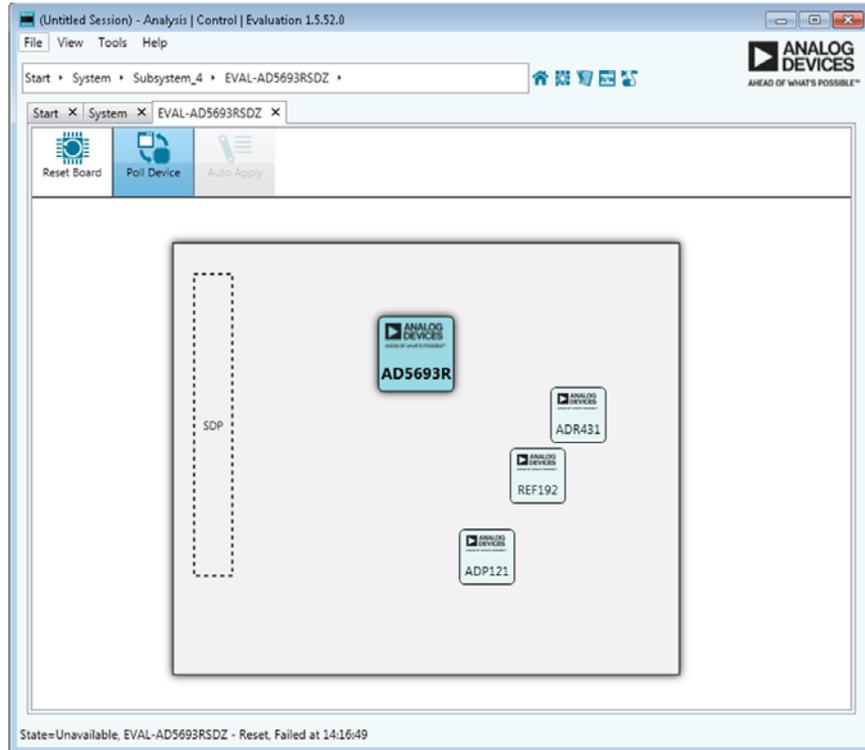
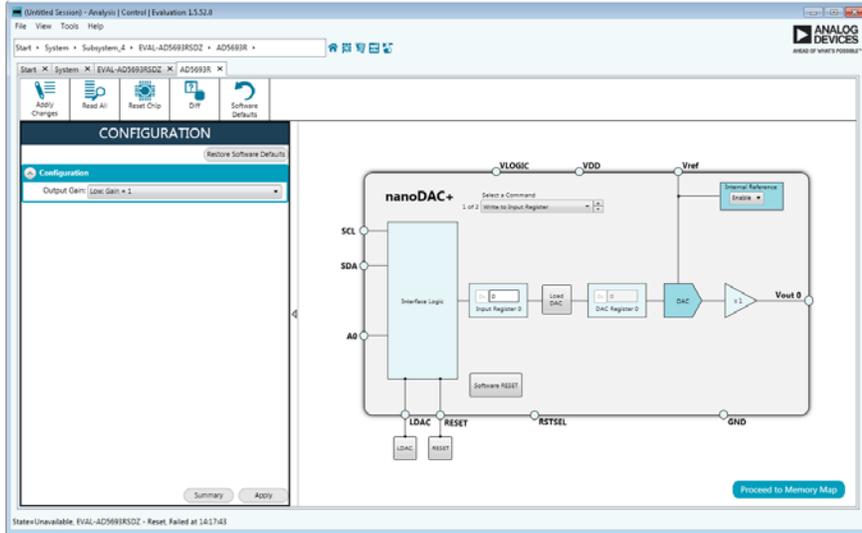


Figure 2. Board View of the [EVAL-AD5693RSDZ](#)



12145-103

Figure 3. Chip Block Diagram View of the AD5693R

BLOCK DIAGRAM AND DESCRIPTION

The [EVAL-AD5693RSDZ](#) software is organized to appear similar to the functional block diagram shown in the [AD5693R](#) data sheet. Therefore, correlating the functions on the [EVAL-AD5693RSDZ](#) evaluation board with the description in the [AD5693R](#) data sheet is simplified.

For a full description of each block, register, and its settings, see the [AD5693R](#) data sheet.

Some of the blocks and their functions are described in this section as they pertain to the evaluation board. The block diagram is shown in Figure 4. Table 1 describes the functionality of each block.

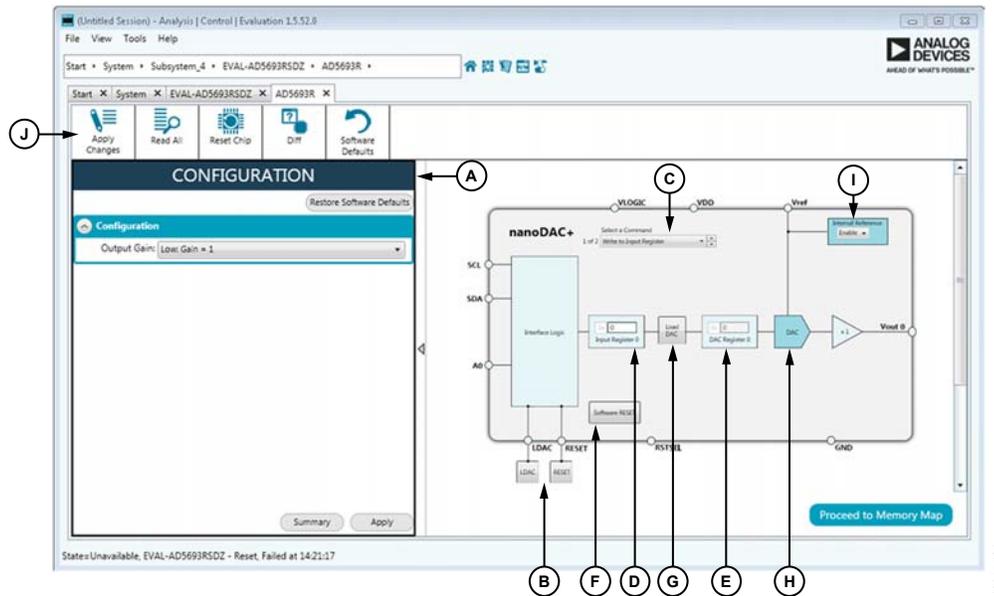


Figure 4. [AD5693R](#) Block Diagram with Labels

Table 1. Block Diagram Functions (See Labels in Figure 4)

Label	Button/Function Name	Description
A	CONFIGURATION Wizard	Used to set the initial configuration for the board. Select the reference gain case from the Output Gain dropdown menu. A gain of 1 is the default. After setting up the initial configuration, click Apply to apply the values. These settings can be modified at any stage while evaluating the board.
B	LDAC and RESET (GPIO buttons)	Act as external GPIO pulses to the LDAC and RESET pins. The LDAC button transfers data from the input register (D) to the DAC register (E). The RESET button clears all data from the input register and the DAC register. These buttons are live; therefore, there is no need to click Apply Changes (J).
C	Select a Command	Command option dropdown menu selects how the data being transferred to the device affects the input and DAC registers. After a data value is entered in the input register (D), this menu determines the internal DAC registers affected by updating the input register (D). After a new value is written in the input register (D), the data can be transferred to the DAC input register, or to the DAC register simultaneously. If the data is transferred to both registers, the channel DAC register (E) reflects the new value.
D	Input register	16-bit data word to be transferred to the device. Click Apply Changes (J) to transfer this 16-bit data word to the device.
E	DAC register	Displays the value that is currently present in the DAC register on the device. Update the DAC register by selecting the appropriate command option or by toggling LDAC (B).
F	Software RESET	Returns the evaluation board and software to default values. This button is live; therefore, there is no need to click Apply Changes (J).
G	Load DAC	Users can individually control which channel loads the values from the input register to the DAC register. Note that the AD5693R is a single-channel DAC and only offers one channel option for the Load DAC function.
H	DAC	DAC configuration options provide access to individual channel configuration options such as power-down options and hardware LDAC mask enable/disable settings.
I	Internal Reference	Select Enable from this setting to enable the on-chip reference for the evaluation board. If Disable is selected, an external reference must be applied. This control is only available on the AD5693R .
J	Apply Changes	Applies all modified values to the device. Note that if an evaluation board is not connected, values entered into the input register are not transferred to the DAC register.

MEMORY MAP

All registers are fully accessible from the **AD5693R Memory Map** tab, shown in Figure 5. To navigate to this tab, click the **Proceed to Memory Map** button, shown in Figure 4. This tab allows registers to be edited at the bit level. The bits shaded in dark gray are read-only bits and cannot be accessed from the **ACE** software. All other bits are toggled.

Clicking the **Apply Changes** button transfers data to the device. All changes made in the memory map tab correspond to the block diagram. For example, if the internal register bit is enabled, it displays as enabled on the block diagram. Any bits or registers that are in bold in the memory map tab are modified values that have not been transferred to the evaluation board (see Figure 6). Click **Apply Changes** to transfer the data to the evaluation board.



Figure 5. **AD5693R Memory Map Tab**

Address (Hex)	Name	Data (Hex)	Data (Binary)
0010	DAC0_Input	1234	0 0 0 1
0020	DAC0_Software_LDAC	0000	0 0 0 0
0040	Control	0000	0 0 0 0
0060	Software_Reset	0000	0 0 0 0

Figure 6. **AD5693R Memory Map with Unapplied Changes in the DAC0_Input Register**

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The [AD5693R](#) evaluation board can be powered through the SDP board or externally by the VPOS_EXT and AGND connectors.

Both AGND and DGND inputs are provided on the board. The AGND and DGND planes are connected at one location close to the [AD5693R](#). To avoid ground loop problems, it is recommended not to connect AGND and DGND elsewhere in the system.

All supplies are decoupled to ground with 10 μ F tantalum and 0.1 μ F ceramic capacitors.

Table 2. Power Supply Connectors

Connector No.	Voltage
J2, Pin 1	Analog positive power supply, V_EXT
J2, Pin 2	AGND

Table 4. Link Functions

Link No.	Options
A1	This link selects the DAC digital voltage source. Position A selects an external reference source via the SMB input, EXT_REF. Position B selects the REF192 external reference. Position C selects the ADR431 external reference.
LINK	Connect only if the EVAL-AD5693RSDZ board of the AD5693R is controlled through the PMOD connector and the SDP board is not connected.
A11	This link selects the DAC analog voltage source. Position A VPOS is powered at 3.3 V. Position B VPOS is powered from an unregulated USB supply. Position C VPOS is powered from an external supply voltage (V_EXT).

LINK OPTIONS

Various link and switch options are incorporated on the [EVAL-AD5693RSDZ](#) evaluation board and must be set for the required operating conditions before using the board. The functions of these link options are described in detail in Table 4.

Table 3 describes the positions of the different links controlled by the PC via the USB port. An SDP board operating in single-supply mode is required.

Table 3. Link Options Setup for SDP Control (Default)

Link No.	Options
A11	A
LINK	Disconnected
A1	A

EVALUATION BOARD SCHEMATICS AND ARTWORK

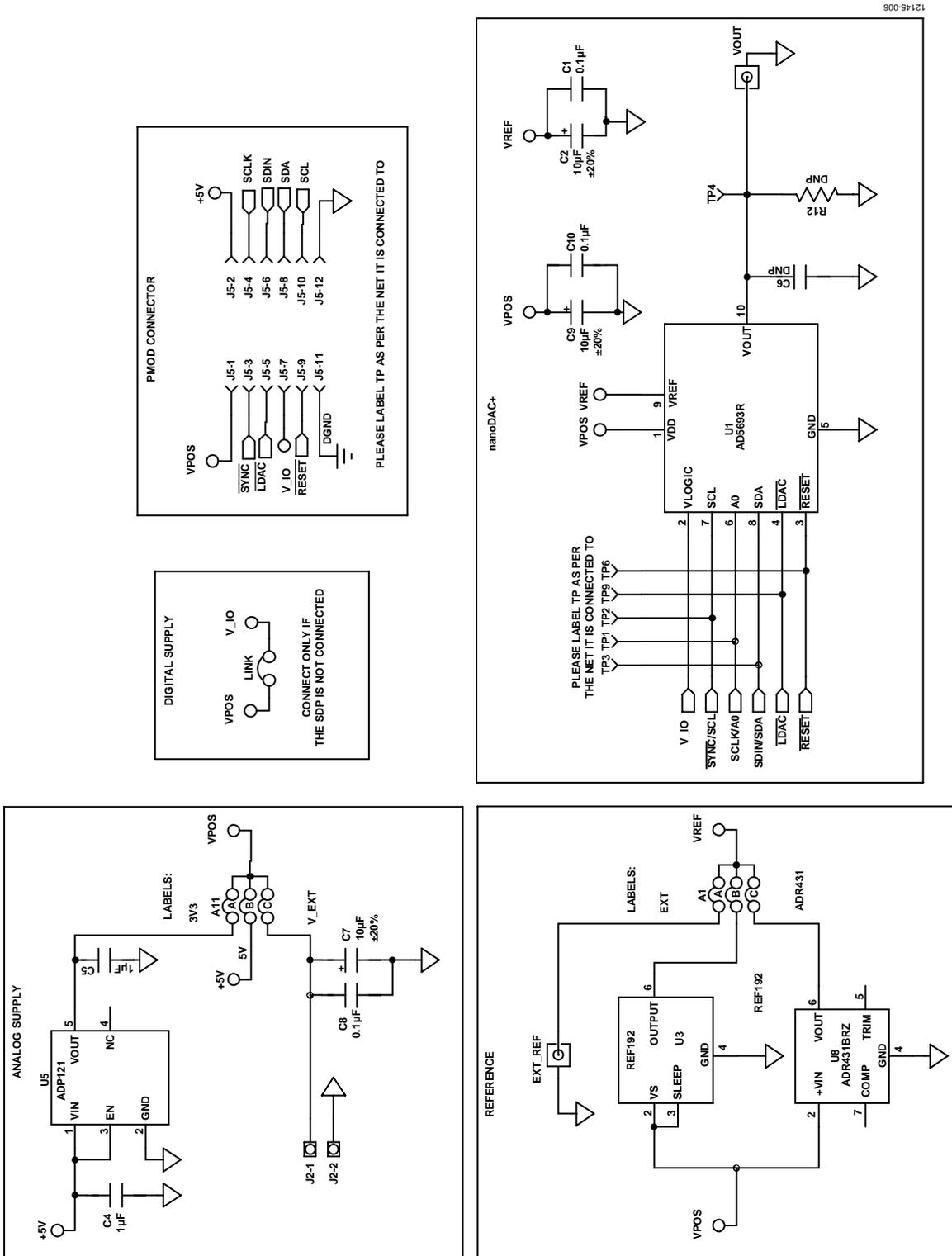
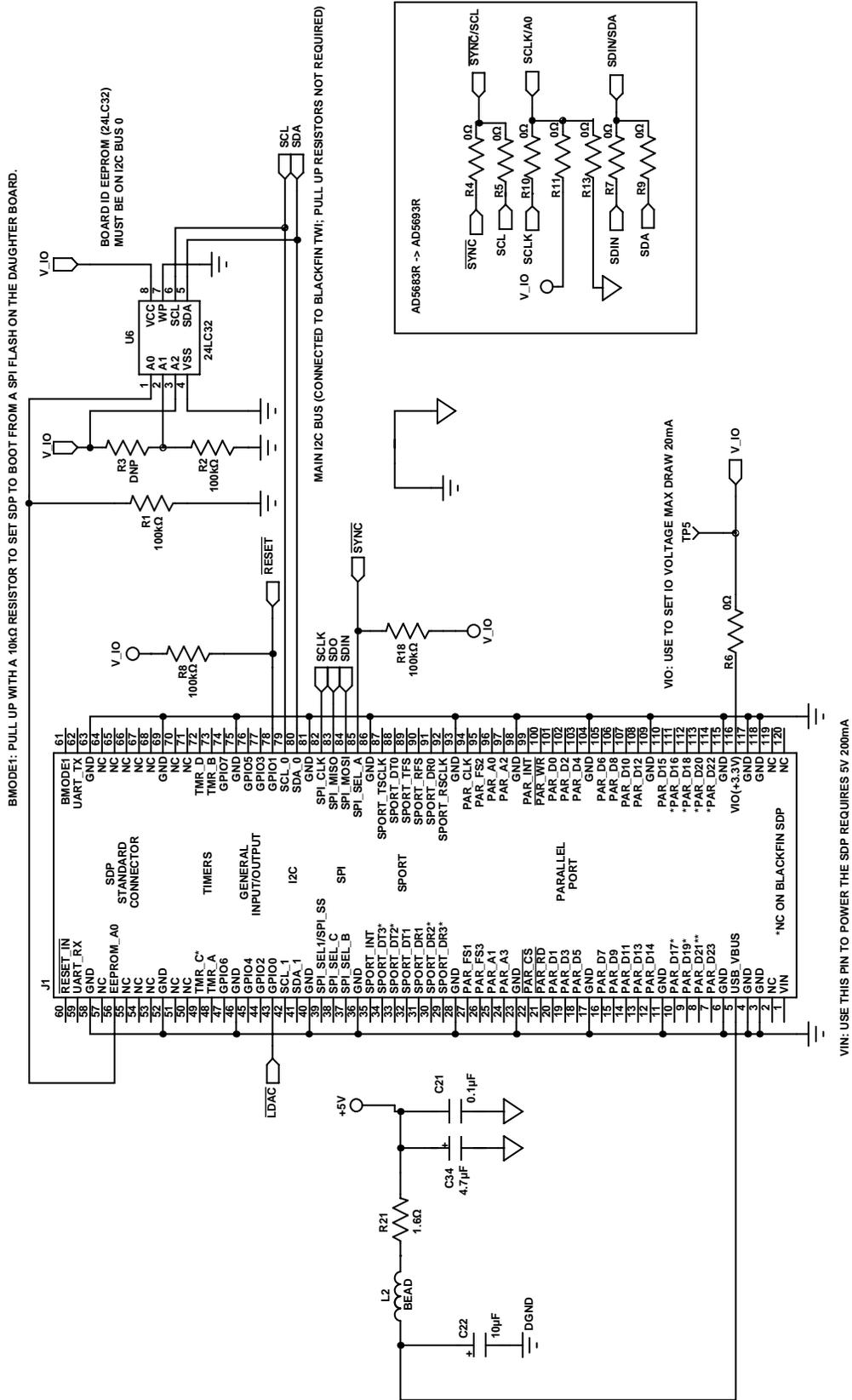


Figure 7. EVAL-AD5693RSDZ Schematic—Power Supply and Signal Routes

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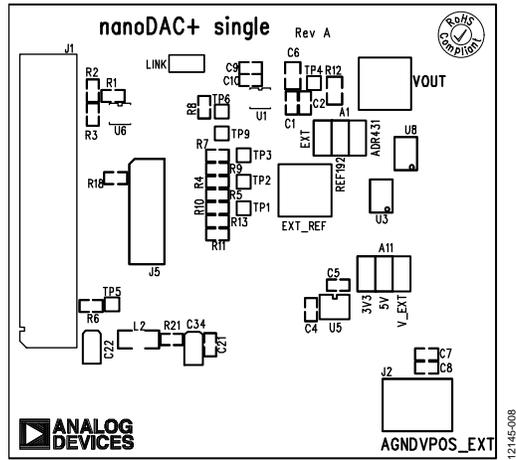


Figure 9. EVAL-AD5693RSDZ Component Placement Drawing

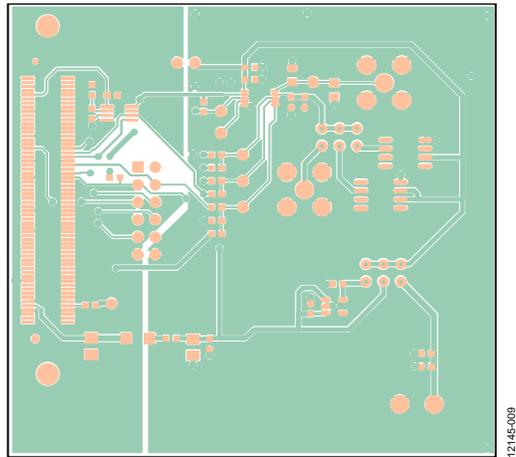


Figure 10. EVAL-AD5693RSDZ Component Side Printed Circuit Board (PCB) Drawing

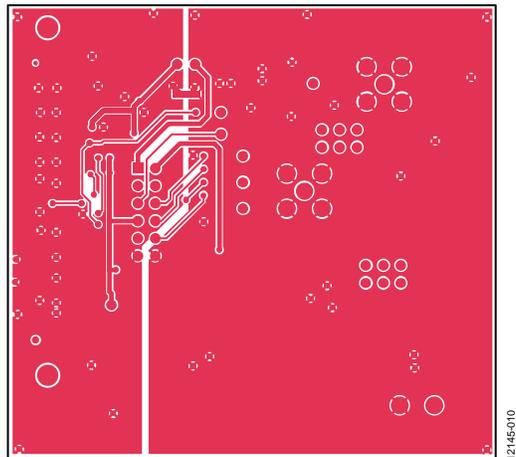


Figure 11. EVAL-AD5693RSDZ Solder Side PCB Drawing

ORDERING INFORMATION

BILL OF MATERIALS

Table 5.

Qty	Reference	Description	Supplier/Part Number ¹
1	U1	AD5693R	Analog Devices/ AD5693R
1	U3	2.5 V reference	Analog Devices/ REF192
1	U5	3.3 V regulator	Analog Devices/ ADP121
1	U6	32 kb, I ² C serial EEPROM	FEC/1331330
1	U8	Ultralow noise XFET voltage references	Analog Devices/ ADR431BRZ
1	LINK	2-pin link	FEC/1022249
2	A1, A11	3-pin link	FEC/148535
2	VOOUT, EXT_REF	SMB jack, 50 Ω	FEC/1206013
1	J1	120-way female connector	FEC/1324660
1	J2	2-pin terminal block	FEC/151789
3	C1, C8, C10	0.1 μ F, 16 V, X7R, ceramic capacitor	FEC/1216538
1	C21	0.1 μ F, 50 V, X7R, ceramic capacitor	FEC/1759122
2	C4, C5	1 μ F, 16 V, X7R, ceramic capacitor	FEC/1658870
3	C2, C7, C9	10 μ F, 10 V, X5R, 0603	FEC/1853538
1	C22	10 μ F, 6.3 V, tantalum	FEC/1190107
1	L2	Inductor	FEC/9526862
7	TP1, TP2, TP3, TP4, TP5, TP6, TP9	Test point	FEC/8731128
4	R1, R2, R8, R18	100 k Ω , SMD, resistor	FEC/9330402
1	R21	1.6 Ω , SMD, resistor	FEC/1627674
4	R5, R6, R9, R13	0 Ω , resistor	FEC/9331662

¹ FEC refers to Farnell Electronic Component Distributors.

NOTES

¹²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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