

Timing Synchronization for Multiple AD9786 TxDACs

by Steve Reine

INTRODUCTION

The AD9786 is a high performance, high speed DAC designed for use in GSM, CDMA2000, and WCDMA base stations. The architecture includes a dual digital signal path with interpolation, as well as a digital complex mixer. This architecture allows the synthesis of an IF at up to 200 MHz at the DAC output, while meeting stringent BTS requirements.

The AD9786 is a single DAC. In some applications, two or more DACs may be included in a design. Typical architectures that require more than one DAC include single sideband rejection transmitters and diversity transmitters. In these applications, the AD9786s may not be co-located, or may even be located on separate PCBs.

These designs may require the complex modulators in multiple DACs to be synchronized. The AD9786 provides a digital user interface that allows the modulators in multiple slave AD9786s to be synchronized to a single master AD9786, or intentionally offset by a programmable number of clock cycles.

There are several timing modes that are available when using the AD9786, as shown in Table 1. This application note focuses on modulator master and modulator slave modes, since these allow the user to synchronize the internal modulators.

THE AD9786 MASTER DEVICE

The default mode for many AD9786 applications is DATACLK master mode. In this mode, a clock is applied at the DAC output sample rate to CLKIN (differential CLK+/CLK-, Pins 5 and 6). A clock output (DATACLK) is provided at Pin 31 at the input data rate for data synchronization. The speed of DATACLK is simply the CLKIN rate divided by the interpolation rate. For simplicity, zero stuffing is not considered in this example. In DATACLK master mode, the output signal at Pin 31 is referred to as DATACLK.

In modulator master mode, the output signal at Pin 31 becomes a square wave at a frequency equal to CLKIN divided by 16. Also, the output signal at Pin 31 is referred to as MODCLK. Figure 1 shows an example of an AD9786 with the interpolation set to 4×. The upper signal in Figure 1 represents CLKIN. The middle plot represents the output of Pin 31 when the AD9786 is in modulator master mode, with its period equal to CLKIN divided by 16. The lower signal in Figure 1 represents the AD9786 programmed for DATACLK master mode, therefore the signal at Pin 31 is equal to the CLKIN divided by four (4× interpolation).

Table 1. AD9786 Timing Modes

| DCLKEXT 02h, Bit 3 | MODSYNC 05h, Bit 3 | DCLKCRC 02h, Bit 2 | Mode | Function |
|-----------------------|-----------------------|-----------------------|-----------------------|---|
| 1 | 0 | X | DATACLK Master | Channel data rate clock output |
| 1 | 1 | X | Modulator Master | Modulator synchronization DATACLK output |
| 0 | 0 | 0 | External Sync Mode | DATACLK inactive, DACCLK synchronous with external data |
| 0 | 0 | 1 | DATACLK Slave | DATACLK input, data rate clock, Data Recovery On |
| 0 | 1 | 0 | Low Setup/Hold | DATACLK input, input data synchronous with DATACLK |
| 0 | 1 | 1 | Modulator Slave | Input modulator synchronizer DATACLK input |

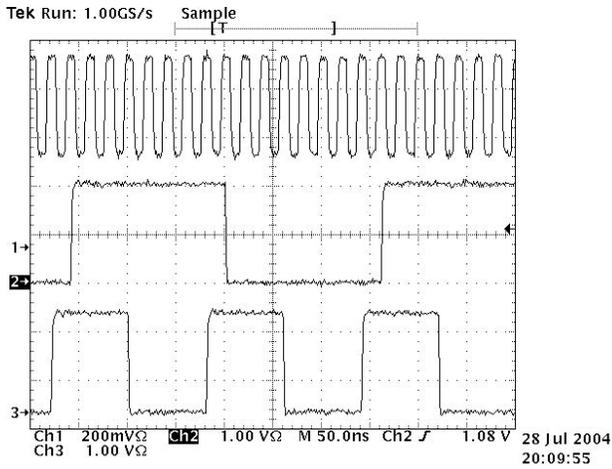


Figure 1. Comparison of DATACLK Master and Modulator Master Outputs at Pin 31, Interpolation = 4X

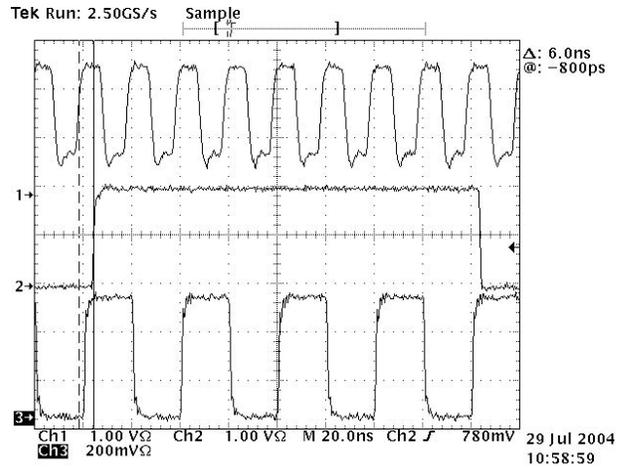


Figure 4. Timing Relationship of Modulator on AD9786 Master or Slave Device to MODCLK (MODADJ = 000) with Interpolation Set to 8X, Modulation = $f_{DAC}/2$

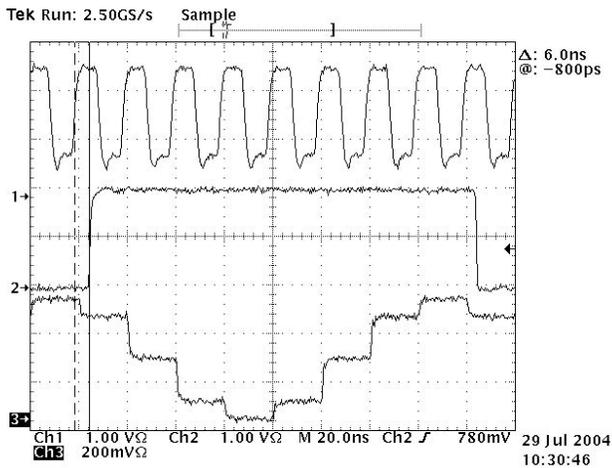


Figure 2. Timing Relationship of Modulator on AD9786 Master or Slave Device to MODCLK (MODADJ = 000) with Interpolation Set to 8X, Modulation = $f_{DAC}/8$

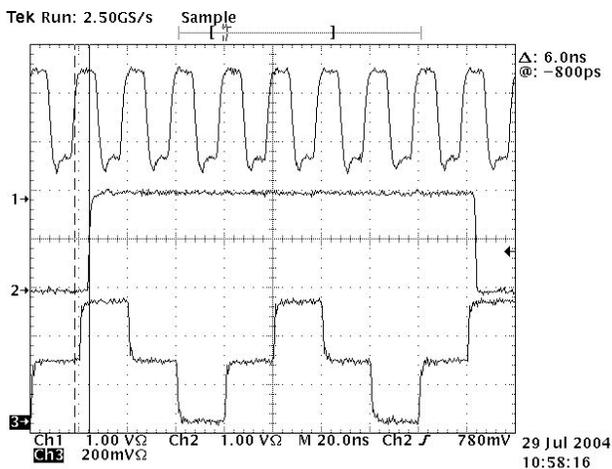


Figure 3. Timing Relationship of Modulator on AD9786 Master or Slave Device to MODCLK (MODADJ = 000) with Interpolation Set to 8X, Modulation = $f_{DAC}/4$

Figures 2 through 4 show the AD9786 in modulator mode with the interpolation filters programmed for 8X and the modulator set for $f_{DAC}/8$, $f_{DAC}/4$, and $f_{DAC}/2$. A stream of full-scale values is clocked into the AD9786, creating a dc input at the DAC full scale. The upper plots in Figures 2 through 4 represent CLKIN. The middle plots represent MODCLK, and the lower plots show the DAC output. The DAC outputs represent the alternating phases of the internal modulator updated on every CLKIN rising edge. Note that there are 16 phases of the modulator for every period of the middle plot (Pin 31 signal in modulator master mode).

Figures 2 through 4 show that there is typically a 7 ns delay from the rising edge of CLKIN to the rising/falling edge of MODCLK. The DAC output is synchronized/aligned with CLKIN on the master and slave devices, and the delay from CLKIN to DAC update is typically 3 ns.

The phase relationship of the AD9786 internal modulator, shown in Figures 2 through 4, is valid for devices programmed in master and slave modes, with the MODADJ bits (Register 05h, Bits 2:0) in the slave device set to 000. That is, if the MODADJ bits are 000 in the slave device, the modulators in the master and slave AD9786s are phase aligned. The MODADJ bits have no effect on the master device.

An imbalance in timing may exist if the CLKIN paths to the AD9786 master and slave devices are not equal in length. This can cause small differences in phase between master and slave modulators and can degrade image rejection performance.

RESET must be asserted before programming the AD9786 in these modes.

Figures 5 through 10 show the modulator synchronization when the AD9786 is in 4X and 2X interpolation. Note that the phase alignment with respect to the MODCLK edges differs depending on the interpolation rate. Master and slave modulators do not autosynchronize when interpolation is set to 1X.

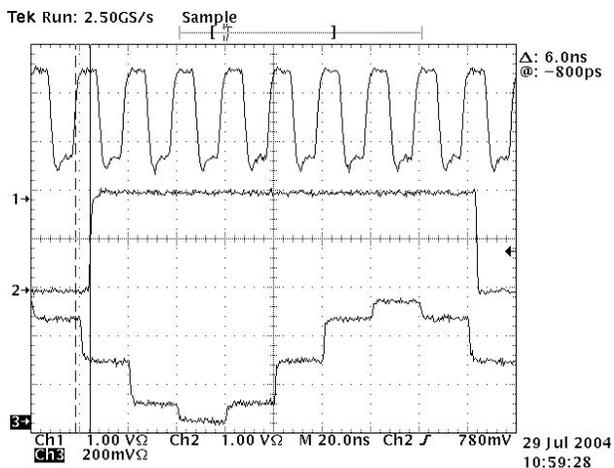


Figure 5. Timing Relationship of Modulator on AD9786 Master or Slave Device to MODCLK (MODADJ = 000) with Interpolation Set to 4×, Modulation = $f_{DAC}/8$

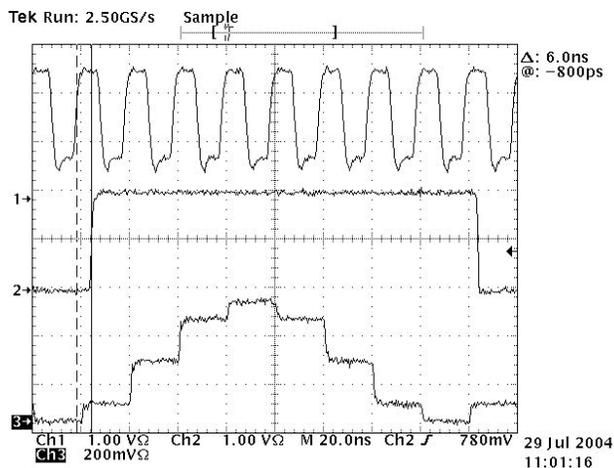


Figure 8. Timing Relationship of Modulator on AD9786 Master or Slave Device to MODCLK (MODADJ = 000) with Interpolation Set to 2×, Modulation = $f_{DAC}/8$

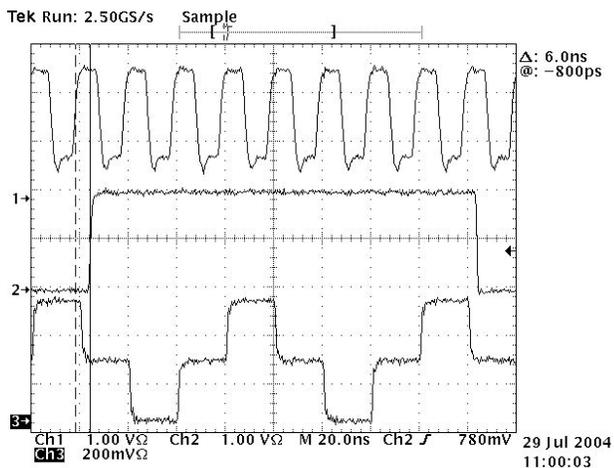


Figure 6. Timing Relationship of Modulator on AD9786 Master or Slave Device to MODCLK (MODADJ = 000) with Interpolation Set to 4×, Modulation = $f_{DAC}/4$

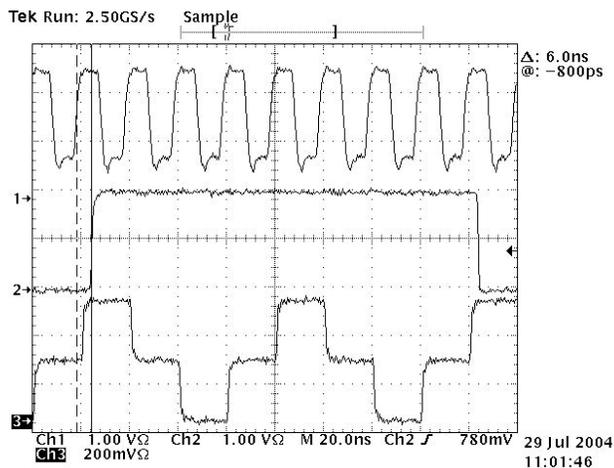


Figure 9. Timing Relationship of Modulator on AD9786 Master or Slave Device to MODCLK (MODADJ = 000) with Interpolation Set to 2×, Modulation = $f_{DAC}/4$

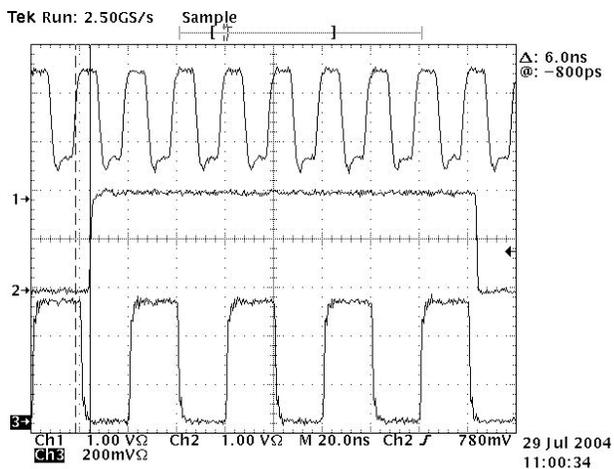


Figure 7. Timing Relationship of Modulator on AD9786 Master or Slave Device to MODCLK (MODADJ = 000) with Interpolation Set to 4×, Modulation = $f_{DAC}/2$

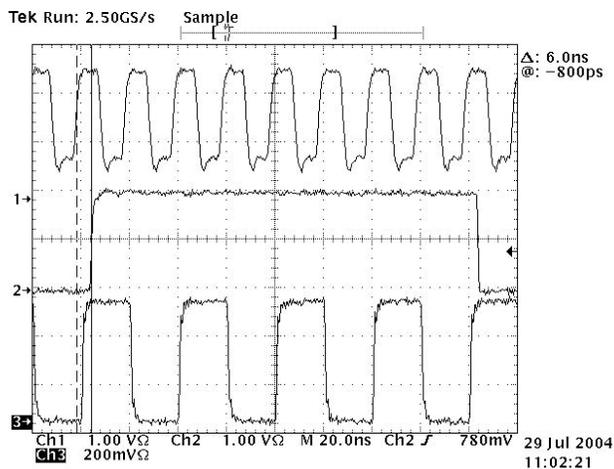


Figure 10. Timing Relationship of Modulator on AD9786 Master or Slave Device to MODCLK (MODADJ = 000) with Interpolation Set to 2×, Modulation = $f_{DAC}/2$

DATA TIMING IN MODULATOR MASTER MODE

When the AD9786 is in modulator master mode, the input data must be synchronized to the CLKIN and to MODCLK. Specifically, a rising edge of CLKIN latches the input data. With 8× interpolation, it is every eighth CLKIN rising edge; with 4× interpolation, it is every fourth rising edge; with 2× interpolation, it is every other CLKIN rising edge. This is shown in the plots in Figures 11 through 13. Note that in every situation, it is advantageous to have the data transitions occur on the edges of MODCLK. Measured setup and hold times around the latching CLKIN edges are $t_s = -0.2$ ns, and $t_h = 2.2$ ns.

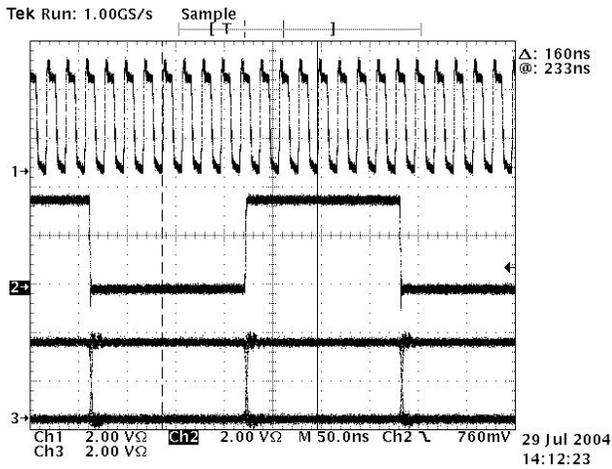


Figure 11. AD9786 in Master Modulator Mode with 8× Interpolation. The dotted and solid vertical lines represent the latching edges of CLKIN.

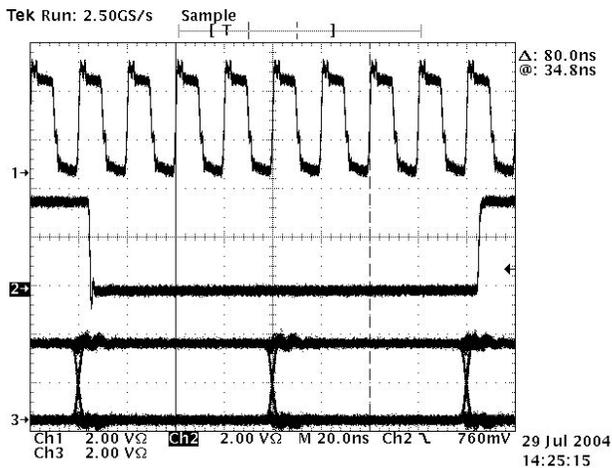


Figure 12. AD9786 in Master Modulator Mode with 4× Interpolation. The dotted and solid vertical lines represent the latching edges of CLKIN.

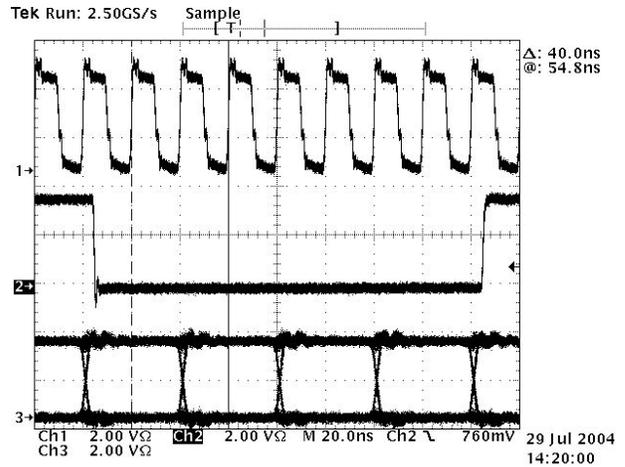


Figure 13. AD9786 in Master Modulator Mode with 2× Interpolation. The dotted and solid vertical lines represent the latching edges of CLKIN.

ADJUSTING THE DATA TIMING IN MODULATOR MASTER MODE

The timing described in Figures 11 through 13 can be adjusted with respect to MODCLK over 15 CLKIN cycles by setting the DATADJ bits (Register 5, Bits 7:4). When the DATAADJ bits are changed, the MODCLK shifts forward or backward. The latching edge of CLKIN remains in the same place in time and, therefore, moves relative to MODCLK as the DATAADJ bits are set. This capability can be used on the master AD9786 for data synchronization, but is much more useful on the slave device as it allows compensation for clock delay when the master and slave AD9786s are located far apart from each other. This is described in more detail in the Data Timing in Modulator Slave Mode section.

Figures 14 through 18 show the effect of various settings of DATAADJ. In all four plots, the input data transitions (third trace) are intentionally placed on the latching edges of CLKIN. As the plots show, MODCLK moves with DATADJ, while the latching edge of CLKIN remains constant.

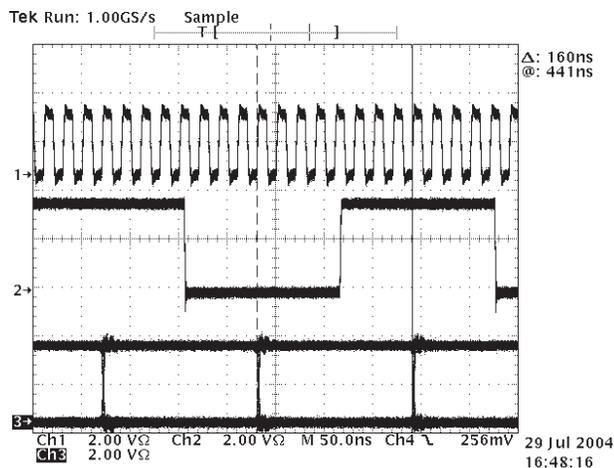


Figure 14. AD9786 in Master Modulator Mode with 8× Interpolation. The dotted and solid vertical lines represent the latching edges of CLKIN. DATAADJ = 0000. These conditions are identical to Figure 11.

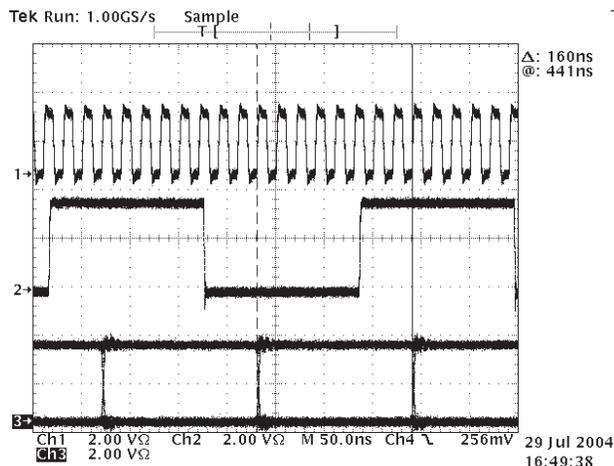


Figure 15. AD9786 in Master Modulator Mode with 8× Interpolation. The dotted and solid vertical lines represent the latching edges of CLKIN. DATAADJ = 0001.

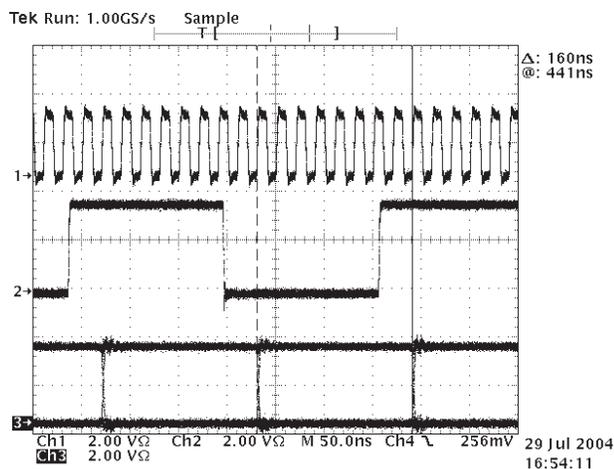


Figure 16. AD9786 in Master Modulator Mode with 8× Interpolation. The dotted and solid vertical lines represent the latching edges of CLKIN. DATAADJ = 0010.

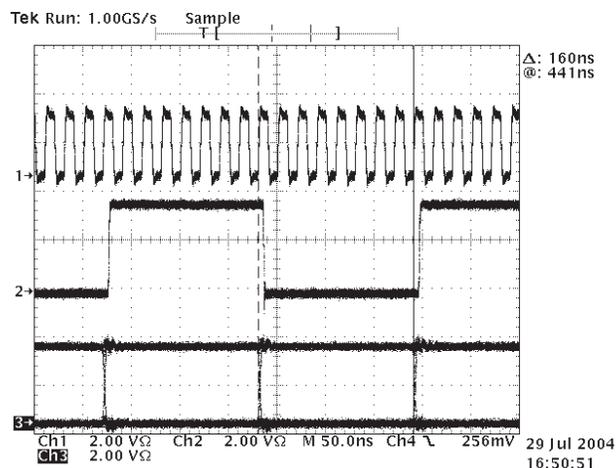


Figure 17. AD9786 in Master Modulator Mode with 8× Interpolation. The dotted and solid vertical lines represent the latching edges of CLKIN. DATAADJ = 0100.

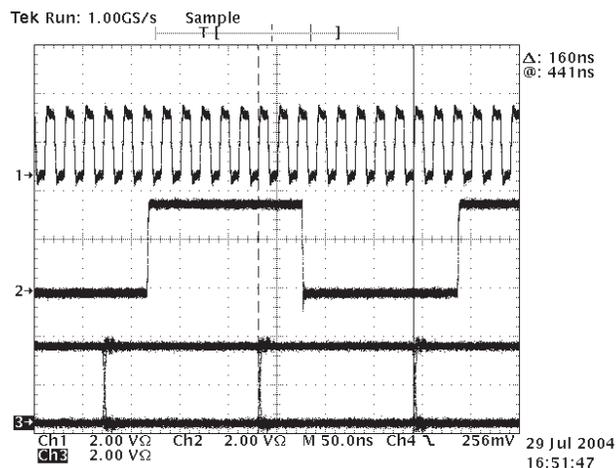


Figure 18. AD9786 in Master Modulator Mode with 8× Interpolation. The dotted and solid vertical lines represent the latching edges of CLKIN. DATAADJ = 0110.

THE AD9786 SLAVE DEVICE

When the AD9786 is programmed for modulator slave mode, it requires a MODCLK signal at the slave device Pin 31. As stated previously, when the MODADJ bits in the slave device are set to 000, and reset is asserted and then de-asserted, the phase of the slave modulator matches the phase of the master modulator.

The MODADJ bits in the slave device can be used to move the phase of the slave modulator by up to seven CLKIN cycles. Figures 19 through 25 represent the conditions of Figures 2 through 4 (interpolation = 8×, modulator = $f_{DAC}/8$), but with the MODADJ bits set over their range.

When the AD9786 slave device modulator is set to $f_{DAC}/4$, there are only four possible output phases for the internal modulator. Therefore, only MODADJ Bits 2:1 have any effect on the modulator alignment. With the modulator set to $f_{DAC}/2$, the MODADJ bits have no effect.

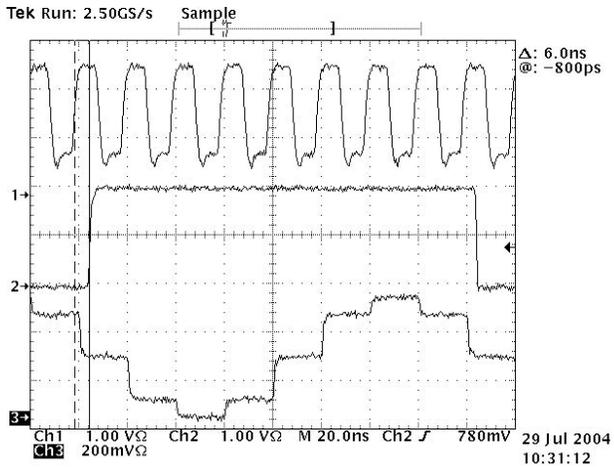


Figure 19. Timing Relationship of Modulator on AD9786 Slave Device to MODCLK Input, Interpolation = 8X, Modulator = $f_{DAC}/8$ MODADJ = 0,0,1

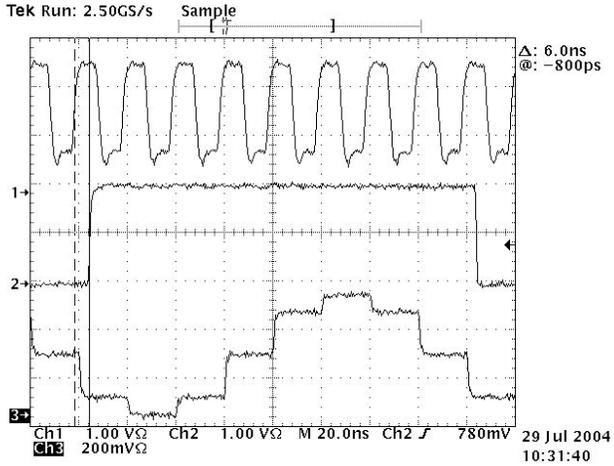


Figure 20. MODADJ = 0,1,0

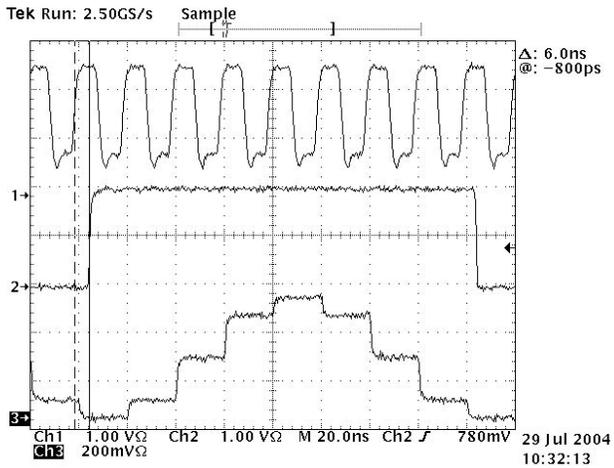


Figure 21. MODADJ = 0,1,1

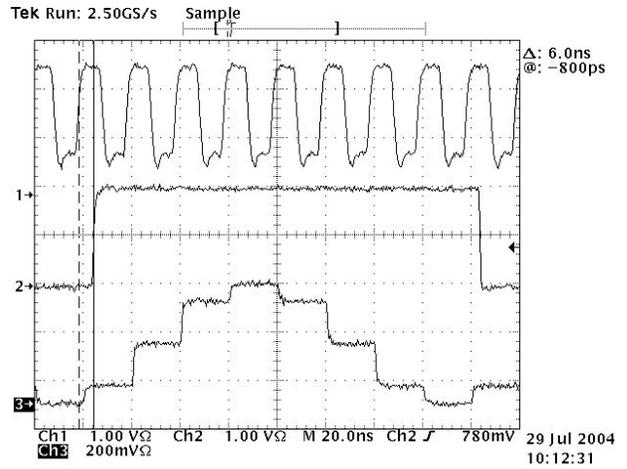


Figure 22. MODADJ = 1,0,0

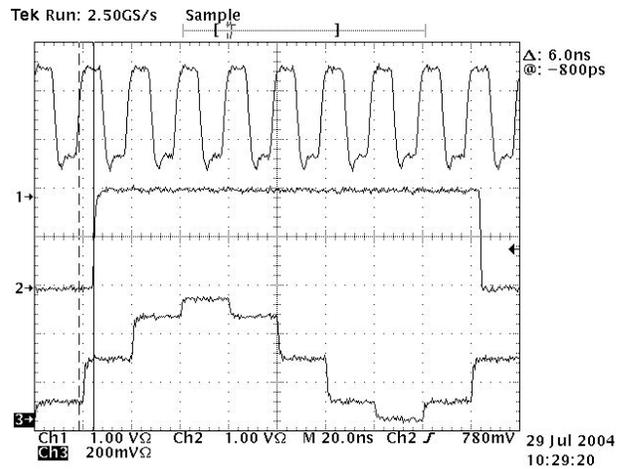


Figure 23. MODADJ = 1,0,1

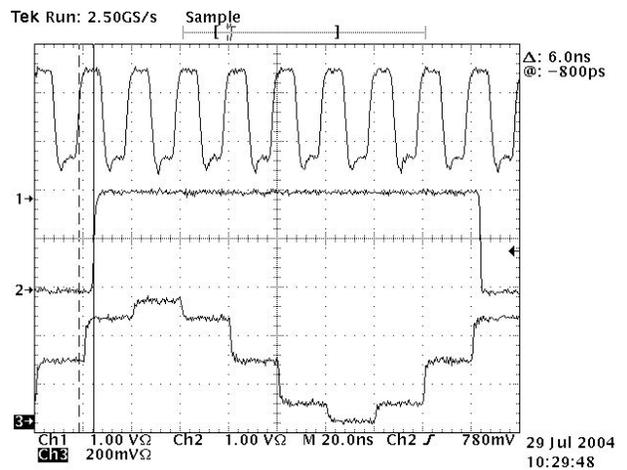


Figure 24. MODADJ = 1,1,0

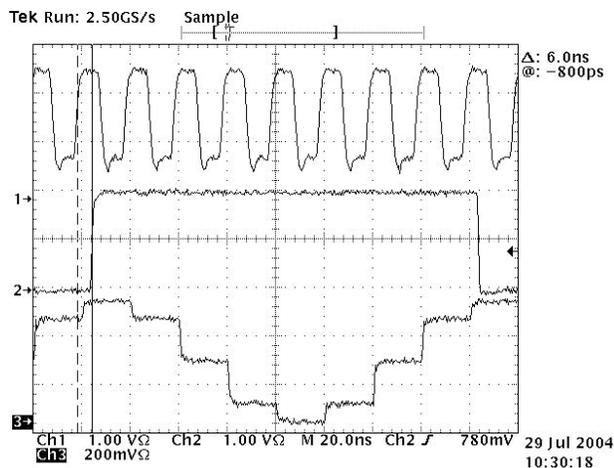


Figure 25. MODADJ = 1,1,1

DATA TIMING IN MODULATOR SLAVE MODE

As in modulator master mode, in modulator slave mode the input data must be synchronized to the CLKIN and to MODCLK. In the description of master mode, the latching edge of CLKIN remained constant while MODCLK was moved back and forth with DATAADJ. In slave mode, with MODCLK as an input, MODCLK remains constant, while the CLKIN latching edge moves as the DATAADJ bits are changed. This programmable capability eases the burden of the data timing on the user. The effect of the DATAADJ bits is shown in Figures 26 through 30. As in Figures 14 through 18, the input data transitions (third trace) are intentionally placed on the latching edges of CLKIN.

The data setup and hold times for the input data with respect to CLKIN are $t_s = -0.2$ ns, and $t_h = 2.2$ ns, the same as in modulator master mode.

In modulator slave mode, MODCLK is an input, therefore, its timing must also be defined with respect to CLKIN. The position of the MODCLK rising edge, with respect to the nearest CLKIN rising edge, determines the data latching edge of CLKIN. In Figure 31, the latching CLK edge is shown when DATAADJ is 0000, and the rising edge of MODCLK occurs at least 2.4 ns before the nearest CLKIN rising edge. In Figure 32, which is more representative of the data in this application note, the rising edge of MODCLK occurs at the same time (0 ns) or after the nearest rising edge of CLKIN. DATAADJ is still 0000 in Figure 32.

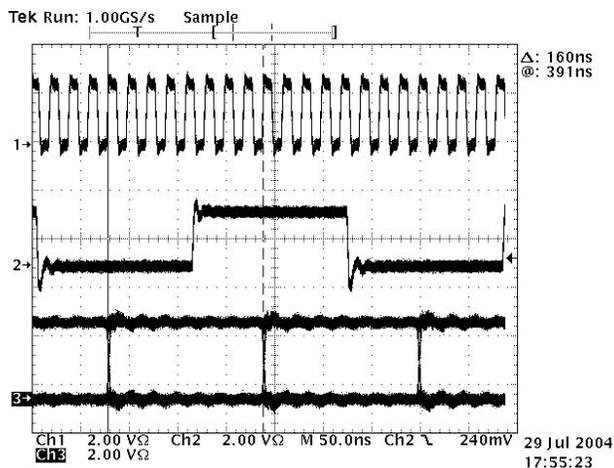


Figure 26. AD9786 in Slave Modulator Mode with 8× Interpolation. The dotted and solid vertical lines represent the latching edges of CLKIN. DATAADJ = 0000.

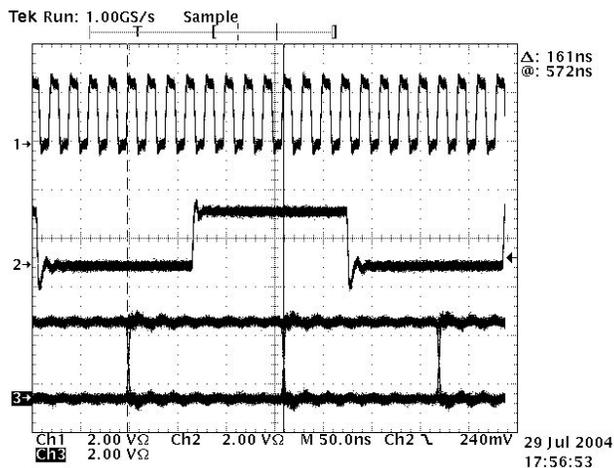


Figure 27. AD9786 in Slave Modulator Mode with 8× Interpolation. The dotted and solid vertical lines represent the latching edges of CLKIN. DATAADJ = 0001.

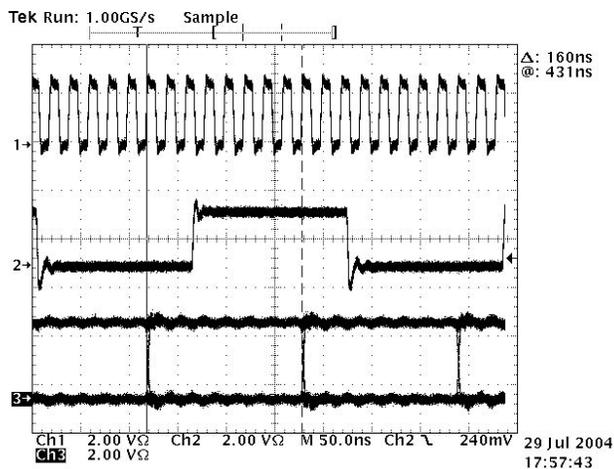


Figure 28. AD9786 in Slave Modulator Mode with 8× Interpolation. The dotted and solid vertical lines represent the latching edges of CLKIN. DATAADJ = 0010.

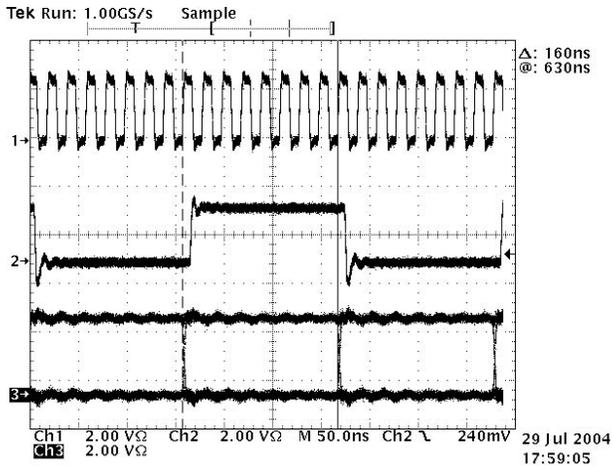


Figure 29. AD9786 in Slave Modulator Mode with 8× Interpolation. The dotted and solid vertical lines represent the latching edges of CLKIN. DATAADJ = 0100.

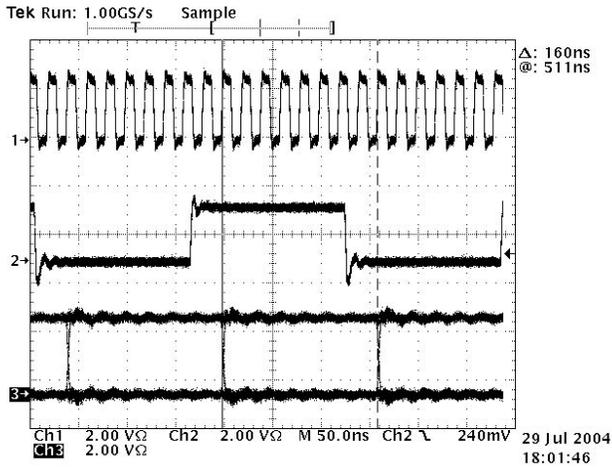


Figure 30. AD9786 in Modulator Slave Mode with 8× Interpolation. The dotted and solid vertical lines represent the latching edges of CLKIN. DATAADJ = 0110.

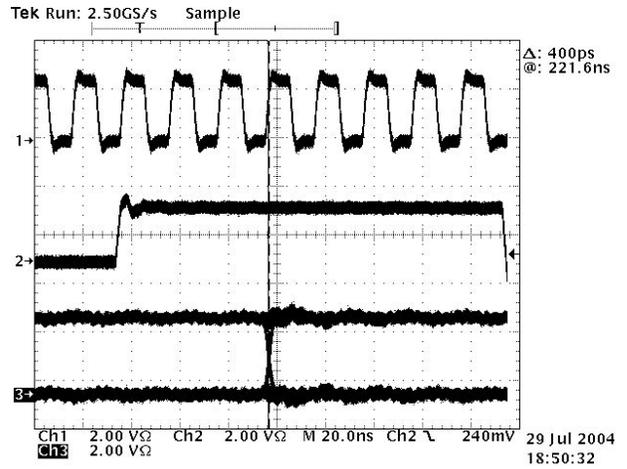


Figure 31. AD9786 Modulator Slave Mode Timing with 8× Interpolation. The rising edge of MODCLK occurs at least 2.4 ns before the rising edge of CLKIN. The vertical lines represent the latching edges of CLKIN. DATAADJ = 0000.

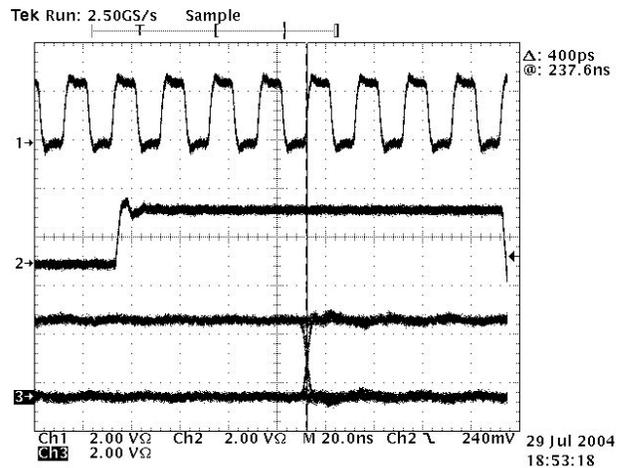


Figure 32. AD9786 Modulator Slave Mode Timing with 8× Interpolation. The rising edge of MODCLK occurs 0.0 ns or more after the rising edge of CLKIN. The vertical lines represent the latching edges of CLKIN. DATAADJ = 0000.