REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A

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TITLE

MICROCIRCUIT, DIGITAL-LINEAR, QUAD, CURRENT OUTPUT, SERIAL INPUT 16 BIT DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON

SIZE	CODE IDENT. NO.	DWG NO.
A	16236	V62/12663

REV

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AMSC N/A

5962-V004-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance quad, current output, serial input 16 bit digital to analog converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12663	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD5544	Quad, current output, serial input 16 bit digital to analog converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	28	MO-150-AH	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Positive power supply (V_{DD}) to ground (GND) ..... -0.3 V, +8 V
Negative power supply (V_{SS}) to GND ..... +0.3 V, -7 V
Reference voltage input ($V_{REF}x$) to GND ..... -18 V, +18 V
Logic input and output to GND ..... -0.3 V, +8 V
Voltage at current output ($V(I_{OUT}x)$) to GND ..... -0.3 V, V_{DD} + 0.3 V
Analog ground ($A_{GND}x$) to digital ground (DGND) ..... -0.3 V, +0.3 V
Input current to any pin except supplies ..... ±50 mA
Power dissipation (P_D) ..... See table I.
Maximum junction temperature range (T_J) ..... 150°C
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature:
  Vapor phase, 60 seconds ..... 215°C
  Infrared, 15 seconds ..... 220°C

1.4 Recommended operating conditions. 2/

Positive power supply (V_{DD}) ..... 2.7 V to 5.5 V
Operating free-air temperature range (T_A) ..... -55°C to +125°C

1.5 Thermal characteristics.

Thermal resistance, junction to ambient (θ_{JA}) ..... 100°C/W

1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Timing waveforms. The timing waveforms shall be as shown in figure 3.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Static performance. 3/							
Resolution	N	1 LSB = V_{REF} / 2^{16} = 153 μV when V_{REF} = 10 V	-55°C to +125°C	01		16	Bits
Relative accuracy	INL		-55°C to +125°C	01		±1.5	LSB
Differential nonlinearity	DNL		-55°C to +125°C	01		±1.5	LSB
Output leakage current	I_{OUT}	Data = 0x0000	+25°C	01		10	nA
			+85°C			20	
Full scale gain error	G_{FSE}	Data = 0xFFFF	-55°C to +125°C	01		±4	mV
Full scale temperature coefficient 4/	TCV_{FS}		-55°C to +125°C	01	1 typical		ppm/°C
Feedback resistor	$R_{FB}x$	V_{DD} = 5 V	-55°C to +125°C	01	4	8	kΩ
Reference input.							
$V_{REF}x$ range	$V_{REF}x$		-55°C to +125°C	01	-15	+15	V
Input resistance	$R_{REF}x$		-55°C to +125°C	01	4	8	kΩ
Input resistance match	$R_{REF}x$	Channel to channel	-55°C to +125°C	01	0.35 typical		%
Input capacitance 4/	$C_{REF}x$		-55°C to +125°C	01	5 typical		pF
Analog output.							
Output current	$I_{OUT}x$	Data = 0xFFFF	-55°C to +125°C	01	1.25	2.5	mA
Output capacitance 4/	$C_{OUT}x$	Code dependent	-55°C to +125°C	01	35 typical		pF
Logic inputs and output.							
Logic input low voltage	V_{IL}		-55°C to +125°C	01		0.8	V
Logic input high voltage	V_{IH}		-55°C to +125°C	01	2.4		V
Input leakage current	I_{IL}		-55°C to +125°C	01		1	μA
Input capacitance 4/	C_{IL}		-55°C to +125°C	01		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
Logic inputs and output – continued.							
Logic output low voltage	V_{OL}	I_{OL} = 1.6 mA	-55°C to +125°C	01		0.4	V
Logic output high voltage	V_{OH}	I_{OH} = 100 µA	-55°C to +125°C	01	4		V
Interface timing. 4/ 5/							
Clock width high	t_{CH}		-55°C to +125°C	01	25		ns
Clock width low	t_{CL}		-55°C to +125°C	01	25		ns
$\overline{CS}$ to clock setup	t_{CSS}		-55°C to +125°C	01	0		ns
Clock to $\overline{CS}$ hold	t_{CSH}		-55°C to +125°C	01	25		ns
Clock to SDO propagation delay	t_{PD}		-55°C to +125°C	01	2	20	ns
Load DAC pulse width	t_{LDAC}		-55°C to +125°C	01	25		ns
Data setup	t_{DS}		-55°C to +125°C	01	20		ns
Data hold	t_{DH}		-55°C to +125°C	01	20		ns
Load setup	t_{LDS}		-55°C to +125°C	01	5		ns
Load hold	t_{LDH}		-55°C to +125°C	01	25		ns
Supply characteristics.							
Power supply range	V_{DD} RANGE		-55°C to +125°C	01	2.7	5.5	V
Positive supply current	I_{DD}	Logic inputs = 0 V	-55°C to +125°C	01		5	µA
Negative supply current	I_{SS}	Logic inputs = 0 V, V_{SS} = -5 V	-55°C to +125°C	01		9	µA
Power dissipation	P_D	Logic inputs = 0 V	-55°C to +125°C	01		1.25	mW
Power supply sensitivity	PSS	ΔV_{DD} = ±5%	-55°C to +125°C	01		0.006	%/%

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions 2/	Temperature, T_A	Device type	Limits		Unit
					Min	Max	
AC characteristics. 6/							
Output voltage settling time	t_S	To ±0.1% of full scale, data = 0x0000 to 0xFFFF to 0x0000	-55°C to +125°C	01	0.9 typical		µs
Reference multiplying bandwidth	BW – 3 dB	$V_{REF}x$ = 5 Vp-p, data = 0xFFFF, C_{FB} = 2.0 pF	-55°C to +125°C	01	12 typical		MHz
DAC glitch impulse	Q	$V_{REF}x$ = 8 V rms, data = 0x0000 to 0x8000 to 0x0000	-55°C to +125°C	01	-1 typical		nV-sec
Feedthrough error	$V_{OUT}x$/ $V_{REF}x$	Data = 0x0000, $V_{REF}x$ = 100 mV rms, f = 100 kHz	-55°C to +125°C	01	-65 typical		dB
Crosstalk error	$V_{OUT}A$/ $V_{REF}B$	Data = 0x0000, $V_{REF}B$ = 100 mV rms, adjacent channel, f = 100 kHz	-55°C to +125°C	01	-90 typical		dB
Digital feedthrough	Q	$\overline{CS}$ = 1, f_{CLK} = 1 MHz	-55°C to +125°C	01	0.6 typical		nV-sec
Total harmonic distortion	THD	$V_{REF}x$ = 5 Vpp, data = 0xFFFF, f = 1 kHz	-55°C to +125°C	01	-98 typical		dB
Output spot noise voltage	e_N	f = 1 kHz, BW = 1 Hz	-55°C to +125°C	01	7 typical		nV / $\sqrt{Hz}$

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ Unless otherwise specified, V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V, $I_{OUT}x$ = virtual GND, $A_{GND}x$ = 0 V, $V_{REF}A$ = $V_{REF}B$ = $V_{REF}C$ = $V_{REF}D$ =10 V, and T_A = full temperature range.

3/ All static performance tests (except $I_{OUT}x$) are performed in a closed loop system using an external precision OP177 current to voltage amplifier. The device R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at 25°C.

4/ These parameters are guaranteed by design and are not subject to production testing.

5/ All input control signals are specified with t_R = t_F = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

6/ All ac characteristic tests are performed in a closed loop system using an AD8038 current to voltage converter amplifier.

Case X

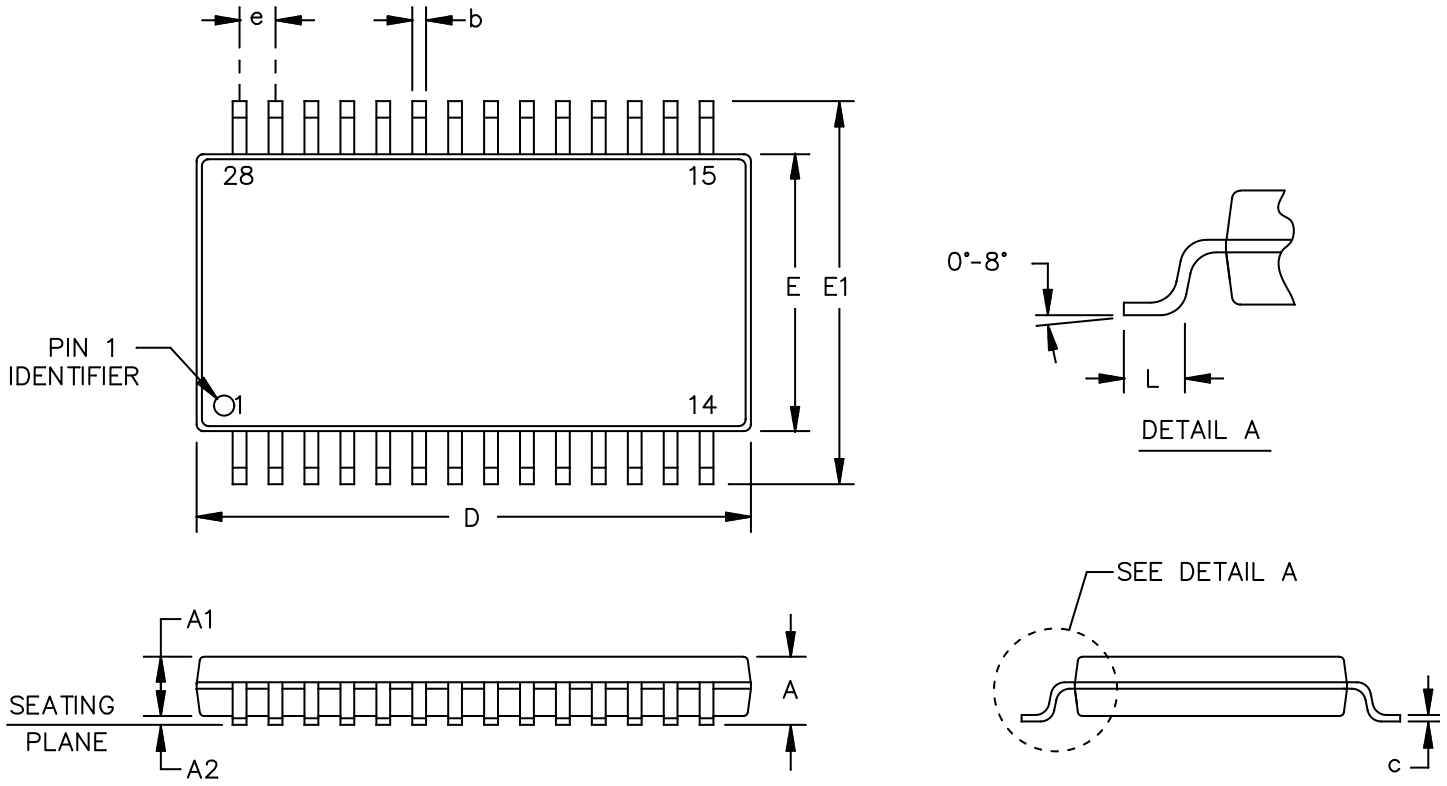

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12663
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Case X

Symbol	Dimensions					
	Inches			Millimeters		
	Min	Med	Max	Min	Med	Max
A	---	---	.078	---	---	2.00
A1	.064	.068	.072	1.65	1.75	1.85
A2	.001	---	.003	0.05	---	0.10
b	.008	---	.014	0.22	---	0.38
c	.003	---	.009	0.09	---	0.25
D	.389	.401	.413	9.90	10.20	10.50
E	.196	.208	.220	5.00	5.30	5.60
E1	.291	.307	.322	7.40	7.80	8.20
e	.025 BSC			0.65 BSC		
L	.021	.029	.037	0.55	0.75	0.95

NOTES:
1. Controlling dimensions are inch, millimeter dimensions are given for reference only.
2. Falls within reference to JEDEC MO-150-AH.

FIGURE 1. Case outline - Continued.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	$A_{GND}A$	DAC A analog ground.
2	$I_{OUT}A$	DAC A current output.
3	$V_{REF}A$	DAC A reference voltage input terminal. Establishes DAC A full scale output voltage. This pin can be tied to the V_{DD} pin.
4	$R_{FB}A$	Establish the voltage output for DAC A by connecting to an external amplifier output.
5	MSB	MSB pin. Set pin during a reset pulse ($\overline{RS}$) or at system power on if tied to ground or V_{DD}.
6	$\overline{RS}$	Reset pin, active low input. Input register and DAC registers are set to all 0's or half scale code, determined by the voltage on the MSB pin. Register data = 0x0000 when MSB = 0.
7	V_{DD}	Positive power supply input. Specified range of operation: 5 V $\pm$ 10 %.
8	$\overline{CS}$	Chip select, active low input. Disable shift register loading when high. Transfers serial register data to the input register when $\overline{CS}$ / $\overline{LDAC}$ returns high. Does not affect $\overline{LDAC}$ operation.
9	CLK	Clock input. Positive edge clocks data into the shift register.
10	SDI	Serial data input. Input data loads directly into the shift register.
11	$R_{FB}B$	Establish the voltage output for DAC B by connecting to an external amplifier output.
12	$V_{REF}B$	DAC B reference voltage input terminal. Establishes DAC B full scale output voltage. This pin can be tied to the V_{DD} pin.
13	$I_{OUT}B$	DAC B current output.
14	$A_{GND}B$	DAC B analog ground.

FIGURE 2. Terminal connections.

Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
15	$A_{GND}C$	DAC C analog ground.
16	$I_{OUT}C$	DAC C current output.
17	$V_{REF}C$	DAC C reference voltage input terminal. Establishes DAC C full scale output voltage. This pin can be tied to the V_{DD} pin.
18	$R_{FB}C$	Establish the voltage output for the DAC C by connecting to an external amplifier output.
19	NC	No connect. Do not connect to this pin.
20	SDO	Serial data output. Input data loads directly into the shift register. Data appears at SDO at 19 clock pulses for the device after input at the SDI pin.
21	$\overline{LDAC}$	Load DAC register strobe, level sensitive active low. Transfer all input register data to DAC registers. Asynchronous active low input.
22	AGNDF	High current analog force ground.
23	V_{SS}	Negative bias power supply input. Specified range of operation: -5.5 V to +0.3 V.
24	DGND	Digital ground pin.
25	$R_{FB}D$	Establish the voltage output for DAC D by connecting to an external amplifier output.
26	$V_{REF}D$	DAC D reference voltage input terminal. Establishes DAC D full scale output voltage. This pin can be tied to the V_{DD} pin.
27	$I_{OUT}D$	DAC D current output.
28	$A_{GND}D$	DACD analog ground.

FIGURE 2. Terminal connections - continued.

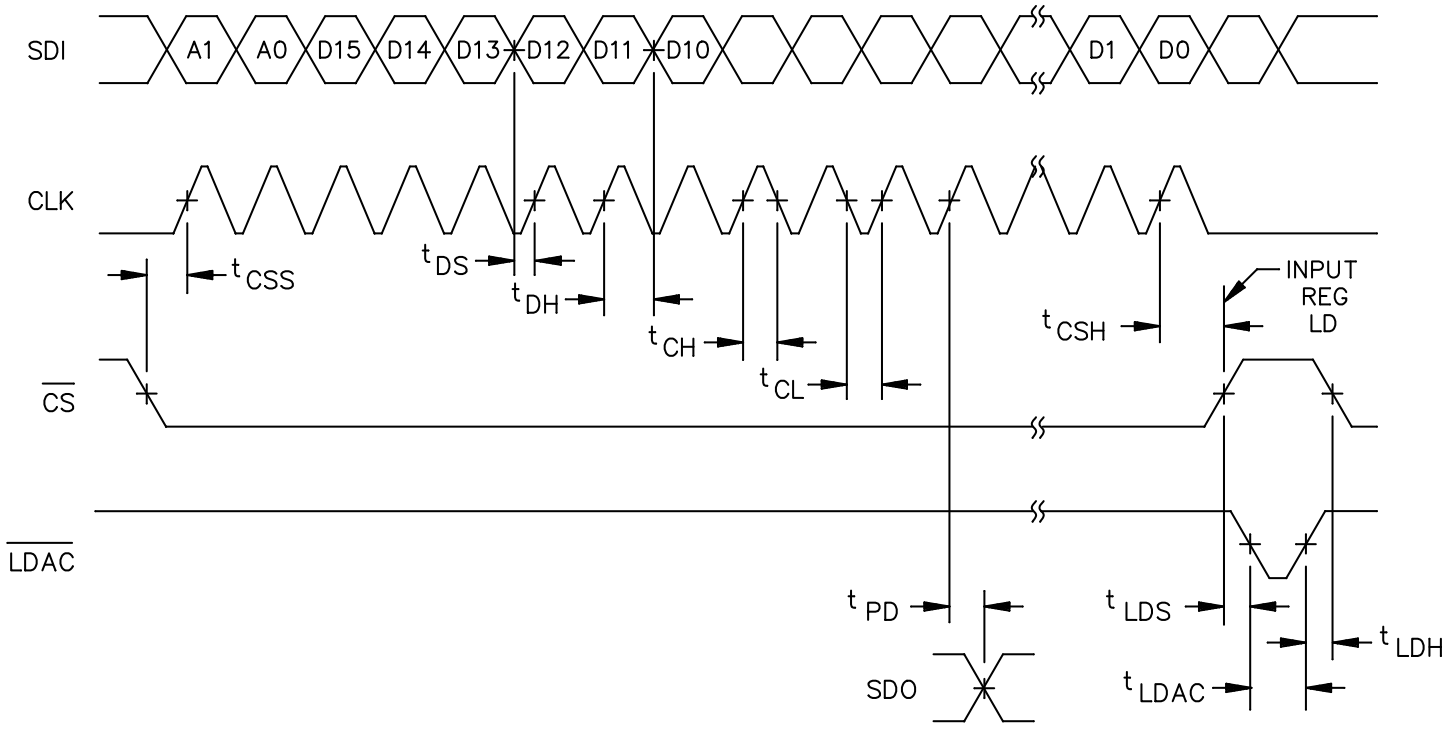

FIGURE 3. Timing waveforms.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12663-01XB	24355	AD5544SRS-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland