REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R120-92.	92-01-27	Michael A. Frye
B	Drawing updated to reflect current requirements. - lgt	01-12-17	Raymond Monnin
C	Redrawn. Update paragraphs to MIL-PRF-38535 requirements. - drw	13-09-20	Charles F. Saffle

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			C	C	C	C	C	C	C	C	C	C	C			
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11			

PMIC N/A

PREPARED BY
Rick C. Officer

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles E. Besore

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
89-12-28

REVISION LEVEL
C

MICROCIRCUIT, LIINEAR, DUAL, CMOS, 12-BIT, D/A CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89657**

SHEET 1 OF 11

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89657	01	L	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function	Gain error
01	7547S	Dual, CMOS, 12-bit D/A converter	±6.0 LSB
02	7547T	Dual, CMOS, 12-bit D/A converter	±3.0 LSB
03	7547U	Dual, CMOS, 12-bit D/A converter	±2.0 LSB

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	Dual-in-line
3	CQCC1-N28	28	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

V_{DD} to DGND	0.3 V dc to +17 V dc
V_{REFA}, V_{REFB}, to AGND	±25 V dc
V_{RFBA}, V_{RFBB}, to AGND	±25 V dc
Digital input voltage to DGND	0.3 V dc to V_{DD} +0.3 V
Voltage at I_{OUTA}, I_{OUTB} to DGND	-0.3 V dc to V_{DD} +0.3 V
AGND to DGND	-0.3 V dc to V_{DD} +0.3 V
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation (P_D)	450 mW 1/
Thermal resistance, junction to case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction to ambient (θ_{JA})	120°C C/W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})	10.8 V dc to 16.5 V dc
Minimum high level input voltage	2.4 V dc
Maximum low level input voltage	0.8 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C
Voltage at V_{REFA}, V_{REFB}	10 V dc
Voltage at AGND, I_{OUTA}	0 V dc
Voltage at AGND, I_{OUTB}	0 V dc

1/ Derate above T_A = +75°C at 6.0 mW/°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution 2/	RES	Guaranteed minimum resolution	1, 2, 3	All	12		Bits
Relative accuracy	R_A	V_{DD} = 10.8 V and 16.5 V	1, 2, 3	01		±1.0	LSB
			1	02, 03		±1.0	
			2, 3, 12			±0.5	
Differential nonlinearity	DNL	Guaranteed monotonic to 12-bits , V_{DD} = 10.8 V and 16.5 V	1, 2, 3	All		±1.0	LSB
Gain error	A_E	Measured using R_{FBA} and R_{FBB}. Both DAC registers loaded with all 1's, V_{DD} = 10.8 V.	1, 2, 3	01		±6.0	LSB
			1	02		±3.0	
				03		±2.0	
			2, 3, 12	02		±3.0	
				03		±2.0	
Gain temperature coefficient 2/	$\frac{\Delta A_E}{\Delta T}$		4	All		±5.0	ppm/°C
Power supply rejection ratio, V_{REFB} to I_{OUTB}	PSRR	V_{DD} = 10.8 V and 16.5 V	1	All		±0.01	%/%
		V_{DD} = 10.8 V	2, 3			±0.02	
Output leakage current	I_{OUTA}	DAC A loaded with all 0's, V_{DD} = 16.5 V	1	All		±10	nA
			2, 3			±250	
	I_{OUTB}	DAC B loaded with all 0's, V_{DD} = 16.5 V	1	All		±10	nA
			2, 3			±250	
Output current settling time to 0.01% of FSR 2/	t_{SL}	I_{OUT} load = 100Ω, C_{EXT} = 13 pF, DAC output measured from falling edge of $\overline{WR}$	9	All		1.5	µs
			10, 11			1.5	
Feedthrough error, 2/ V_{REFA} to I_{OUTA} or V_{REFB} to I_{OUTB}	FT	V_{REFA} = V_{REFB} = ±20 Vpp, 10 kHz sine wave, DAC register loaded with all 0's	4	All		-65	dB
			5, 6			-65	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Reference input resistance	R_{IN}	V_{DD} = 10.8 V	1, 2, 3	All	9.0	20	kΩ
Reference input resistance match (V_{REFA}/V_{REFB})	R_{MIN}	V_{DD} = 10.8 V	1, 2, 3	01, 02		±3.0	%
			1	03		±3.0	
			2, 3			±1.0	
Digital input high voltage	V_{IH}	V_{DD} = 10.8 V and 16.5 V	1, 2, 3	All	2.4		V
Digital input low voltage	V_{IL}	V_{DD} = 10.8 V and 16.5 V	1, 2, 3	All		0.8	V
Input current	I_{IN}	$V_{IN} = V_{DD}$ = 16.5 V	1	All		1.0	μA
			2, 3			10	
Digital input capacitance 2/	C_{IN}	T_A = +25°C	4	All		10	pF
Output capacitance 2/	C_{OUTA}	DAC A = all 0's, T_A = +25°C	4	All		70	pF
		DAC A = all 1's, T_A = +25°C				140	
Output capacitance 2/	C_{OUTB}	DAC B = all 0's, T_A = +25°C	4	All		70	pf
		DAC B = all 1's, T_A = +25°C				140	
Functional test		See 4.3.1c	7	All			
Data setup time	t_{DS}	See figure 3	9	All	60		ns
			10, 11 2/		80		
Data hold time	t_{DH}	See figure 3	9	All	25		ns
			10, 11 2/		25		
Chip select or update to write setup time	t_{CWS}	See figure 3	9	All	80		ns
			10, 11 2/		100		
Chip select or update to write hold time	t_{CWH}	See figure 3	9	All	0		ns
			10, 11 2/		0		
Write pulse width	t_{WR}	See figure 3	9	All	80		ns
			10, 11 2/		100		
Supply current	I_{DD}	V_{DD} = 16.5 V	1, 2, 3	All		2.0	mA

1/ V_{DD} = 10.8 V to 16.5 V, unless otherwise specified. $V_{REFA} = V_{REFB}$ = 10 V, voltage at AGND = 0 V, voltage at $I_{OUTA} = I_{OUTB}$ = 0 V.

2/ If not tested, shall be guaranteed to the limits specified in table I herein.

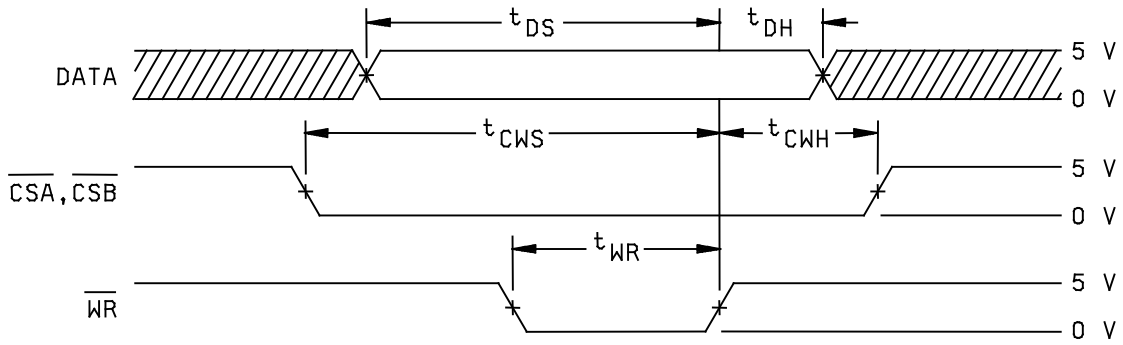
Device type	01, 02, 03	02
Case outline	L	3
Terminal number	Terminal symbol	Terminal symbol
1	AGND	NC
2	I_{OUTA}	AGND
3	R_{FBA}	I_{OUTA}
4	V_{REFA}	R_{FBA}
5	$\overline{CSA}$	V_{REFA}
6	DB_0(LSB)	$\overline{CSA}$
7	DB_1	DB_0(LSB)
8	DB_2	NC
9	DB_3	DB_1
10	DB_4	DB_2
11	DB_5	DB_3
12	DGND	DB_4
13	DB_6	DB_5
14	DB_7	DGND
15	DB_8	NC
16	DB_9	DB_6
17	DB_{10}	DB_7
18	DB_{11}(MSB)	DB_8
19	$\overline{WR}$	DB_9
20	$\overline{CSB}$	DB_{10}
21	V_{DD}	DB_{11}(MSB)
22	V_{REFB}	NC
23	R_{FBB}	$\overline{WR}$
24	I_{OUTB}	$\overline{CSB}$
25	------	V_{DD}
26	------	V_{REFB}
27	------	R_{FBB}
28	------	I_{OUTB}

FIGURE 1. Terminal connections.

$\overline{CSA}$	$\overline{CSB}$	$\overline{WR}$	Function
X	X	1	No data transfer
1	1	X	No data transfer
		0	A rising edge on $\overline{CSA}$ or $\overline{CSB}$ loads data to the respective DAC from data bus
0	1		DACA register loaded from data bus
1	0		DACB register loaded from data bus
0	0		DACA and DACB register loaded from data bus

0 = Logic low level
1 = Logic high level
X = Irrelevant
 = Rising edge triggered

FIGURE 2. Truth table.



Notes

1. All input signal rise and fall times are measured from 10% to 90% of +5.0 V, $t_r = t_f = 20$ ns.
2. Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$

FIGURE 3. Timing diagram.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Subgroup 12 test is used for grading and part selection at +25°C and is not included in PDA calculations.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 12
Group A test requirements (method 5005)	1, 2, 3, 4**, 5**, 6**, 7, 9, 10**, 11**, 12**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
**Subgroups 10 and 11, if not tested, shall be guaranteed to the limits specified in table I herein.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 shall include verification of the truth table.

d. Subgroup 12 test is used for grading and part selection at +25°C.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-09-20

Approved sources of supply for SMD 5962-89657 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8965701LA	1ES66	MX7547SQ/883B
5962-8965702LA	1ES66	MX7547TQ/883B
	24355	AD7547TQ/883B
5962-89657023A	24355	AD7547TE/883B
5962-8965703LA	1ES66	MX7547UQ/883B
	24355	AD7547UQ/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
1ES66	Maxim Integrated 160 Rio Robles San Jose, CA 95134
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland