REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Page 11: Correction to terminal connections. Editorial changes throughout.	88-05-11	M. A. Frye
B	Add one vendor, CAGE 54186 for devices 01, 02, and 03. Make changes to 1.3 and table I. Editorial changes throughout.	89-06-23	Wm. J. Johnson
C	Update drawing to current requirements. – drw	03-12-15	Raymond Monnin
D	Redrawn. Update paragraphs to MIL-PRF-38535 requirements. - drw	15-12-10	Charles F. Saffle

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																				
SHEET																				
REV	D																			
SHEET	15																			
REV STATUS				REV			D	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Marcia B. Kelleher

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Da DiCenzo

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
87-12-02

REVISION LEVEL
D

MICROCIRCUIT, CMOS, DUAL, 8-BIT, MULTIPLYING DIGITAL TO ANALOG CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87701**

SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-87701	01	R	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number	Circuit function
01	7528	CMOS dual 8-bit buffered DAC, ±4 LSB's of gain error
02	7528	CMOS dual 8-bit buffered DAC, ±2 LSB's of gain error
03	7528	CMOS dual 8-bit buffered DAC, ±1 LSB's of gain error

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage	+5 V dc to +15 V dc
V_{DD} to AGND	0 V dc, +17 V dc
V_{DD} to DGND	0 V dc, +17 V dc
Digital input voltage to DGND	-0.3 V dc to +15 V dc
V_{RFBA}, V_{RFBB}, to DGND	±25 V dc
V_{REFA}, V_{REFB}, to AGND	±25 V dc
V pin 1 to DGND	-0.3 V dc to V_{DD}
V pin 2, V pin 20 to AGND	-0.3 V dc to +15 V dc
AGND to DGND	-0.3 V dc, V_{DD} + 0.3 V
DGND to AGND	+0.3 V dc
Power dissipation (P_D):	
Up to +75°C	450 mW
Derate above +75°C	6 mW/°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance (θ_{JC})	See MIL-STD-1835
Thermal resistance (θ_{JA})	+120°C

1.4 Recommended operating conditions.

Operating ambient temperature range (T_A)	-55°C to +125°C
Supply voltage range (V_{DD})	+4.75 V dc to +5.25 V dc and +14.25 V dc to +15.75 V dc
V_{REF} DACA = V_{REF} DACB	+10 V dc
OUT DACA = OUT DACB	0 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional diagram and mode selection. The functional diagram and mode selection shall be as specified on figure 2.

3.2.4 Write cycle timing diagram. The write cycle timing diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Resolution	RES	V_{DD} = +5 V	1, 2, 3	All		8	Bits
		V_{DD} = +15 V				8	
Relative accuracy 2/	RA	V_{DD} = +5 V	1, 2, 3	01		±1	LSB
			1	02		±1	
			2, 3			±0.5	
		V_{DD} = +5 V, T_A = +25°C	12			±0.5	
		V_{DD} = +5 V	1	03		±1	
			2, 3			±0.5	
		V_{DD} = +5 V, T_A = +25°C	12			±0.5	
		V_{DD} = +15 V	1, 2, 3	01		±1	
			1	02		±1	
			2, 3			±0.5	
		V_{DD} = +15 V, T_A = +25°C	12			±0.5	
		V_{DD} = +15 V	1	03		±1	
			2, 3			±0.5	
		V_{DD} = +15 V, T_A = +25°C	12			±0.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Gain error 3/	A_E	DAC register loaded with 1111 1111 1111	V_{DD} = +5 V	1	01		±4	LSB
				2, 3			±6	
				1, 2, 3	02		±4	
			V_{DD} = +5 V T_A = +25°C	12			±2	
			V_{DD} = +5 V	1	03		±4	
				2, 3			±3	
			V_{DD} = +5 V T_A = +25°C	12			±1	
			V_{DD} = +15 V	1	01		±4	
				2, 3			±5	
				1	02		±4	
				2, 3			±3	
			V_{DD} = +15 V T_A = +25°C	12			±1	
			V_{DD} = +15 V	1	03		±4	
				2, 3			±1	
			V_{DD} = +15 V T_A = +25°C	12			±1	
Differential nonlinearity	DNL	V_{DD} = +5 V, all grades guaranteed monotonic to 8-bits over operating temperature range		1, 2, 3	All		±1	LSB
		V_{DD} = +15 V, all grades guaranteed monotonic to 8-bits over operating temperature range		1, 2, 3	All		±1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Power supply rejection $\Delta gain/\Delta V_{DD}$	PSRR	ΔV_{DD} = ±5%	V_{DD} = +5 V	1	All		.02	±%/%
				2, 3			.04	
			V_{DD} = +15 V	1	All		.01	
				2, 3			.02	
Output leakage current pin 2	I_{OL}	DAC latches loaded with 0000 0000	V_{DD} = +5 V	1	All		±50	nA
				2, 3			±400	
			V_{DD} = +15 V	1	All		±50	
				2, 3			±200	
Output leakage current pin 20			V_{DD} = +5 V	1	All		±50	
				2, 3			±400	
			V_{DD} = +15 V	1	All		±50	
				2, 3			±200	
Reference input resistance V_{REFA}, V_{REFB}	R_{IN}		V_{DD} = +5 V	1, 2, 3	All	8	15	kΩ
			V_{DD} = +15 V			8	15	
Digital input high voltage	V_{IH}		V_{DD} = +5 V	1, 2, 3	All	2.4		V
			V_{DD} = +15 V			13.5		
Digital input low voltage	V_{IL}		V_{DD} = +5 V	1, 2, 3	All		0.8	V
			V_{DD} = +15 V				1.5	
Digital input current	I_{IN}	V_{IN} = 0 V or V_{DD}	V_{DD} = +5 V	1	All		±1	µA
				2, 3			±10	
			V_{DD} = +15 V	1	All		±1	
				2, 3			±10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Supply current from V_{DD}	I_{DD}	All digital inputs = V_{IL} or V_{IH}	V_{DD} = +5 V	1, 2, 3	All		2	mA
			V_{DD} = +15 V				2	
		All digital inputs = 0 V or V_{DD}	V_{DD} = +5 V	1	All		100	µA
				2, 3			500	
			V_{DD} = +15 V	1			100	
				2, 3			500	
Gain temperature coefficient	ΔAE/Δt	4/	V_{DD} = +5 V	1, 3, 3	All		±70	ppm/°C
			V_{DD} = +15 V				±35	
Feedthrough error V_{REFA} to OUTA	FT_{REFA}	V_{REF} = ±10 V, 100 kHz sinewave, DAC latches loaded with 0000 0000 4/ 5/	V_{DD} = +5 V	4, 5, 6	All		-70	dB
			V_{DD} = +15 V				-70	
Feedthrough error V_{REFB} to OUTB	FT_{REFB}		V_{DD} = +5 V	4, 5, 6	All		-70	
			V_{DD} = +15 V				-70	
Digital input capacitance	C_{IN}	T_A = +25°C DB0-DB7 6/	V_{DD} = +5 V	4	All		10	pF
			V_{DD} = +15 V				20	
		$\overline{WR}$, $\overline{CS}$, $\overline{DACA}$ /DACB T_A = +25°C 6/	V_{DD} = +5 V	4	All		10	
			V_{DD} = +15 V				15	
Output capacitance pin 2	C_{OUTA}	DAC latches loaded with 0000 0000 T_A = +25°C 4/	V_{DD} = +5 V	4	All		50	pF
			V_{DD} = +15 V				50	
Output capacitance pin 20	C_{OUTB}		V_{DD} = +5 V	4	All		50	
			V_{DD} = +15 V				50	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output capacitance pin 2	C_{OUTA}	DAC latches loaded with 1111 1111 $T_A = +25°C$ 4/	V_{DD} = +5 V	4	All		120	pF
			V_{DD} = +15 V				120	
Output capacitance pin 20	C_{OUTB}		V_{DD} = +5 V	4	All		120	
			V_{DD} = +15 V				120	
Chip select to write setup time	t_{CS}	7/	V_{DD} = +5 V	9	All	200		ns
				10, 11		230		
			V_{DD} = +15 V	9	All	60		
				10, 11		80		
Chip select to write hold time	t_{CH}	7/	V_{DD} = +5 V	9	All	20		ns
				10, 11		30		
			V_{DD} = +15 V	9	All	10		
				10, 11		15		
Write pulse width	t_{WR}	$t_{CS} \ge t_{WR}$, 7/ $t_{CH} \ge 0$	V_{DD} = +5 V	9	All	180		ns
				10, 11		200		
			V_{DD} = +15 V	9	All	60		
				10, 11		80		
Data valid to write setup time	t_{DS}	7/	V_{DD} = +5 V	9	All	110		ns
				10, 11		130		
			V_{DD} = +15 V	9	All	50		
				10, 11		70		
Data valid to write hold time	t_{DH}	7/	V_{DD} = +15 V	9, 10, 11	All	10		ns
			V_{DD} = +15 V	9, 10, 11	All	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Data select to write setup time	t_{AS}	7/	V_{DD} = +5 V	9	All	200		ns
				10, 11		230		
			V_{DD} = +15 V	9	All	60		
				10, 11		80		
Data select to write hold time	t_{AH}	7/	V_{DD} = +5 V	9	All	20		ns
				10, 11		30		
			V_{DD} = +15 V	9	All	10		
				10, 11		15		
Reference input resistance match	$\frac{R_{MIN}}{\Delta V_{REF}}$	4/	V_{DD} = +5 V	1, 2, 3	All		±1	%
			V_{DD} = +15 V	1, 2, 3	All		±1	
Channel-to-channel isolation V_{REFA} to OUTB	CH_{ISO}	V_{REFA} = ±10 V, 100 kHz sinewave, V_{REFB} = 0 V 4/	V_{DD} = +5 V	4, 5, 6	All		60	dB
			V_{DD} = +15 V	4, 5, 6	All		60	
Channel-to-channel isolation V_{REFB} to OUTA	CH_{ISO}	V_{REFB} = ±10 V, 100 kHz sinewave, V_{REFA} = 0 V 4/	V_{DD} = +5 V	4, 5, 6	All		60	dB
			V_{DD} = +15 V	4, 5, 6	All		60	
Output current settling time	t_{SL}	4/	V_{DD} = +5 V	9, 10, 11	All		350	ns
			V_{DD} = +15 V	9, 10, 11	All		180	

1/ V_{OUT1} = 0 V; V_{REF} = +10 V, AGND = DGND unless otherwise specified.

2/ See 4.3.1d.

3/ Measured using internal RFBA and RFBB. Gain error is adjustable.

4/ Guaranteed if not tested.

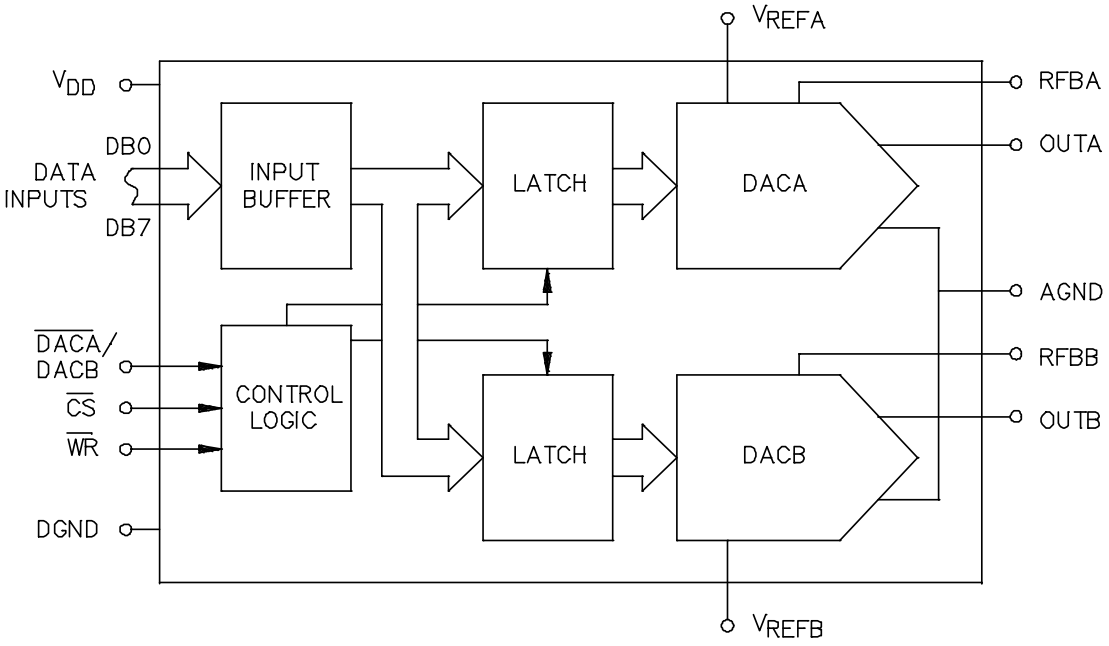
5/ Feedthrough error can be reduced by connecting the metal lid to ground.

6/ See 4.3.1c.

7/ Timing in accordance with figure 3.

Device type	All
Case outline	2 and R
Terminal number	Terminal symbol
1	AGND
2	OUTA
3	R_{FBA}
4	V_{REFA}
5	DGND
6	$\overline{DACA}$ /DACB
7	(MSB) DB7
8	DB6
9	DB5
10	DB4
11	DB3
12	DB2
13	DB1
14	DB0 (LSB)
15	$\overline{CS}$
16	$\overline{WR}$
17	V_{DD}
18	V_{REFB}
19	R_{FBB}
20	OUTB

FIGURE 1. Terminal connections.

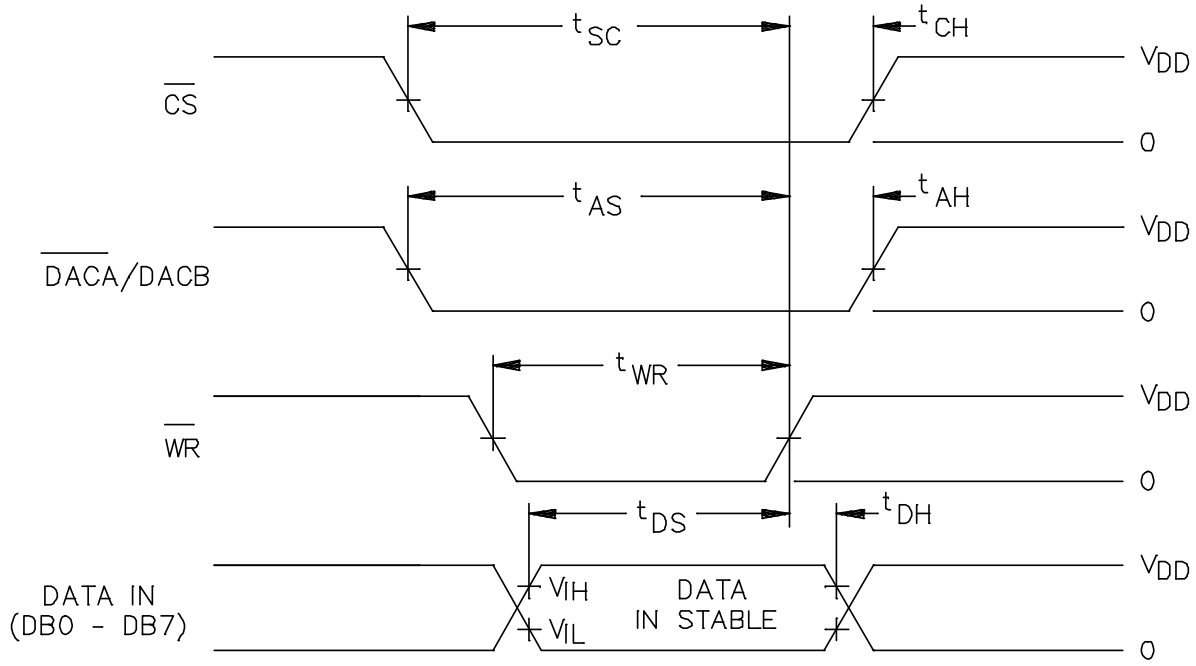


Mode selection table

$\overline{\text{DACA}}$ /DACB	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DACA	DACB
L	L	L	Write	Hold
H	L	L	Hold	Write
X	H	X	Hold	Hold
X	X	H	Hold	Hold

L = Low state
H = High state
X = Don't care

FIGURE 2. Functional diagram and mode selection.



NOTES:

1. All input signal rise and fall times
   Measured from 10% to 90% of V_{PP}.
   V_{PP} = +5 V, $t_r = t_f$ = 20 ns;
   V_{PP} = +15 V, $t_r = t_f$ = 40 ns.

2. Timing measurement reference level $\frac{V_{IH} + V_{IL}}{2}$.

FIGURE 3. Write cycle timing diagram.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. Optional subgroup 12 is used for grading and part selection at +25°C, it is not included in PDA.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 12
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 9, 10**, 11**, 12
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Optional subgroup 12 is used for grading and part selection at +25°C.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 15-12-10

Approved sources of supply for SMD 5962-87701 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-87701012A	3/	AD7528SE/883B
	3/	MP7528SL/883
	3/	PM7528BRC/883B
5962-8770101RA	24335	AD7528SQ/883B
	1ES66	MX7528SQ/883B
	3/	MP7528SD/883
	3/	PM7528BR/883B
5962-87701022A	24335	AD7528TE/883B
	3/	MP7528TL/883
	3/	PM7528BRC/883B
5962-8770102RA	24335	AD7528TQ/883B
	1ES66	MX7528TQ/883B
	3/	MP7528TD/883
	3/	PM7528BR/883B
5962-87701032A	24335	AD7528UE/883B
	3/	MP7528UL/883
	3/	PM7528ARC/883B
5962-8770103RA	24335	AD7528UQ/883B
	1ES66	MX7528UQ/883B
	3/	MP7528UD/883
	3/	PM7528AR/883B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Rt 1 Industrial Park PO Box 9106 Norwood, MA 02062 Point of contact: Raheen Business Park Limerick, Ireland
1ES66	Maxim Integrated 160 Rio Robles San Jose, CA 95134