Application Report
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# Adjustable/Variable Clock Timer For the bq24030/2/5 Li-Ion One-Cell Battery Chargers

PMP Portable Power

**ABSTRACT**

The bq2403x Battery Charger and Dynamic Power Path Management (DPPM) IC is a highly integrated IC which minimizes the required wall adapter size by reducing the battery charging current during peak current demands by the system. Typically a 5-hour charge timer is used to limit the charge time on the battery as a safety feature. Because the charging current can be reduced at any time for any duration, the timer could expire before the battery fully charges and enter a fault mode. A special feature was added to slow the clock frequency of the timer by the amount proportional to the reduction in charge current, except when the reduction is due to voltage regulation, thus extending the safety timer as needed to finish the charge. Of the two main ways to reduce the charge current and slow the timer, the most common way is to enter DPPM mode due to a limited source current; the second, less common way is going into thermal regulation.

## 1 Potential Issues

All the timed specifications in the data sheet are affected by the change in the safety timer clock. This is the only internal clock, and slowing this affects any timed function. Typically, extending the short timed events (10 μs to 100 ms) by a factor of 2 to 3, is not critical to safe operation and can be ignored. The TMR pin permits a designer to adjust these times over a range of 3x to 4x. If a specific timed parameter is an issue, some solutions are available.

## 2 Areas That May Be Affected

The clock is used for four events: (1) the safety timer, (2) deglitch – termination and refresh, (3) break before make when switching input sources, and (4) USB boot up. The USB boot-up time is typically extended because the input current is limited to 100 mA and the load (system plus programmed charge current) typically exceeds this limit; the IC then enters DPPM mode. The time duration for the *break before make* ac-to-USB or USB-to-ac power transition, by toggling PSEL, can be extended if the system output voltage drops to the DPPM threshold. The deglitch times during voltage regulation and refresh are not affected.

## 3 How much can the timed duration change (based on a nominal $R_{TMR}$ resistance of 50 kΩ)?

The USB boot-up time is typically set to 150 ms (with $R_{TMR}$ = 50 kΩ), if DPPM is not active, and is extended to ~275 ms if DPPM is active. The make-before-break duration for switching between ac to USB or USB to ac, when using the PSEL pin, typically increases from 50 μs to 100 μs, if in DPPM mode.

## 4 How to determine how much the time is adjusted (delayed)?

The time duration can be estimated by monitoring the voltage on the timer pin. When not in DPPM mode, the voltage on the TMR pin is 2.5 V. The time changes proportionally (1.25 V would be a clock frequency at half normal speed) to the percent change in the TMR voltage between 2.5 V and 0.8 V, where it is clamped and then becomes nonlinear below 0.8 V.

Figure 1 shows the USB boot-up time while in DPPM, with the dynamic timer in its linear range, with a 100-mA charge rate and ~30 mA of system load current. The top waveform (CH:3) is the OUT voltage which steps from the battery voltage to the input voltage, when USB is applied. After 22 ms, the charging starts and the output drops and enters DPPM mode at ~4 V (DPPM-out threshold) and the TMR voltage (CH:2 – middle waveform) drops from 2.5 V to 1.96 V for 158 ms. The bottom waveform (CH:1) is the ISET1 voltage and mirrors the voltage on the TMR pin during all charging times except when in the nonlinear TMR region (Viset1< 0.8 V). The total boot-up time in the Figure 1 (100-mA input limit) is 22 ms + 158 ms = 180 ms. The voltage on the TMR pin was reduced from 2.5 V to 1.96 V for 158 ms. This portion of the boot up is typically 122 ms when not in DPPM but was extended by the ratio 2.5 V/1.96 V $\times$ 122 ms = 156 ms. This corresponds well with the measured time of 158 ms. This example is not typical because it requires a low programmed charge level to keep the TMR pin in its linear region. Typically, if DPPM is set below the battery voltage, one gets 144 ms for a boot up ®$_{TMR}$ = 50 kΩ).

Figure 2 shows the USB boot-up mode without DPPM (Vdppm set below the battery voltage). See Table 1 for the setup information. Channel 4 is the voltage on the timer pin and channel 3 is the ISET1 voltage that is an indication of charge current. The AC (CH:1) is applied (USB mode, PSEL=L), the AC, OUT (CH:2) and TMR voltage come up immediately followed 22 ms later by the charge current (CH:3). The charge current pulls the output down near the battery where the 100-mA-limited USB input current is shared between the system and battery for ~122 ms. The part is not in DPPM because the battery voltage is above the DPPM threshold. The end of the boot-up time can be measured by observing when the charging current increases due to more available input current. The boot-up time, without DPPM, is the initial 22 ms + 122 ms of the 100-mA-limited input current = 144 ms.

Similarly, any time adjustment due to DPPM, (frequency change of the clock signal) can be estimated, for 0.8 V < $V_{TMR}$ <2.5 V, by monitoring the percent change in the voltage on the TMR pin.

Figure 3 shows the typical USB boot up, in DPPM with the TMR pin clamped in its nonlinear region. The USB power (CH1) is applied, the OUT voltage steps to ~5.2 V and the TMR voltage (CH:4) steps to 2.5 V for 22 ms. The TMR voltage then drops to 0.8 V for 252 ms. When not in DPPM, the corresponding time (see Figure 2) is 122 ms, which is a factor of 252/122 = 2.06. (Because the TMR voltage is clamped, the time change is not proportional to the TMR voltage change.) Therefore the total USB boot-up time, when the TMR voltage is clamped, is typically 22 ms + 252 ms = 274 ms. This is the typical result if the DPPM threshold is set above the battery voltage. One common way to avoid system reset is stay in low power mode for the first 300 ms when powering up with a USB input. Remember that if a battery is present with a useable amount of energy stored in it, the IC always quickly (typically less than 10 μs) connects the battery to the system when the OUT voltage drops 60 mV below the battery's voltage

## 5 What can be done if the extended time becomes an issue?

Typically, the extended boot-up time and deglitch times during power transfer are not an issue, especially if understood during the design phase and can be accounted for in the design. In the special case where the change in clock frequency (time duration) is critical, the following two solutions are available. The first solution is to disable the DPPM function by setting the $V_{DPPM-OUT}$ threshold below the battery's minimum voltage. This is done by changing the $R_{DPPM}$ resistance, $R_{DPPM}$ = $V_{DPPM-OUT}$/(1.15 $\times$ 100 μA), where $V_{DPPM-OUT}$ is set below the minimum expected battery voltage. If the load exceeds the input current, the OUT voltage drops to the battery's voltage first and enters the battery supplement mode. The timer is not adjusted. Note that this solution can be fixed by changing the $R_{DPPM}$ resistor or implemented *on the fly* by switching in/out a parallel resistor. This works well to keep the USB boot-up time fixed, but has no effect for a thermal regulation case.

The second solution can be used if $V_{DPPM-OUT}$ is to be set above the minimum battery voltage or if the battery is not present and requires the $R_{TMR}$ resistor to be actively adjusted by switching in/out a parallel resistor so that the desired frequency (time duration) is achieved. A lower resistance increases the clock

frequency and shortens the time duration. As noted previously, the frequency changes linearly for voltages between 2.5 V and 0.8 V on the timer pin and is nonlinear for voltages below this range. The formula in the data sheet can be used to calculate the resistance for the linear range. For the nonlinear case, the value has to be determined empirically on the laboratory bench. This method works for either the DPPM or thermal regulation case.

Note that boot-up is disabled if the PSEL pin is pulled high (connected to the AC pin) and the adapter powers the AC pin.

## 6 What is the typical time base when not in DPPM?

Note that all time durations in the data sheet specification are based on using a 50-kΩ TMR resistor, which sets the internal clock timer frequency to ~12.8 kHz. The time durations are produced by clocking counters set to a fixed value, and once the value is reached, the action is implemented. The shortest timed event is one-half of a clock frequency and the longest is the safety timer set typically to t(safety) = 0.36 s/Ω× 50 kΩ = 18000 seconds or 5 hours.

All other specified timed events are a function of this time; so, a 45-kΩ resistor decreases all the data-sheet-listed times by 10% (increase the clock frequency by 10%). Changing the clock frequency, at any time, instantly changes how fast the counter times out. Using this information, one can modify the $R_{TMR}$ resistance by switching in or out a parallel resistance to change the specified times.

Another approach is to add more system capacitance; so, dropping into DPPM mode is less likely during transients. It is recommended that, as a minimum, enough system capacitance is provided so the output is held above its critical voltage for 100 µs. This is only necessary when power transfer takes place with a depleted or missing battery; otherwise, the battery supplement mode would activate and support the system.

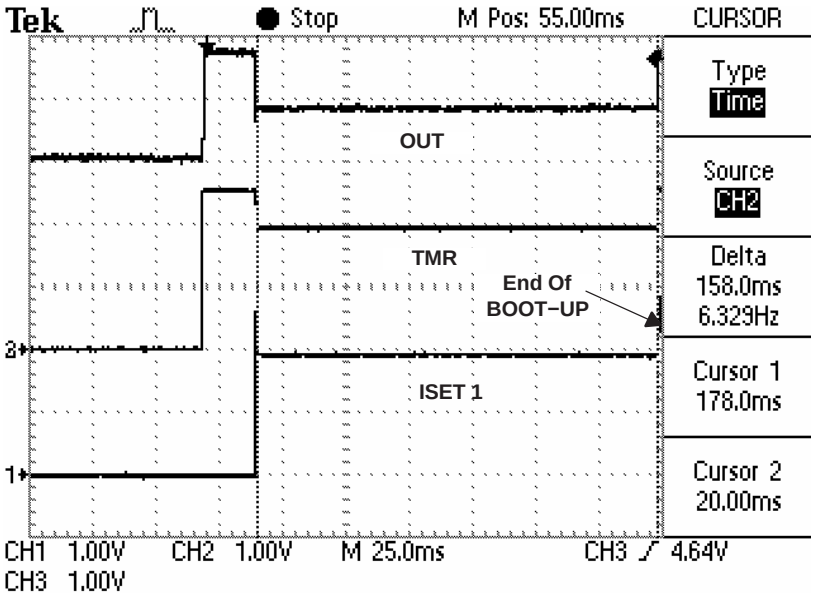


**Figure 1. USB Boot-Up With DPPM Set Above Battery Voltage – TMR Adjusted (in Linear Region)**

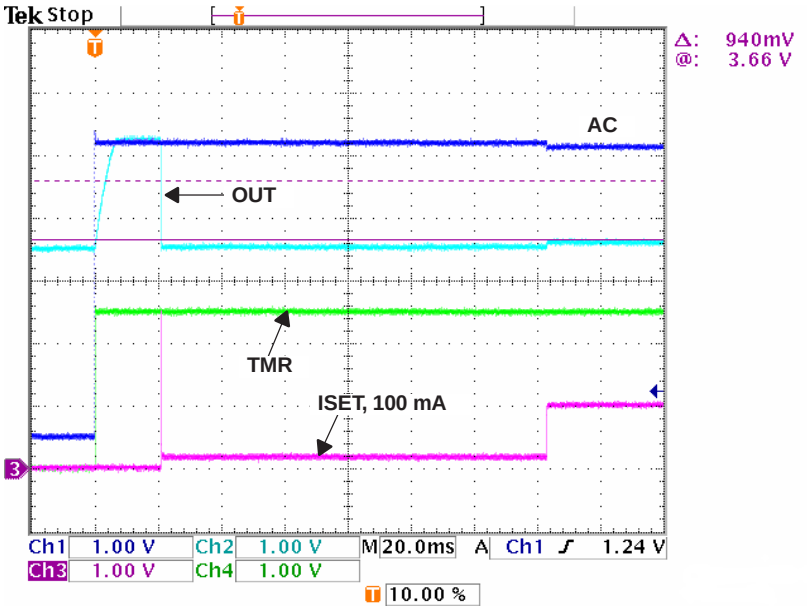


**Figure 2. USB Boot-Up With DPPM Disabled – TMR Not Adjusted**

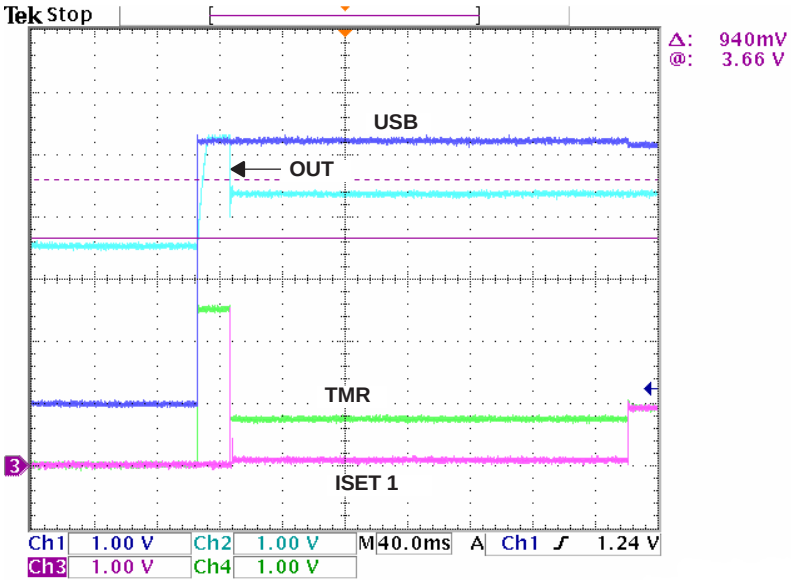


**Figure 3. USB Boot-Up With DPPM Set Above Battery Voltage – TMR Adjust Clamped**

**Table 1. Setup Information for USB Boot Up**

| Plot | Description | Action | CH1 | CH2 | CH3 | CH4 | Setup |
|---|---|---|---|---|---|---|---|
| Fig. 1 | USB boot up, TMR in Linear Region | Applied USB, in DPPM | ISET1 | TMR | OUT | | AC0VDC; USB5VDC; OUT10µF+160 Ω; BAT3.4VDC; DPPM3.65k10nFcap; PSEL-L; TMR50k; bq24035 EVM; |
| Fig. 2 | USB boot up (AC), Vtmr=2.5V | Applied AC, not in DPPM | AC | OUT | ISET1 | TMR | AC5VDC; USB0VDC; OUT100µF+60 Ω; BAT3.5VDC; DPPM28.4k10nFcap; PSEL-L;TMR50k; bq24035 EVM; |
| Fig. 3 | USB boot up (USB), TMR clamped | Applied USB, goes into DPPM | USB | OUT | ISET1 | TMR | AC0VDC; USB5VDC; OUT100µF+60 Ω; BAT3.5VDC; DPPM3.75k10nFcap; PSEL-L;TMR50k; bq24035 EVM; |

## 7 What are the differences between boot-up with and without DPPM?

Figure 1 shows USB boot-up (PSEL=L) in DPPM mode with a slight reduction in charger current, ~24% reduction on the ISET1 pin. The TMR pin's voltage reduces by ~24% from 2.5 V to 1.9 V, and the time duration during the TMR adjust is ~160 ms. If the timer were not adjusted, it would be 76% as long or 121.6 ms.

Figure 2 shows USB boot-up where the DPPM is disabled and the TMR pin stays constant. The duration during the 100-mA source is ~122 ms. Figure 1 and Figure 2 indicate a linear relationship between the time change and voltage change on the TMR pin.

Figure 3 shows USB boot-up in DPPM mode with a large enough load such that the TMR pin is clamped internal to the IC. The 100-mA time duration is ~255 ms (255/122 = 2.09 times as long as without the DPPM). There is not a linear relationship (2.5/2.09 = 1.19 which does not equal 0.8 V) and has to be characterized with the system. At the time of this application report, no adjusted USB time (100-mA period) has been observed that was longer than 287 ms. Therefore, the timer can only slow down ~287/122 = 2.35 times as long, no matter how low the charge current is reduced.

## 8 Conclusion

The benefits of the dynamic clock, while in DPPM, to adjust the clock frequency proportion to the reduction in charging current, is useful in keeping the safety timer set to a meaningful time duration. Changing the clock frequency typically does not cause any issues because timed events, other than the safety timer, happen so infrequently. The USB boot-up and PSEL-initiated power transfers (not usually done) put the IC into DPPM mode, thereby extending the boot-up or power transfer times. Typically, the increase in time is not an issue, especially if known about in the design phase, and can be easily solved if it is. Planning for a 300-ms USB boot up (keep system in low power mode for 300 ms) or a 100-µs power transfer (enough system capacitance to run system for 100 µs) is one easy solution. If no precautions are taken, the worst case is that the output drops down to the battery's voltage and goes into battery supplement mode (assuming the battery is present and has useable energy). Disabling the DPPM feature, during these two events, or applying a lower value resistor to the TMR pin, during the events, are two ways to counter the change in the clock frequency. No cases are known where the adjustable clock frequency compromises safety.

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