3.3-V to 12-V High-Efficiency Ceramic Only Non-Synchronous Boost Converter

Sophie Chen *Systems Power*

ABSTRACT

This reference design describes the functionality of the controller in more detail. This design explains the procedures of a non-synchronous boost converter from 3.3 V to 12.0 V with TPS43000 PWM controller.

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1 Introduction

The TPS43000 is a high-frequency, voltage-mode, synchronous PWM controller that can be flexibly used in buck, boost, buck-boost, and SEPIC topologies. This full-featured controller is designed to drive a pair of external MOSFETs (N/P) and can be used with a wide range of output voltages and power level. It can be widely used in networking equipment, servers, PDAs, cellular phones, and telecommunication applications.

A schematic of this board is shown in Figure 1. Recommended parts list is provided in Table 1. The layout of the PCB board is shown in Figure 7.

The specification for this board is as follows:

- V_{IN} = 3.3 V ±10%
- V_{OUT} = 12 V
- I_{OUT} = 0.2 to 1.5 A, nominal current is 1 A and no PFM.
- Ripple = 1.5%
- Efficiency at nominal load > 90%

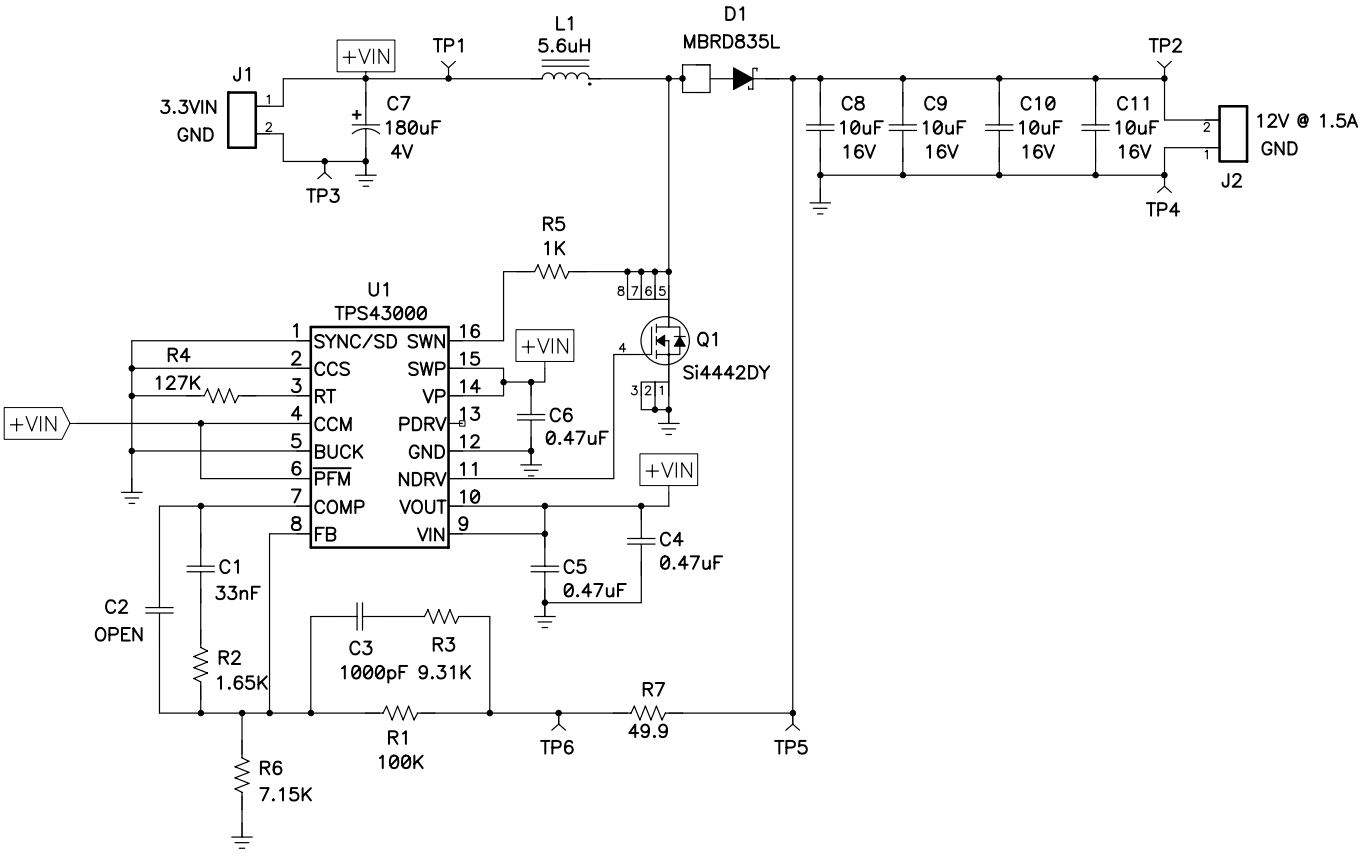


Figure 1. Schematic of PMP145

2 Design Procedure

2.1 Frequency Setting

The TPS43000 can operate either in constant frequency, or in an automatic PFM mode. In the automatic PFM mode, the controller goes to sleep when the inductor current goes discontinuous, and wakes up when the output voltage has fallen by 2%. Please refer to the slus489 datasheet for more detail. The PFM mode is not used in this application. The converter operates at fixed 300 kHz.

A resistor R4, which is connected from RT pin to ground, programs the oscillator frequency. The approximate operating frequency is calculated in equation (1).

$$f\,(MHz) = \frac{38}{R4(k\Omega)} \tag{1}$$

R4 = 127 kΩ is chosen for 300 kHz operation.

2.2 Inductance Value

The inductance value is calculated in equation (2).

$$L_{MIN} = \frac{V_{OUT} \times D \times (1 - D)^2}{f \times 2 \times I_{OUT(\min)}} \tag{2}$$

I_{RIPPLE} is the ripple current flowing through the inductor, which affects the output voltage ripple and core losses. Based on 20% current ripple and 300 kHz, the inductance value is calculated as 5.5 µH and a 5.6-µH inductor is used.

2.3 Input and Output Capacitors

The output capacitance and the ESR needed is calculated in equations (3) and (4).

$$C_{OUTPUT(\min)} = \frac{I_{OUT(\max)} \times D_{MAX}}{f \times V_{RIPPLE}} \tag{3}$$

$$ESR_{OUT} = \frac{V_{RIPPLE}}{\frac{I_{OUT(\max)}}{1 - D_{MAX}} + \frac{I_{IN(ripple)}}{2}} \tag{4}$$

With 1% output voltage ripple, the capacitance needed is at least 31 µF and the ESR should be less than 17 mΩ. Four 10-µF/16-V ceramic capacitors are used.

The input capacitance is shown in equation (5). The calculated value is about 78-µF and a 180-µF low-ESR SP capacitor is used.

$$C_{IN(\min)} = I_{IN(ripple)} \times D_{MAX} \times \frac{T_S}{V_{IN(ripple)}} \tag{5}$$

2.4 Compensation Design

For the boost converter, there is a right-half-plane (RHP) zero, which moves with the operating conditions. The phase starts to drop off a decade before this zero, limiting the system's bandwidth. In this circuit, the RHP zero is around 17.2 kHz. The L-C frequency of the power stage, f_C, is around 2.9 kHz and the ESR zero is around 1.6 MHz, as shown in Figure 2. The overall crossover frequency, f_{0db}, is chosen at 5 kHz for reasonable transient response and stability. R1 to R3 and C1 to C3 form a Type III compensator network. Both zeros (f_{Z1} and f_{Z2}) from the compensator are set at 0.5 f_C and f_C to compensate the phase delay caused by RHP zero. Only one pole, (f_{p1}) is set up at the RHP zero. C2, related to the second pole, is open because the ESR zero is as high as 1.6 MHz. The frequency of poles and zeros are defined by the following equations:

$$f_{Z1} = \frac{1}{2 \times \pi \times R2 \times C1}; \quad f_{Z2} \approx \frac{1}{2 \times \pi \times R1 \times C3}, \quad \textit{assuming } R1 \gg R3 \tag{6}$$

$$f_{P1} = \frac{1}{2 \times \pi \times R3 \times C3}; \quad f_{P2} \approx \frac{1}{2 \times \pi \times R2 \times C1}, \quad \textit{assuming } C1 \gg C2 \tag{7}$$

The compensator values are shown below:

C1 = 33 nF, C2: open, C3 = 1000 pF, R1 = 100 kΩ, R2 = 1.65 kΩ; R3 = 9.31 kΩ.

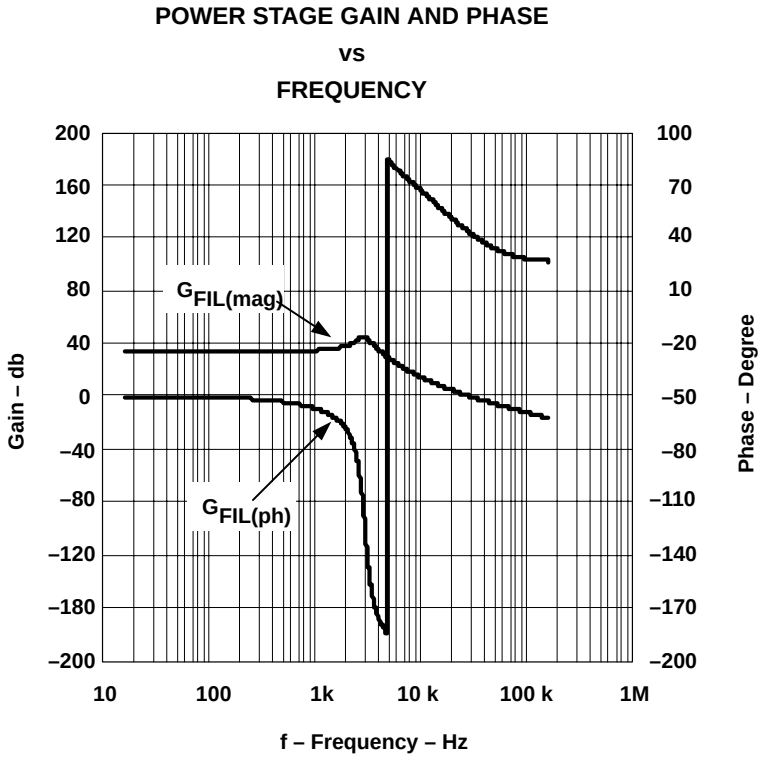


Figure 2.

2.5 MOSFETs and Diode

Si4442DY ($R_{DS(on)}$ = 7.5 mΩ) is chosen. MBRD835L is used for the rectify diode.

2.6 Voltage Sense Resistor

R1 and R6 operate as output voltage divider. The internal reference voltage is 0.8 V. The relationship between the output voltage and divider is shown in equation (8).

$$\frac{V_{REF}}{R6} = \frac{V_{OUT}}{R1 + R6} \tag{8}$$

With 100-kΩ R1 and 12.0-V output regulation, R6 is calculated as 7.15 kΩ.

3 Test Results

3.1 Efficiency Curves

The tested efficiency at different loads and input voltages are shown in Figure 3. The maximum efficiency is as high as 93.3% at 0.5-A output.

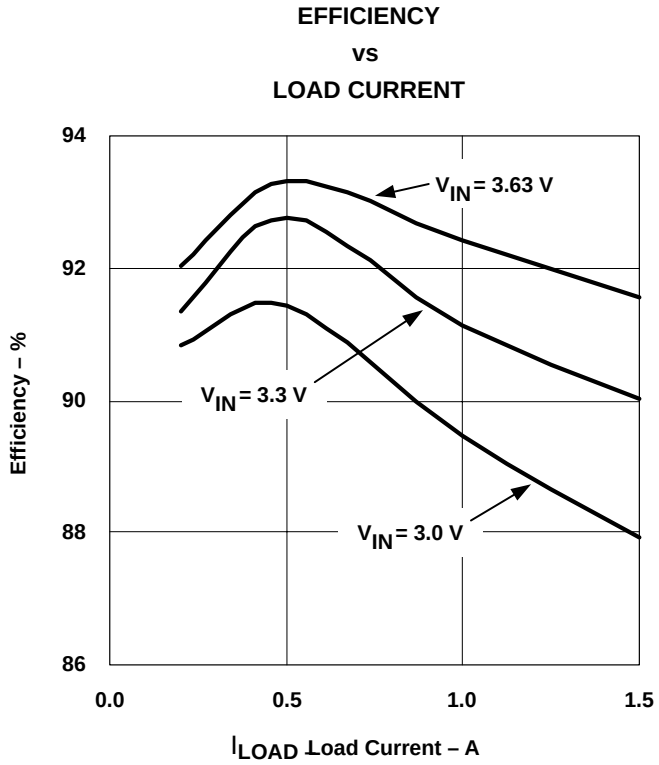
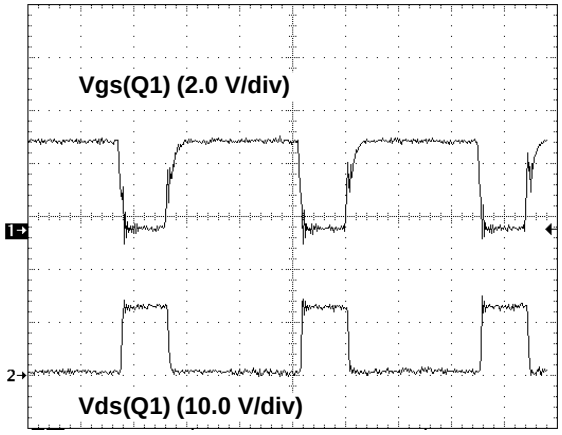


Figure 3.

3.2 Typical Operation Waveform

Typical operation waveform is shown in Figure 4 with V_{IN} = 3.3 V, I_{OUT} = 1.0 A.

TYPICAL OPERATION



t – Time – 1 μ**s/div**

Figure 4.

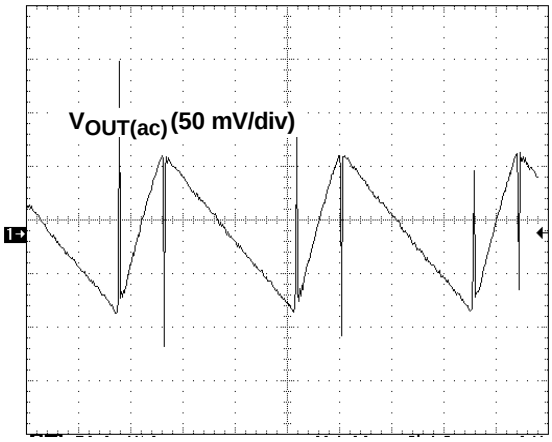
Ch1: gate-source voltage of Q1; Ch2: drain-source voltage waveform of Q1.

3.3 Transient Response and Output Ripple Voltage

The output ripple is about 140 mV peak-to-peak at 1.5-A output.

When the load changes from 1.0 A to 1.2 A, the overshooting voltage is about 200 mV.

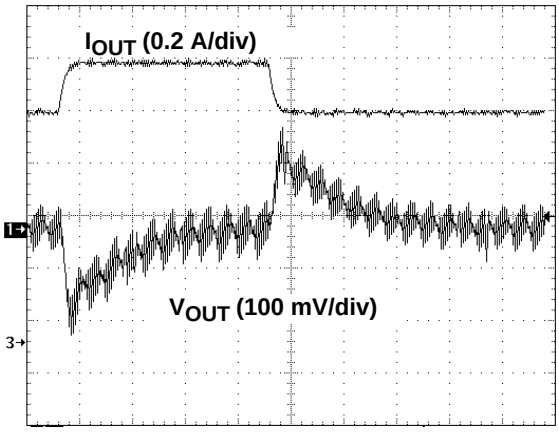
OUTPUT RIPPLE



t – Time – 1 μ**s/div**

Figure 5.

TRANSIENT RESPONSE



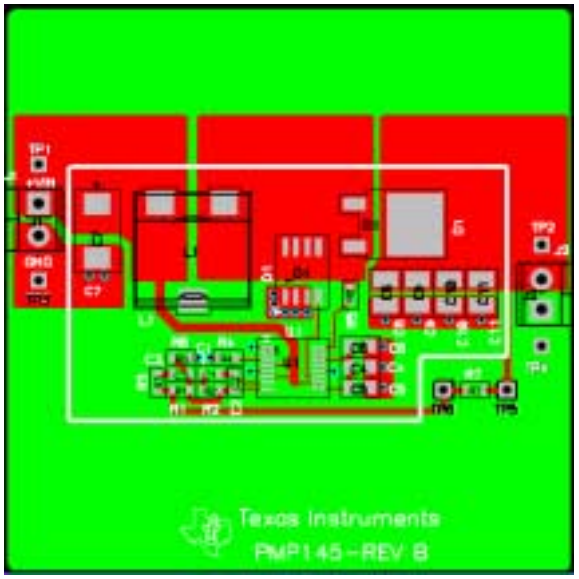
t – Time – 200 μ**s/div**

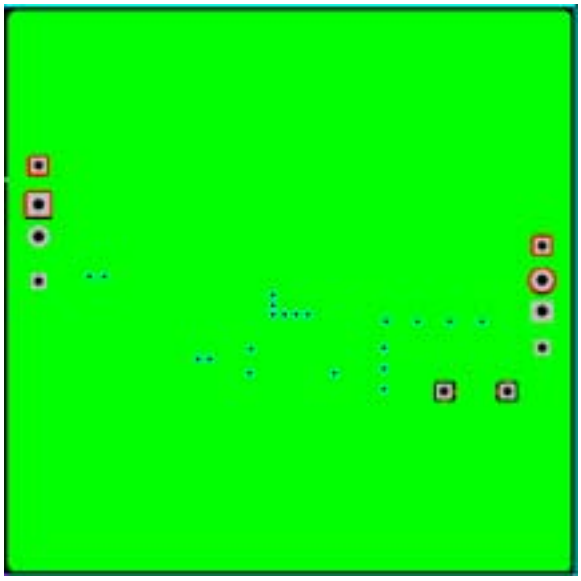
Figure 6.

4 PCB Layout

Figure 7 shows the PCB layout. All the components are on the top side of the board. The bottom side of the board is the ground plane. The PWB is made large to dissipate the losses.

Top View





Bottom View

Figure 7. PCB Layout

5 List of Material

Table 1 lists the board components and their values, which can be modified to meet the application requirements.

Table 1. List of Materials

Size	Reference	Qty	Description	Manufacturer	Part Number
Capacitor	C1	1	Ceramic, 33 nF, 25 V, X7R, 10%, 603	Murata	GRM188R71E333K
	C2	1	Ceramic, open, 50 V, COG, 5%, 603	Murata	GRM1885C1HxxxJ
	C3	1	Ceramic, 1000 pF, 50 V, X7R, 10%, 603	Murata	GRM188R71H102K
	C4,C5,C6	3	Ceramic, 0.47 μF, 25 V, X7R, 10%, 805	Murata	GRM21BR71E474K
	C7	1	180 μF, 4.0 V, 18 mΩ, 20%, 7343 (D)	Panasonic	EEFUE0G181R
	C8,C9,C10,C11	4	Ceramic, 10 μF, 16 V, 10%, 1210	Murata	GRM32ER61C106K
Diode	D1	1	Schottky, 8 A, 35 V, DPAK	ON Semiconductor	MBRD835L
Terminal Block	J1,J2	2	2-pin, 6 A, 3.5 mm, 0.27 x 0.25””	OST	ED1514
Inductor	L1	1	SMT, 5.6 μH, 8.8 A, 11.4 mΩ, 12.9 mm sq	Sumida	CEP125–5R6
Resistor	R1	1	Chip, 100 kΩ, 1/16 W, 1%, 603	Std	Std
	R2	1	Chip, 1.65 kΩ, 1/16 W, 1%, 603	Std	Std
	R3	1	Chip, 9.31 kΩ, 1/16 W, 1%, 603	Std	Std
	R4	1	Chip, 127 kΩ, 1/16 W, 1%, 603	Std	Std
	R5	1	Chip, 1 kΩ, 1/16 W, 1%, 603	Std	Std
	R6	1	Chip, 7.15 kΩ, 1/16 W, 1%, 603	Std	Std
	R7	1	Chip, 49.9 Ω, 1/16 W, 1%, 603	Std	Std
MOSFET	Q1	1	N-channel, 30 V, 17 A, 7.5 mΩ, SO–8	Siliconix	Si4442DY
IC	U1	1	Multi-topology high-frequency, PWM controller, TSSOP–16	Texas Instruments	TPS43000PW
Test Point	TP1,TP2,TP3, TP4,TP5,TP6	6	Black, 1 mm, 0.038”	Farnell	240–333
	N/A	1	Printed circuit board, FR4, 0.032, SMOBC	any	PMP145

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Texas Instruments
Post Office Box 655303
Dallas, Texas 75265