Application Report
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PRU-ICSS Migration Guide: AM335x to AM437x

Catalog Processors *Catalog Processors*

ABSTRACT

This migration guide details the Programmable Real-Time Unit (PRU) subsystem hardware differences and outlines software modifications required for porting PRU firmware and ARM® code to AM437x.

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Trademarks

1 Introduction

This document serves as a software migration guide to assist in porting legacy software developed for the programmable real-time unit subsystem and industrial communication subsystem (PRU-ICSS) on AM335x to AM437x platforms.

For more details about the PRU-ICSS on each device, see the *PRU-ICSS* chapter in the *AM335x and AMIC110 Sitara™ Processors Technical Reference Manual* [1] and the *AM437x ARM® Cortex™-A9 Processors Technical Reference Manual* [2].

NOTE: The focus of this document is the PRU subsystem and broad market, non-industrial applications. Some ICSS or industrial specific features may be omitted.

2 AM335x and AM437x Hardware Differences

This section provides an overview of the hardware differences between AM335x and AM437x. Both a high-level overview of the system-on-chip (SoC)-level hardware differences and a detailed overview of the PRU-ICSS hardware differences are included.

2.1 SoC-Level Hardware Differences

AM335x and AM437x devices support different peripherals and features. The SoC memory map, peripheral register map, pinmuxing, ARM interrupt controller events, and eDMA mapping also differ between the devices.

For additional details, see the device-specific data sheets and user's guides available at the device product pages:

- AM335x [3]
- AM437x [4]

2.2 PRU-ICSS Hardware Differences Between AM335x and AM437x

The table here compares the PRU-ICSS hardware between AM335x and AM437x. One primary difference is that AM335x has one instance of the PRU-ICSS, while AM437x has two instances. Note the two instances on AM437x are not identical.

Figure 1 and Figure 2 show a comparison block diagram of the subsystems:

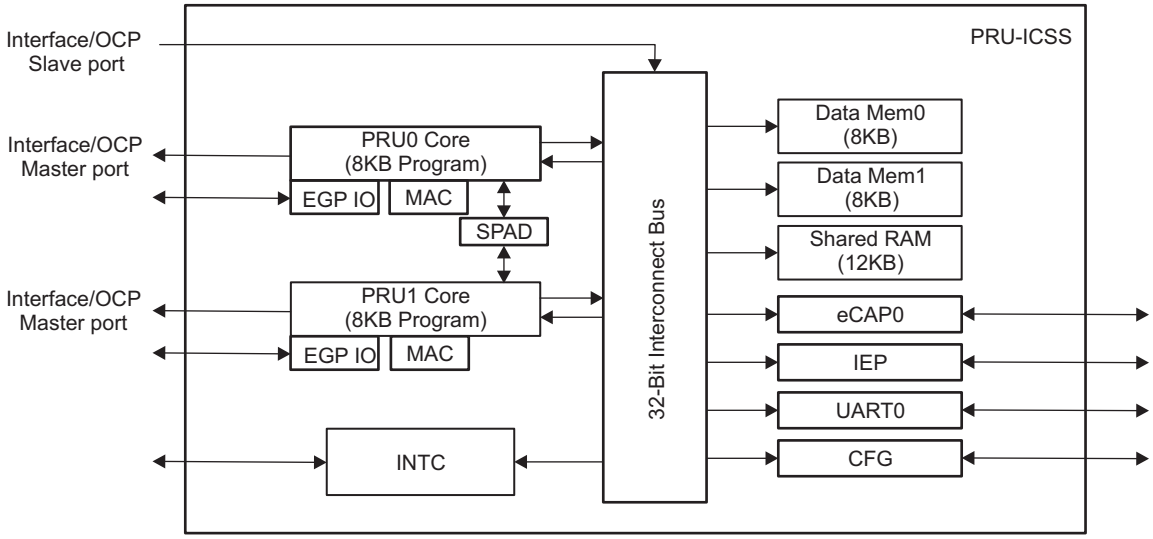

Figure 1. AM335x PRU-ICSS Block Diagram

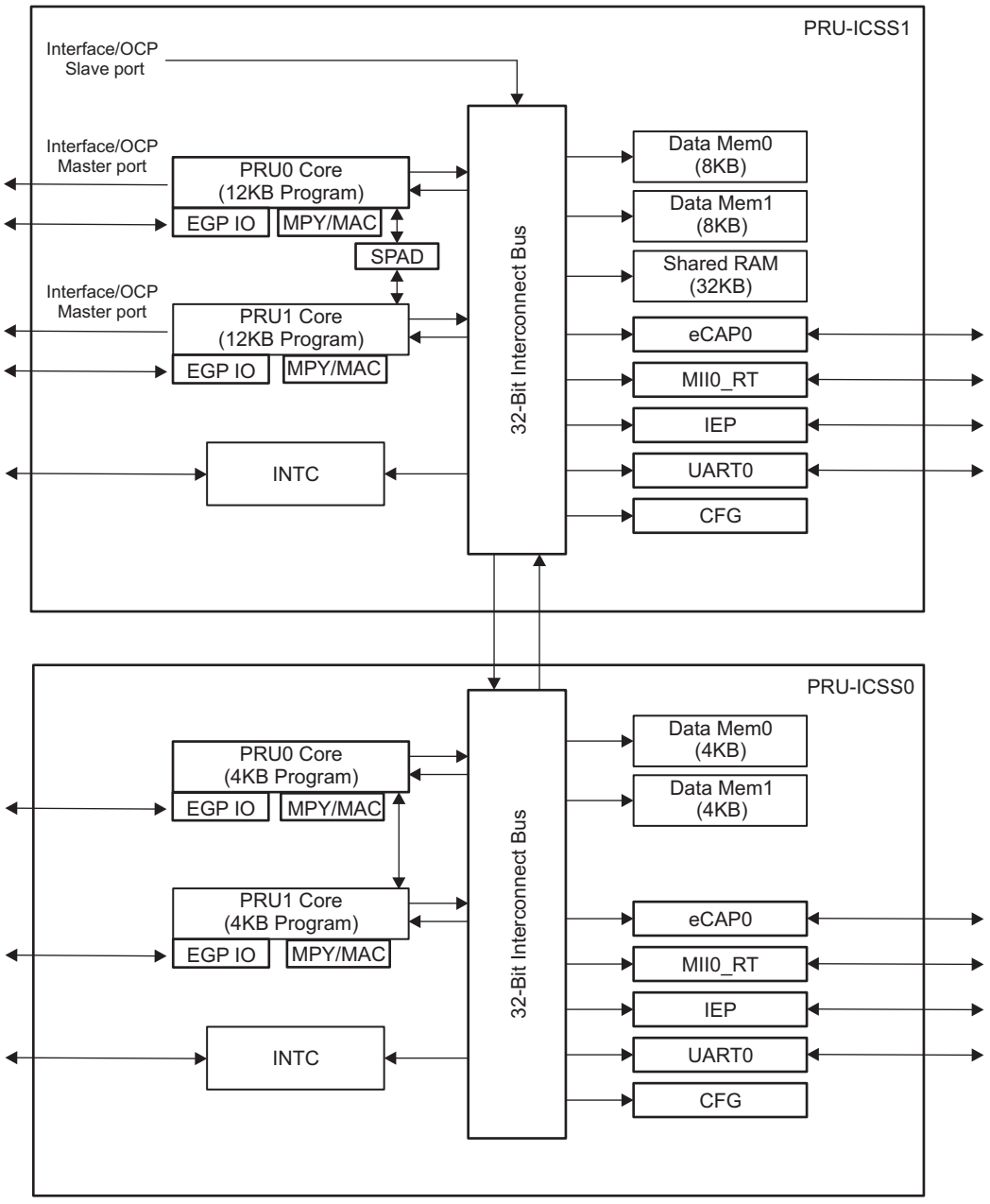

Figure 2. AM437x PRU-ICSS Block diagram

2.2.1 PRU-ICSS Memory Map Comparison

2.2.1.1 PRU-ICSS Memory Map Comparison

The AM437x PRU-ICSS local and global memory maps are backwards compatible with AM335x. However, the PRU-ICSS base address within the SoC memory map differs between devices. Table 1 compares these base addresses, which function as the starting address for the PRU-ICSS global memory map.

Table 1. PRU-ICSS Base Address Comparison for Global Memory Map

	AM335x	AM437x (PRU-ICSS1)
Start Address	0x4A30_0000	0x5440_0000

Note that on AM437x, the base address listed above corresponds to PRU-ICSS1. The PRU-ICSS0 memory map is accessed through the PRU-ICSS1 expansion port (address 0x5444_0000).

2.2.1.2 PRU-ICSS Submodules Register Content and Offsets

The register content and offsets of the following PRU-ICSS submodules are identical on AM335x and AM437x:

- PRU-ICSS INTC
- PRU-ICSS PRU<n> Control
- PRU-ICSS PRU<n> Debug
- PRU-ICSS UART
- PRU-ICSS eCAP

The register content and offsets of the following PRU-ICSS submodules are backwards compatible:

- PRU-ICSS IEP
- PRU-ICSS CFG

2.2.2 Constants Table Differences

The PRU-ICSS constant table entries are backwards compatible.

2.2.3 PRU Module Interface to PRU I/Os Differences

The functionality and structure of R30 and R31 is preserved on AM437x. The supported GPI / GPO modes are backwards compatible. However, the number of PRU I/Os pinned out on each device differs.

2.2.4 Interrupt Controller Differences

The basic structure of the interrupt controller is the same in both devices. The INTC mapping framework of mapping system events to channels to hosts is still the same. Both devices support the same number of total system events (64), channels (16), and hosts (10). However, on AM437, Host 7 within each PRU-ICSS is exported for signaling the other PRU-ICSS (instead of the ARM). On both devices, Host0 and Host1 are connected to the PRU cores and Host2-6, Host8-9 are exported for signaling the ARM and eDMA.

The INTC system events are partially backwards compatible. There are some system events that differ between AM335x and AM437x, as shown in Table 2.

The ARM interrupt numbers mapped to the PRU-ICSS source interrupts have also been updated on AM437x. For these changes, see Table 3.

Table 2. INTC Event Differences

Event	AM335x Function	AM437x Function	
	PRU-ICSS1	PRU-ICSS1	PRU-ICSS0
57	GPIO0	eHRPWM0-2 Trip Zone	eHRPWM3-5 Trip Zone
56	eHRPWM0-2 Trip Zone	PRU-ICSS0 Host Interrupt 7	PRU-ICSS1 Host Interrupt 7
50	CPSW (c0_rx_thresh_pend)	CPSW (c2_rx_thresh_pend)	CPSW (c2_rx_thresh_pend)
49	CPSW (c0_rx_pend)	CPSW (c2_rx_pend)	CPSW (c2_rx_pend)
48	CPSW (c0_tx_pend)	CPSW (c2_tx_pend)	CPSW (c2_tx_pend)
47	CPSW (c0_misc_pend)	CPSW (c2_misc_pend)	CPSW (c2_misc_pend)
46	eHRPWM1	eHRPWM1	eHRPWM4
43	eHRPWM0	eHRPWM0	eHRPWM3
37	eHRPWM2	eHRPWM2	eHRPWM5
34	McASP1 RX	ADC1 (Mag Card)	ADC1 (Mag Card)
33	McASP1 TX	QSPI	QSPI

Table 3. ARM Mapping of Source Interrupt to Event Number Comparison

Source	AM335x Event Number	AM437x Event Number	
	PRU-ICSS1	PRU-ICSS1	PRU-ICSS0
PRU_ICSS<k>_EVTOUT0	20	52	191
PRU_ICSS<k>_EVTOUT1	21	53	192
PRU_ICSS<k>_EVTOUT2	22	54	193
PRU_ICSS<k>_EVTOUT3	23	55	194
PRU_ICSS<k>_EVTOUT4	24	56	195
PRU_ICSS<k>_EVTOUT5	25	-	-
PRU_ICSS<k>_EVTOUT6	26	58	196
PRU_ICSS<k>_EVTOUT7	27	59	197

2.2.5 Peripheral Differences

2.2.5.1 PRU-ICSS UART

The PRU-ICSS UART is identical on AM335x and AM437x.

2.2.5.2 PRU-ICSS eCAP

The PRU-ICSS eCAP is identical on AM335x and AM437x.

2.2.5.3 PRU-ICSS Industrial Ethernet Peripheral (IEP)

The PRU-ICSS IEP is backwards compatible on AM335x and AM437x.

The AM437x IEP Timer supports more compare registers (16 on AM437x vs 8 on AM335x) and adds support for a programmable reset value within the IEP_TMR_CNT_RST register.

2.2.6 Instruction Set and Format Compatibility

The instruction set and format on AM437x is identical with AM335x.

3 Porting AM335x PRU Software to AM437x

The software changes required to port legacy code from AM335x to AM437x are based on the hardware differences between the two devices. This section details the key differences in software and describes how legacy AM335x code can be modified for AM437x PRU-ICSS1. Note additional modifications may be required relating to other SoC differences that are external to the PRU-ICSS. Some of these modifications are discussed in the modifying software for SoC related differences section.

NOTE: The below sections assume that the legacy AM335x software is ported to AM437x PRU-ICSS1. Additional considerations may be required when porting to AM437x PRU-ICSS0.

A checklist of changes required for both legacy PRU firmware and ARM code is provided in Table 4 and Table 5.

Table 4. PRU Firmware Checklist

1	PRU addresses within global memory map
2	PRU-ICSS interrupt system event numbers
3	SoC related changes (for example, peripheral addressing or registers, and so forth)

Table 5. ARM Code Checklist

1	PRU addresses within global memory map
2	PRU-ICSS interrupt system event numbers
3	SoC related changes (for example, peripheral addressing or registers, pinmux configuration, ARM Interrupt Controller, and so forth)

3.1 Updating Global Memory Map References

When porting the legacy software to AM437x PRU-ICSS1, the PRU-ICSS base address needs to be updated in both the PRU firmware and ARM code. Note that most PRU firmware code should use the local memory map to reduce latencies and would not require any modification. Only firmware that accesses the global memory map requires updates.

No change is required for any offsets within the PRU-ICSS global memory map.

3.2 Updating PRU System Events and PRU-ICSS INTC Mapping

The AM335x and AM437x PRU INTC have some system event differences. If the existing application uses one of these system events, the system events will need to be updated both in the PRU firmware code and in the interrupt controller mapping in the ARM code.

If an interrupt used on AM335x is no longer supported on AM437x, one option is to poll or periodically read the peripheral's status register, if it exists. For peripheral details, see the AM437x TRM [2]. Note that there are additional latencies when accessing memories outside the PRU subsystem.

The functionality of the Host interrupt 7 has also changed between AM335x and AM437x. Any system events mapped to Host 7 in AM335x legacy code should be remapped to Host2-6 or Host8-9. This impacts ARM code and could also impact the PRU firmware (i.e. if the PRU configures the INTC).

The ARM interrupt controller has also changed with respect to the interrupt numbers mapped to the PRU-ICSS host interrupts. In the ARM code, the user needs to confirm that IRQs are updated for the new PRU-ICSS event numbers.

3.3 Modifying Software for SoC Related Differences

AM335x and AM437x devices have additional differences at the SoC level that also require changes in both PRU firmware and ARM code. Below is a list of some key differences that require code updates; however, this is not an exhaustive list.

Key differences between the AM335x and AM437x devices require PRU legacy code updates include:

- Global device memory map
  - Start addresses of peripherals and features
  - Base addresses of modules
  - Register addresses and offsets
- Peripherals
  - For additional details, see the device-specific data sheets and user's guides available at the device product pages: link to AM335x and AM437x product folders.
  - Peripherals may have new memory or register maps. The functionality of registers may also change.
- Pinmuxing

4 References

1. *AM335x and AMIC110 Sitara™ Processors Technical Reference Manual*
2. *AM437x ARM® Cortex™-A9 Processors Technical Reference Manual* product page
3. AM3358 product page
4. AM4377 product page

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