Application Report
SPRAC90–June 2017

PRU-ICSS Feature Comparison

Catalog Processors

ABSTRACT

This application report documents the feature differences between the PRU subsystems available on different TI processors.

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Trademarks

1 Introduction

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Table 1. PRU-ICSS Feature Comparison

Features	AM335x	AM437x		AM570x	AM571x	AM572x	K2G
	PRU-ICSS1	PRU-ICSS1	PRU-ICSS0	2x PRU-ICSS (1)	2x PRU-ICSS (1)	2x PRU-ICSS (1)	2x PRU-ICSS (1)
Number of PRU cores	2	2	2	2	2	2	2
Max Frequency	200 MHz	225 MHz (2)	225 MHz (2)	200 MHz	200 MHz	200 MHz	200 MHz
IRAM size (per PRU core)	8 KB	12 KB	4 KB	12 KB	12 KB	12 KB	16 KB
DRAM size (per PRU core)	8 KB	8 KB	4 KB	8 KB	8 KB	8 KB	8 KB
Shared DRAM size	12 KB	32 KB	0 KB	32KB	32KB	32KB	64KB w/ ECC
General Purpose Input (per PRU core)	Direct; or 16-bit parallel capture; or 28-bit shift	Direct; or 16-bit parallel capture; or 28-bit shift; or 3ch EnDat 2.2; or 9ch Sigma Delta	Direct; or 16-bit parallel capture; or 28-bit shift; or 3ch EnDat 2.2; or 9ch Sigma Delta	Direct; or 16-bit parallel capture; or 28-bit shift; or 3ch EnDat 2.2; or 9ch Sigma Delta	Direct; or 16-bit parallel capture; or 28-bit shift; or 3ch EnDat 2.2; or 9ch Sigma Delta	Direct; or 16-bit parallel capture; or 28-bit shift	Direct; or 16-bit parallel capture; or 28-bit shift; or 3ch EnDat 2.2; or 9ch Sigma Delta
General Purpose Output (per PRU core)	Direct; or Shift out	Direct; or Shift out	Direct; or Shift out	Direct; or Shift out	Direct; or Shift out	Direct; or Shift out	Direct; or Shift out
GPI Pins (PRU0, PRU1)	17, 17	13, 0	20, 20	0/21(3), 21/17	0/21(3), 21/21	21, 21	20, 20
GPO Pins (PRU0, PRU1)	16, 16	12, 0	20, 20	0/21(3), 21/17	0/21(3), 21/21	21, 21	20, 20
MPY/MAC	Y	Y	Y	Y	Y	Y	Y
Scratchpad	Y (3 banks)	Y (3 banks)	N	Y (3 banks)	Y (3 banks)	Y (3 banks)	Y (3 banks)
CRC16/32	0	2	2	2	2	2 (4)	2
INTC	1	1	1	1	1	1	1
Peripherals	Y	Y	Y	Y	Y	Y	Y
UART	1	1	1	1 / not pinned out (5)	1	1	1
eCAP	1	1	not pinned out	1 / not pinned out (5)	1	1	1
IEP	1	1	not pinned out	1 / not pinned out (5)	1	1	1
MII_RT	2	2	not pinned out	2	2	2	2
MDIO	1	1	not pinned out	1	1	1	1

(1) The name PRU-ICSS and PRUSS are used interchangeably throughout the AM57xx and K2G documentation to describe the Programmable Real-Time Unit (PRU) and Industrial Communication Subsystem.

(2) The default frequency for AM437x is 200 MHz. However, the max frequency 225 MHz is achievable through display PLL CLKOUT. For DSS limitations when configuring this PLL for frequencies >200 MHz, see the AM437x Sitara Processors Technical Reference Manual.

(3) AM571x and AM570x PRU-ICSS1 does not pin out the PRU0 core GPIs/GPOs. The other AM571x and AM570x PRU cores (PRU-ICSS1 PRU1, PRU-ICSS2 PRU0, PRU-ICSS2 PRU1) each pin out the number of GPIs/GPOs is listed in Table 1.

(4) AM572x SR1.1 does not have CRC16/32. Within the AM57x family, this feature is only available in AM572x SR2.0, AM571x, and AM570x.

(5) AM570x PRU-ICSS2 does not pin out these submodules. However, they are pinned out on the other AM570x subsystem (PRU-ICSS1).

2 References

AM437x Sitara Processors Technical Reference Manual

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