AN-1304 LM5068 -48V Hot Swap Controller

ABSTRACT

This application report explains the function and design of components connected to MOSFET's gate terminal that limit inrush currents during insertion of a module into a live backplane when using the LM5068 without external current sense resistor.

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1 Introduction

The LM5068 is a hot-swap controller that allows a circuit card to be safely inserted or removed from live backplane without having to shutdown the system power. The wide operating input voltage range (from –10V to –90V) is well suited for - 48V power systems. The LM5068 provides a current limited power to turn-on circuit cards thus preventing glitches on the power supply rail and damage to board connectors and components. The under-voltage and over-voltage protection of the LM5068 ensure that the input voltage is stable and within tolerance before applying power to the load.

2 Theory of Operation

The LM5068 is a hot-swap controller used as system supply monitor as well as current limiter. The system monitor function senses the supply voltage for under-voltage and over-voltage conditions and will shutdown the external MOSFET to stop power from flowing to load during these conditions. The current monitor functions to limit inrush current and output overload circuit current to prevent damage to the system.

The LM5068 has three current limit thresholds, at 50mV, 100mV and 200mV, to limit overload circuit current during output short-circuit or other overload conditions using a current sense resistor. From the above current limit thresholds, it is clear that overload current limit threshold of 100mV (IACL, active current limit loop) is twice the circuit breaker (ICB) current limit of 50mV, and the user doesn't always have the flexibility to set his inrush current limit to twice the steady state current limit threshold of 50mV, due to application limitations. This application report describes an alternative approach to overcome these situations without the use of current-sense resistor.

In the application circuit shown in Figure 1, the input power to the module (shown here as load) is controlled by placing an N-channel external MOSFET switch in the power path. Resistors R1,R2 & R3 determine the UV and OV thresholds of the power supply input. Both the controller (LM5068) and the external MOSFET work together to limit the charging current when the board is first plugged into the live backplane. When the power is first applied to VDD, the controller holds the gate of the MOSFET (Q1) to ground. After a programmable debounce delay determined by the timer capacitor CT, an internal 60uA current source begins to charge the MOSFET gate. The capacitor C2 and resistor R4 acts as a feedback network to accurately control the dv/dt and inrush current in the load capacitor CL. The drain voltage fall rate as the MOSFET turns on, is fed back to the gate terminal through R4 and C2, to appropriately control the gate voltage rise time. The MOSFET gate is supplied by a constant current source of 60uA. The desired value of capacitor C2 can be calculated as follows. Refer to the schematic in Figure 2.

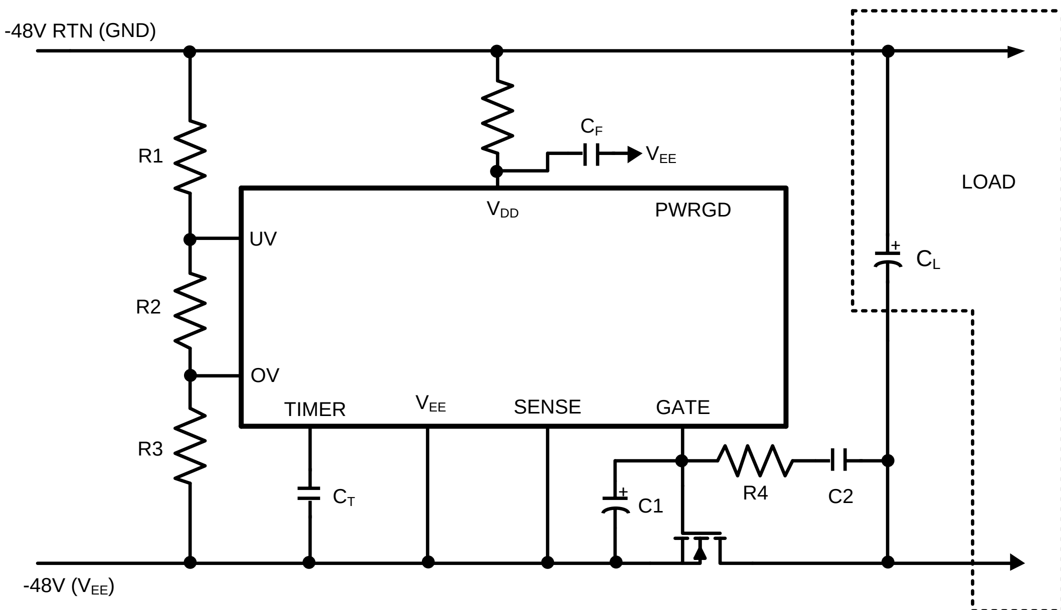

Figure 1. Typical Application Schematic

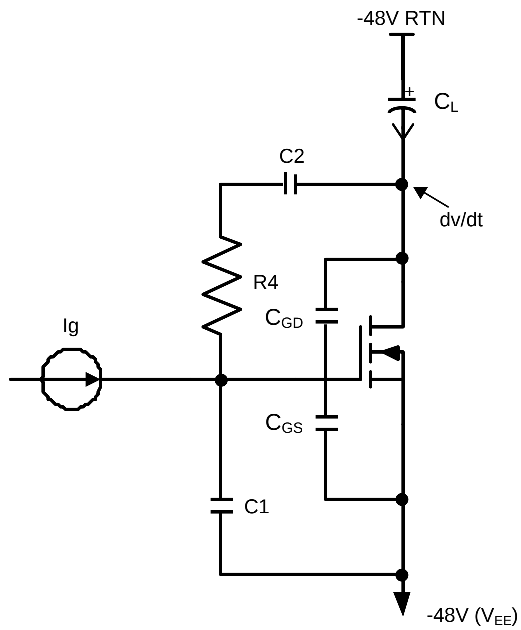

Figure 2. Calculation of Feedback Capacitor C2

The rate of change of drain voltage is given by,

$$\frac{dv}{dt} = \frac{Ig}{(C2 + C_{GD})} = \frac{I_{L(max)}}{C_L} \tag{1}$$

where Ig is the gate current source, and IL(max) is the maximum inrush current that is allowed, and CGD is the MOSFET's gate to drain capacitance.

From equation (1) , C2 can be calculated as

$$C2 + C_{GD} = C_L \text{ x } \frac{Ig}{I_{L(max)}} \tag{2}$$

$$C2 = C_L \text{ x } \frac{Ig}{I_{L(max)}} - C_{GD} \tag{3}$$

R4 is calculated to limit current and to have a maximum drop of less than a volt at 60µA of MOSFET gate current, and to eliminate any kind of glitch at the gate terminal during normal operation or during plugging into the live backplane using R4, C1 filter. Capacitor C1 and R4 prevent Q1 from turning on momentarily when the power pins first make contact. Without C1 and R4, Capacitor C2 would pull up the gate of Q1 to approximately even before the LM5068 powers up and the pull-down of the gate is activated.

$$Vg = \left|V_{EE}\right| \text{x } \frac{C2 + C_{GD}}{C_{GS}} \tag{4}$$

In the above equation, C_{GS}, is the internal gate to source capacitance of the MOSFET. By placing capacitor C1 in parallel with gate to source capacitance of Q1, this issue can be avoided. The value of C1 is calculated as follows.

$$C1 \geq \left[\frac{(V_{IN(max)} - V_{th})}{V_{th}} \text{ x } (C2 + C_{GD})\right] - C_{GS} \tag{5}$$

where Vth is MOSFET's minimum gate threshold voltage and CGD is the gate to drain capacitance of the MOSFET.

3 Conclusion

This application report describes the functionality of LM5068 hot-swap controller as a inrush current limiter and system monitor without using a current sense resistor. It should be understood that without sense resistor some features of LM5068 are disabled, including limiting output overload circuit current and excessive supply currents.

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