

A Step-By-Step Design Approach to TPS2300/01/11/20/21/30/31 Hotswap Controllers

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ABSTRACT

The TPS2300/01/10/11/20/21/30/31 hotswap controllers allow safe board insertion and removal from a live backplane. With the current-sensing resistor (R_{SENSE}) and the current-limit-setting resistor (R_{SET}), the current limit can be set much more easily than other hotswap controllers. This report uses a simple step-by-step design approach to select the essential components and parameters for typical hotswap applications. By following the design procedure demonstrated in this report, the solutions with TPS23xx become simple.

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1 Design Specifications

1.1 Typical Application Diagram

A typical hotswap application diagram using TPS23xx hotswap controllers is illustrated in Figure 1.

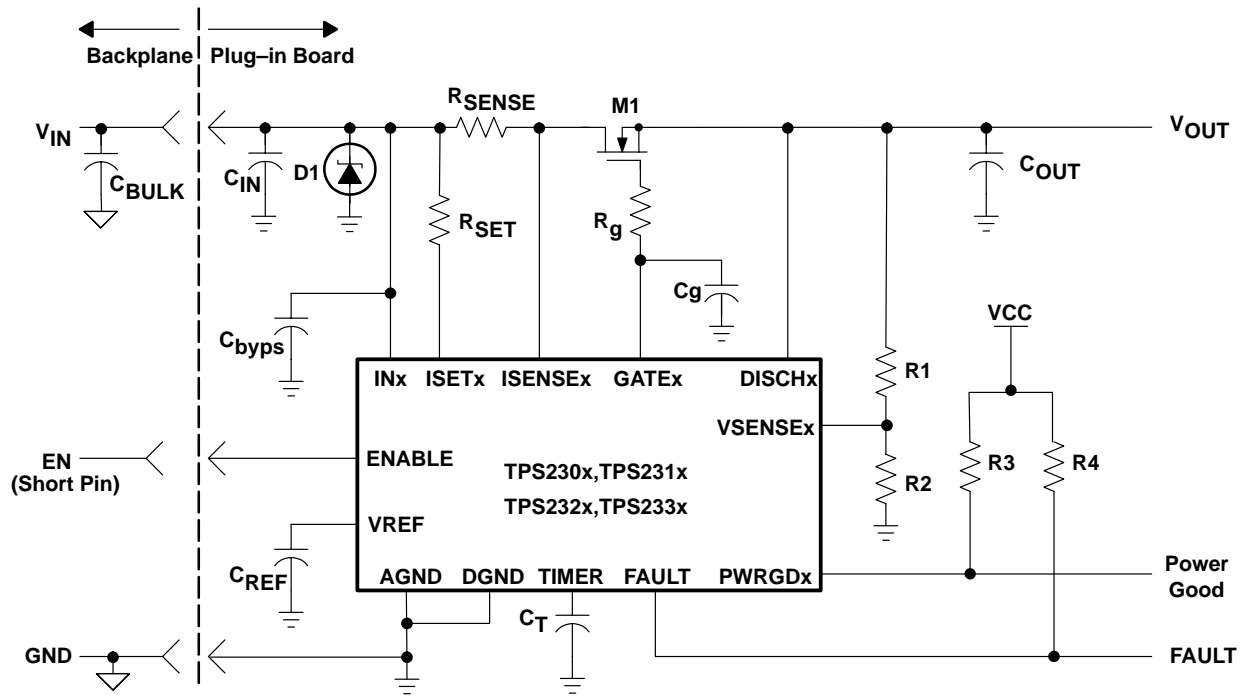


Figure 1. Typical Application Diagram of TPS23xx Hotswap Controllers

Some of the components may not be required depending on applications as explained in this report.

1.2 Design Requirements

To design the hotswap stage correctly, the system requirements provide the important conditions for the design. The most important information about the systems includes:

- Direct load total capacitance of the hotswap stage output, C_{OUT}
- Direct backplane total bulk capacitance, or the total input capacitance on the hotswap stage input, C_{BULK} , required by the system
- Maximum load continuous current, I_{MAX} , specified by the application
- Input supply voltage, V_{IN} , specified by the application
- Pullup voltage source for PWRGD and FAULT outputs, VCC, defined by the application. If the separate supply (VCC) is not available, it can be directly tied to the input or output of the hotswap stage through the pullup resistors (R3 and R4).

2 Step-by-Step Design Approach

2.1 Input Capacitor Considerations

A 0.01 to 0.1- μ F bypass capacitor, C_{byps} , on IN pin is recommended. A 0.1- μ F ceramic capacitor on VREF pin is required due to the operational stability requirement for the internal voltage regulator of the TPS23xx controllers.

The immediate input capacitor C_{IN} of the hotswap stage, is not required because of the large bulk capacitor, C_{BULK} , on the backplane. But it can help to reduce high frequency noise during hotswap events when installed. If installed, the capacitance must be very small compared to the backplane bulk capacitor to minimize the voltage fluctuations during hot plugin and removal. A ratio of 1/1000 or less is recommended for the C_{IN} over the C_{BULK} . If there is no physical board-to-board plugin or removal between the input supply stage (or the backplane shown in the diagram) and the input of TPS23xx, the capacitor has little effect.

2.2 Overvoltage Protection

A 13-V to 14-V Zener diode (D1) is recommended for applications with a 12-V input supply. The diode helps to limit the input voltage spikes under the absolute maximum voltage ratings of the device. For 5-V or less supplies, the Zener diode is not required, but it still helps to protect the device against negative spikes during some abnormal situations, such as a hot short from the supply to ground.

2.3 Current Limit

Since the maximum load current, I_{MAX} , is specified by the application, a current limit can be set accordingly. Considering all potential variations of the components, such as sense resistor (R_{SENSE}), current limit setting resistor (R_{SET}), layout, and TPS23xx circuit breaker, a 25% margin on top of the I_{MAX} is recommended for the current limit. That is:

$$I_{LMT_SET} = 1.25 \times I_{MAX} \quad (1)$$

One of the most important features for TPS23xx devices is to use two resistors (R_{SENSE} and R_{SET}) instead of one resistor to set the current limit threshold. Traditionally, hotswap controllers use a single current sense resistor to set the current limit. The problem is that the calculated sense resistance value might not be available. For example, if the circuit breaker of a controller has a 50-mV threshold and the current limit needs to be 2.9 A, then the sense resistance should be 17.2 m Ω but the closest available resistor is 15 m Ω . If that resistor is used, the sense resistor alone creates a +13% shift on the current limit. For TPS23xx, however, an accurate sense resistance can be arbitrarily chosen first and then calculate the set resistor R_{SET} . Since the R_{SET} is in the range of a few hundred to a few thousand ohms, it is easy to select R_{SET} to be 100% accurate or very close (e.g., within 5%) to the calculated value.

Another benefit is that the voltage drop on R_{SENSE} is flexible for TPS23xx, while it is a fixed value for other hotswap controllers. The voltage drop can be set to be much less than the sense threshold voltage of most traditional hotswap controllers. Therefore, the selection of R_{SENSE} becomes easy.

Although the sense resistor R_{SENSE} can be arbitrarily chosen for TPS23xx, a couple of boundary conditions should be considered so that a good choice can be made. The first limitation is the power loss or the voltage drop on the resistor should be small. A high efficiency of the hot-swap stage is always desired, so that the voltage drop on the R_{SENSE} must be small. If a minimum efficiency requirement, η_{MIN} , is available, the maximum sense resistance is:

$$R_{\text{SENSE}} < \frac{V_{\text{IN}} \times (1 - \eta_{\text{MIN}})}{I_{\text{MAX}}} \quad (2)$$

The other boundary, which sets the lower limit of R_{SENSE} , is the circuit breaker accuracy and the layout factors. If R_{SENSE} is too small, the voltage drop across R_{SENSE} is also very small. Therefore, the trace impedances and sense-resistor contacts may cause a significant variation to total sense resistance. Besides, the circuit breaker comparator can be another factor affecting the accuracy of the current-limit setting due to its input offset. Considering all these factors, a 20-mV drop on the R_{SENSE} should be the absolute minimum, but 40 mV is the recommended minimum for typical applications. So the minimum R_{SENSE} can be calculated by:

$$R_{\text{SENSE}} \geq \frac{40 \text{ mV}}{I_{\text{LMT_SET}}} \quad (3)$$

The R_{SENSE} should be selected so that it is just a little higher than that calculated by equation (3) so the power loss on the sense resistor is minimized. If the results from equations (2) and (3) conflict with each other, then either the efficiency requirement is unrealistically high, or the 40-mV voltage drop limit on R_{SENSE} has to be lowered to meet the application requirements. If the minimum voltage drop limit on R_{SENSE} is reduced, the accuracy of the current limit setting can not be assured.

Once the R_{SENSE} is selected, R_{SET} can be calculated by the following equation.

$$R_{\text{SET}} = \frac{I_{\text{LMT_SET}} \times R_{\text{SENSE}}}{50 \mu\text{A}} \quad (4)$$

Then select an available resistor with the closest value to the outcome of equation (4). After the resistor is chosen, use equation (5) to calculate the current limit I_{LMT} with the values of R_{SENSE} and R_{SET} . If the calculated I_{LMT} is not within 115% to 135% of I_{MAX} , reselect the R_{SENSE} and repeat the above steps until the current limit is set to within that range.

$$I_{\text{LMT}} = \frac{R_{\text{SET}} \times 50 \mu\text{A}}{R_{\text{SENSE}}} \quad (5)$$

With the R_{SENSE} and I_{LMT} determined, the maximum power rating for the sense resistor is limited by the following constraint:

$$P_{\text{RSENSE}} > 2 \times R_{\text{SENSE}} \times (I_{\text{LIM}})^2 \quad (6)$$

The maximum voltage rating of the resistor is recommended to be at least $2 \times V_{\text{IN(MAX)}}$.

2.4 MOSFET Selection

Some widely used N-channel power MOSFETs, which can be used with TPS23xx controllers, are listed in Table 1 as a reference.

Table 1. List of N-Channel Power MOSFETs Suitable for TPS23xx Hotswap Controllers

PART NUMBER	V _{DSS} (V)	I _D at 70°C (A)	V _{GS} (V)	R _{DS(on)} (mΩ)	T _J (MAX) (°C)	R _{θJC} (MAX) (°C/W)	PACKAGE	MANUFACTURER
SI3456DV	30	4.1	20	45	150	—	TSOP-6	Vishay/Siliconix
SI4420DY	30	10	20	9	150	—	SO-8	Vishay/Siliconix
SUD50N03-10	30	10	20	10	175	1.8	TO-252	Vishay/Siliconix
SI4874DY	30	13	20	7.5	150	21 (1)	SO-8	Vishay/Siliconix
SUY50N03-10CP	30	15	20	10	175	2.1	TO-251	Vishay/Siliconix
SUD30N03-30	30	21	20	30	175	3.0	TO-252	Vishay/Siliconix
SUD30N04-10	40	30	20	10	175	1.8	TO-252	Vishay/Siliconix
SUD50N03-10P	30	40	20	10	175	2.3	TO-252	Vishay/Siliconix
IRF7201	30	5.6	20	30	150	—	SO-8	International Rectifier
IRF7458	30	11	30	8	150	20 (2)	SO-8	International Rectifier
IRF7832	30	16	20	4	150	20 (2)	SO-8	International Rectifier
IRF6603	30	20	20	3.9	150	3.0	DirectFET	International Rectifier
IRLR3303	30	25	16	31	150	1.6	D-Pak	International Rectifier
IRL3103	30	45	16	12	175	2.2	D-Pak	International Rectifier

NOTES: 1. Junction-to-foot thermal impedance.
2. Junction-to-lead thermal impedance.

Due to hot plug and removal events, the input and output of the hotswap stage could have excessive voltage spikes. If a short circuit happens in the system, an excessive current spike can occur before the current limiting circuit takes control. Although the duration is usually very small, the energy can be large and potentially cause big voltage fluctuations on the rail. Yet a more severe condition, when the hotswap output is shorted to ground or a low-impedance load, causes the external MOSFET to operate at high current and high drain-to-source voltage, which could violate the safe operating area (SOA) of the MOSFET. Once that happens, MOSFET breakdown occurs. In order to ensure the safe operation of the external FET, the drain-to-source voltage rating of the FET, V_{DSS}, should be reasonably higher than V_{IN}. A 2-to-1 or 3-to-1 ratio of the V_{DSS} over V_{IN} is recommended. The current rating of the FET at the maximum case temperature (usually 70~100°C), I_D, should be at least 2 times the I_{LMT}.

$$V_{DSS} > 2 \times V_{IN} \quad (7)$$

$$I_{D@TC(MAX)} > 2 \times I_{LMT} \quad (8)$$

The gate-to-source voltage rating, V_{GS}, of the FET should be at least 14 V because the TPS23xx gate voltage can be as high as 12 V above the source voltage (or voltage on DISH pin).

$$V_{GS} > 14 \text{ V} \quad (9)$$

The other important parameter in choosing a FET is the on-resistance R_{DS(on)}. Assuming a minimum efficiency of η_{MIN} is given, the maximum R_{DS(on)} is

$$R_{DS(on)} < \frac{V_{IN} \times (1 - \eta_{MIN})}{I_{MAX}} - R_{SENSE} \quad (10)$$

With the V_{DSS}, I_D, V_{GS}, and R_{DS(on)}, a FET can be selected from Table 1 or other available power MOSFETs.

2.5 TIMER Capacitor and Gate Capacitor

With a selected FET, the maximum transient power dissipation, or so-called single pulse power P_{PULSE} can be calculated with given conditions and FET parameters. For a safe operation of the FET, it is essential to keep the worst case power dissipation under the pulse power limit. By choosing an appropriate capacitor on TIMER pin C_T , TPS23xx ensures the safe operation of the FET.

For power FETs from different manufacturers, different parameters and/or curves are provided for calculating the pulse power limit. Some FETs, such as several power MOSFETs from Vishay Inc., have characteristic curves showing the pulse power limit (P_{PULSE_LMT}) at different pulse widths. In those cases, just use the curves and find the pulse power value at 10-ms pulse width. If 10-ms pulse width is not available, use the pulse width (t_{pulse}) that is close to 10 ms. A factor of 0.5 is included for safety and also because the case temperature rises when the pulse power applies. That is:

$$P_{PULSE@tpulse} = 0.5 \times P_{PULSE_LMT} \times \frac{T_{J(MAX)} - T_{A(MAX)}}{T_{J(PULSE)} - T_{C(PULSE)}} \quad (11)$$

The $T_{J(MAX)}$ is the maximum junction temperature rating of the FET, the $T_{A(MAX)}$ is the application specified maximum ambient temperature, and the $T_{J(PULSE)}$ and the $T_{C(PULSE)}$ are the junction and case temperatures to generate the pulse power limit. Usually $T_{J(PULSE)}$ is the same as $T_{J(MAX)}$, and the $T_{C(PULSE)}$ is 25°C. If the $T_{J(PULSE)}$ and $T_{C(PULSE)}$ are not given, use $T_{J(MAX)}$ as the $T_{J(PULSE)}$, and let the $T_{C(PULSE)}$ equal to 25°C.

If the maximum safe operating area (SOA) curve of the FET is given, such as most FETs from International Rectifier Inc., and many FETs from Vishay Inc, the maximum current $I_{D(MAX)}$ at the given supply voltage V_{IN} can be found. Typically several SOA curves at different pulse widths, t_{pulse} , are provided. Use the 10-ms pulse width if available; otherwise, pick the pulse width that is close to 10 ms. Then the pulse power at t_{pulse} can be calculated by:

$$P_{PULSE@tpulse} = 0.5 \times V_{IN} \times I_{D(MAX)} \times \frac{T_{J(MAX)} - T_{A(MAX)}}{T_{J(PULSE)} - T_{C(PULSE)}} \quad (12)$$

Figure 2 shows an example of selecting the pulse power from a single pulse power curve and an SOA curve.

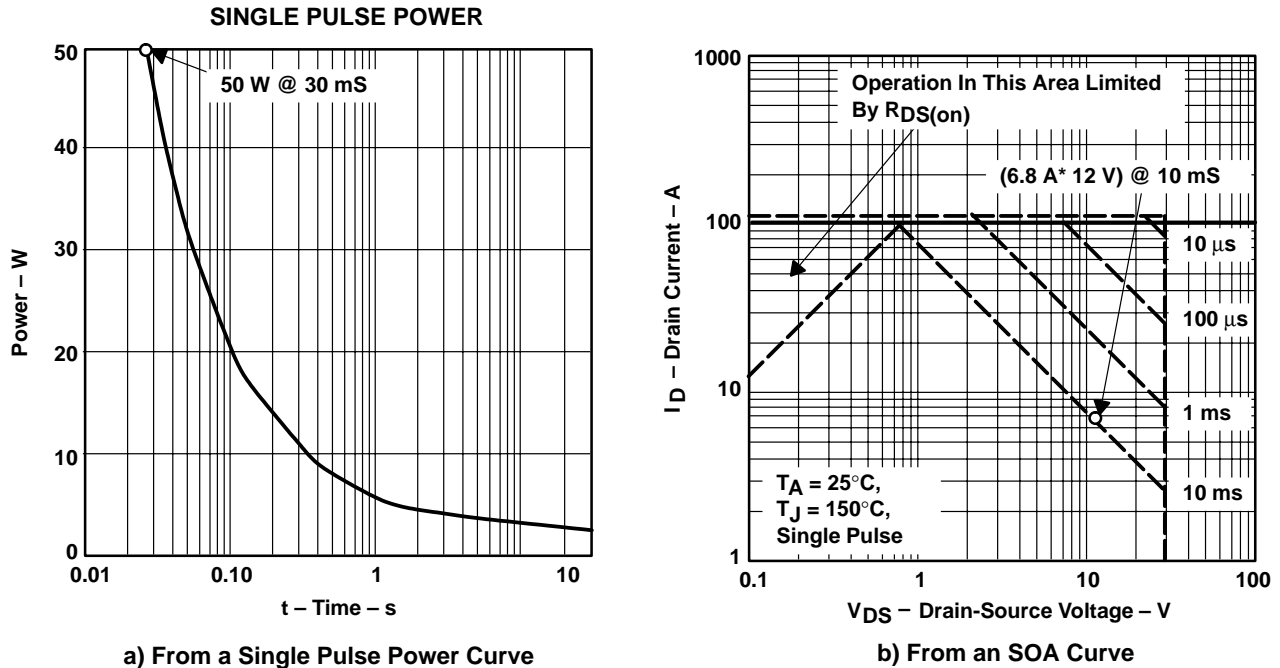


Figure 2. Find Pulse Power From a Single Pulse Power and SOA Curve

If both the pulse power curve and the SOA curves are not provided for the FET, although very unlikely, the thermal impedance of the FET can be used to calculate the pulse power:

$$P_{\text{PULSE@tpulse}} = 0.5 \times \frac{T_{\text{J(MAX)}} - T_{\text{A(MAX)}}}{R_{\theta\text{JC(MAX)}}} \quad (13)$$

where the $R_{\theta\text{JC(MAX)}}$ is the maximum junction-to-case thermal impedance (typically in the range of 1.0°C/W to 4.0°C/W); and let $t_{\text{pulse}} = 100 \text{ mS}$.

Sometimes, a so-called junction-to-lead or junction-to-foot thermal impedance is given instead of the junction-to-case thermal impedance. Then $R_{\theta\text{JC(MAX)}}$ can be estimated by dividing the junction-to-lead or junction-to-foot thermal impedance by a factor of 5. The method of using the thermal impedance to calculate the pulse power is to be used only when both the pulse power and SOA curves are not available.

With the calculated pulse power limit (P_{PULSE}) at a given pulse width (t_{pulse}), and the worst-case power dissipation for the FET is also known, which is $V_{\text{IN}} \times I_{\text{LMT}}$, then the maximum fault time before shutdown can be calculated by:

$$t_{\text{FAULT(MAX)}} = t_{\text{pulse}} \times \left(\frac{P_{\text{PULSE@tpulse}}}{V_{\text{IN}} \times I_{\text{LIM}}} \right)^2 \quad (14)$$

then the maximum timer capacitance C_{T} is:

$$C_{\text{T(MAX)}} = 0.8 \times t_{\text{FAULT(MAX)}} \times \frac{50 \mu\text{A}}{0.5 \text{ V}} \quad (15)$$

where 0.8 is a factor considering normal ceramic capacitor tolerance of $\pm 20\%$.

The minimum turnon ramp-up time, t_{ON} , is limited by the total load capacitance (C_{OUT}) and the current limit.

$$t_{ON(MIN)} = C_{OUT} \times \frac{V_{IN}}{I_{LMT}} \quad (16)$$

With the minimum turn-on time, the inrush current equals the current limit, I_{LMT} , thus the minimum timer capacitance is:

$$C_{T(MIN)} = 1.2 \times t_{ON(MIN)} \times \frac{50 \mu A}{0.5 V} \quad (17)$$

or

$$C_{T(MIN)} = 1.2 \times C_{OUT} \times \frac{50 \mu A \times V_{IN}}{0.5 V \times I_{LMT}} \quad (18)$$

where the factor 1.2 is also due to capacitance tolerance consideration.

If a lower inrush current (I_{inrush_spec}) or a longer turnon time (t_{ON_spec}) is required, an external capacitor (C_g) on the GATE pin of TPS23xx is required. With either I_{inrush_spec} or t_{ON_spec} specified, the other can be calculated with the following equation:

$$t_{ON_spec} = C_{OUT} \times \frac{V_{IN}}{I_{inrush_spec}} \quad (19)$$

Then the external gate capacitance (C_g) can be calculated by:

$$C_g = \left[\left(t_{ON_spec} \times \frac{14 \mu A}{V_{IN} + 1} \right) - C_{RSS} \right] \quad (20)$$

where C_{RSS} is the average gate-to-drain capacitance through the operating voltage range (0 V to V_{IN}) for the FET.

The C_{RSS} is not constant with the drain-to-source voltage changing, but fortunately it is relatively small and can be neglected in most cases. Then equation (20) can be simplified as:

$$C_g = t_{ON_spec} \times \frac{14 \mu A}{V_{IN} + 1} \quad (21)$$

If the average C_{RSS} of a FET is more than 10% of the calculated C_g from equation (21), then it should be considered, and the C_g should be calculated by equation (20) and not by equation (21).

When the inrush current during power up is less than the current limit, the TIMER is not charged in the power-up period and the minimum timer capacitance from equation (18) is no longer valid. However, for noise immunity, a minimum of 500-pF capacitance is required. Practically, a 1-nF gate capacitor is recommended as $C_{T(MIN)}$ to prevent the device from false triggering.

So the timer capacitor C_T must be well below the result from equation (15) and it must be larger than 1 nF, or the result from equation (18), depending on whether the inrush current is less than or equal to the current limit. Although the inrush current requirement sometimes is not specified by applications, it is still a good practice to set an inrush current that is lower than the current limit I_{LMT} . Then an external gate capacitance can be chosen according to equation (20) or (21).

With the selected gate capacitance, the turn-on time and the inrush current can be calculated by:

$$t_{ON} = C_g \times \frac{V_{IN} + 1}{14 \mu A} \quad (22)$$

and

$$I_{inrush} = \frac{C_{OUT}}{C_g} \times \frac{V_{IN}}{V_{IN} + 1} \times 14 \mu A \quad (23)$$

where the gate-to-drain capacitance C_{RSS} is ignored.

If the average C_{RSS} of a FET is more than 10% of the calculated C_g from equation (21), then C_{RSS} should be counted by replacing the C_g with $(C_g + C_{RSS})$ in equations (22) and (23).

2.6 The Resistors

A gate resistor is not needed for typical applications. Only if one GATE output of TPS23xx is used to drive multiple external power MOSFETs, then a 10-Ω or higher gate resistance, R_g , is required for each FET. Besides, some MOSFETs have unusually large gate leakage noise when operated at high voltage (e.g., 12 V); then a 10-Ω gate resistor should be added to filter out the noise.

The VSENSE resistor divider is set by:

$$R2 = R1 \times \frac{1.225 V}{V_{OUT_GOOD} - 1.225 V} \quad (24)$$

where the V_{OUT_GOOD} is the power-good output voltage threshold specified by the application.

For example, in a 12-V application, the V_{OUT_GOOD} is normally specified at about 10 V. To reduce the power dissipation in the divider and still provide a stable feedback, a 20-kΩ to 100-kΩ value for $R1$ is recommended.

The upper limit of the pullup resistors for PWRGD and FAULT depends on the amount of drive needed by the load. The internal pulldown transistors of TPS23xx limit the lower boundaries of $R3$ and $R4$. Those limits are:

$$R3 > \frac{VCC}{2 \text{ mA}} \quad (25)$$

$$R4 > \frac{VCC}{2 \text{ mA}} \quad (26)$$

where VCC is the pullup supply voltage of the PWRGD and FAULT.

The maximum allowable VCC voltage is 13 V, and it can be directly tied to the input supply or the output rail of the hotswap stage.

2.7 Extra Step for Dual-Channel Controllers

The design steps described above apply to all the single-channel and dual-channel controllers. For dual-channel controllers, use all the design steps above to design each channel independently except the final value of the TIMER cap, because the two channels have only one TIMER pin. Therefore, the timer cap value has to satisfy two sets of results for the two channels. In other words, first design the two channels separately to get the $C_{TX(MIN)}$ and $C_{TX(MAX)}$ for each channel, then select a value within both ranges:

$$\text{MAX} \left(C_{T1(\text{MIN})}, C_{T2(\text{MIN})} \right) \leq C_T \leq \text{MIN} \left(C_{T1(\text{MAX})}, C_{T2(\text{MAX})} \right) \quad (27)$$

2.8 Layout

All hotswap applications require a careful layout design effort because of the potential high current transients during hotswap or in fault conditions.

First of all, the power trace length from the input supply (V_{IN}) on the edge of the connector through the sense resistor to the FET and to the output load, should be minimized to reduce parasitic inductance and power loss. The width of the power trace should be large enough to handle the current and reduce the power loss. A ground plane is strongly recommended for the power return path.

The sense resistor layout is very important for the total accuracy of the design. Figure 3 shows a practical layout around the sense resistor.

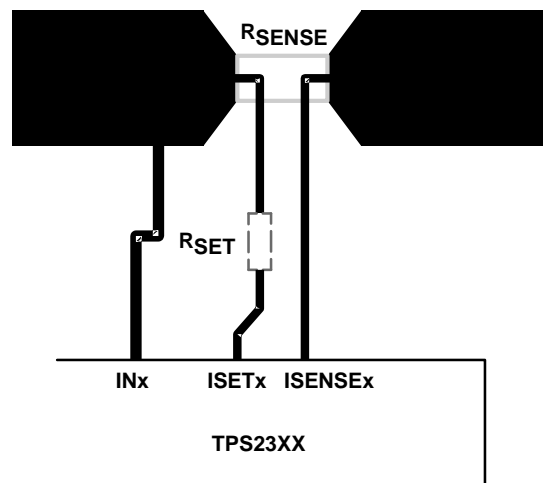


Figure 3. Recommended Layout Design Around the Sense Resistor

3 A Design Example

3.1 Application Specifications

$V_{IN} = 12 \text{ V}$, $I_{MAX} = 3 \text{ A}$, $C_{OUT} = 1000 \mu\text{F}$, $C_{BULK} = 220 \mu\text{F}$, $\eta_{MIN} = 98\%$, $T_{A(\text{MAX})} = 70^\circ\text{C}$, $V_{OUT_GOOD} = 10 \text{ V}$.

3.2 Design Steps

Since the application has only one supply, choose a single-channel controller (TPS2330 or TPS2331) as the hotswap controller.

STEP 1

$C_{IN} < C_{BULK}/1000 = 0.22 \mu\text{F}$, set $C_{IN} = 0.1 \mu\text{F}$.

$C_{byps} = 0.1 \mu\text{F}$; $C_{REF} = 0.1 \mu\text{F}$.

A Zener diode of 13 V is needed, so 1N4743A can be selected.

STEP 2

By equation (1),

$$I_{LMT_SET} = 1.25 \times I_{MAX} = 3.75 \text{ A}$$

By equation (2),

$$R_{SENSE} < \frac{V_{IN} \times (1 - \eta_{MIN})}{I_{MAX}} = 80 \text{ m}\Omega$$

By equation (3),

$$R_{SENSE} \geq \frac{40 \text{ mV}}{I_{LMT_SET}} = 10.67 \text{ m}\Omega$$

Select $R_{SENSE} = 15 \text{ m}\Omega$.

With equation (4),

$$R_{SET} = \frac{I_{LMT_SET} \times R_{SENSE}}{50 \mu\text{A}} = 1.125 \text{ k}\Omega$$

Therefore, use a 1.13-k Ω resistor for R_{SET} , since the value is readily available.

With the selected R_{SENSE} and R_{SET} , the current limit is set by equation (5):

$$I_{LMT} = \frac{R_{SET} \times 50 \mu\text{A}}{R_{SENSE}} = 3.77 \text{ A}$$

which is within 115% to 135% range of 3 A (or 3.45 A to 4.05 A range).

The power rating of the sense resistor is limited by equation (6):

$$P_{RSENSE} > 2 \times R_{SENSE} \times (I_{LIM})^2 = 0.213 \text{ W}$$

So the sense resistor must be rated at least 1/4 watt.

STEP 3

FET requirements are:

$V_{DSS} > 24 \text{ V}$, $I_D > 7.54 \text{ A}$, $V_{GS} > 14 \text{ V}$, and

$$R_{DS(on)} < \frac{V_{IN} \times (1 - \eta_{MIN})}{I_{MAX}} - R_{SENSE} = 65 \text{ m}\Omega$$

Then a FET can be selected. For example, SI4420DY can be chosen as the FET.

STEP 4

The single pulse power at $t_{\text{pulse}} = 30 \text{ ms}$ (shown on page 2–4 in the SI4420DY data sheet) is about 50 W.

By equation (11),

$$P_{\text{PULSE@tpulse}} = 0.5 \times 50 \times \frac{150-70}{150-25} = 16 \text{ W}$$

then:

$$t_{\text{FAULT(MAX)}} = t_{\text{pulse}} \times \left(\frac{P_{\text{PULSE@tpulse}}}{V_{\text{IN}} \times I_{\text{LMT}}} \right)^2 = 30 \times \left(\frac{16}{12 \times 3.77} \right)^2 = 3.75 \text{ ms}$$

Then the maximum timer capacitance C_T is:

$$C_{T(\text{MAX})} = 0.8 \times t_{\text{FAULT(MAX)}} \times \frac{50 \mu\text{A}}{0.5 \text{ V}} = 0.3 \mu\text{F}$$

Since no inrush current limit is specified, no gate cap is required. Without an external gate cap, the turnon time would be:

$$t_{\text{ON@no_gate_cap}} = C_{\text{OUT}} \times \frac{V_{\text{IN}}}{I_{\text{LMT}}} = 3.183 \text{ ms}$$

and the minimum timer capacitance should be

$$C_{T(\text{MIN})} = 1.2 \times C_{\text{OUT}} \times \frac{50 \mu\text{A} \times V_{\text{IN}}}{0.5 \text{ V} \times I_{\text{LMT}}} = 0.382 \mu\text{F}$$

Since $C_{T(\text{MIN})}$ is greater than $C_{T(\text{MAX})}$, there is no solution for C_T .

One option to solve the conflict is to select a larger FET and repeat above steps. The other option is to set a lower inrush current limit because lower inrush current is usually preferred. Although it is not specified in the given conditions of this example, it can be arbitrarily chosen. For example, let the maximum inrush current to be limited to 50% of I_{MAX} , or 1.5 A. Then the turnon time needs to be:

$$t_{\text{ON_spec}} = C_{\text{OUT}} \times \frac{V_{\text{IN}}}{I_{\text{inrush_spec}}} = 8 \text{ ms}$$

and the required external gate capacitance is:

$$C_g = t_{\text{ON_spec}} \times \frac{14 \mu\text{A}}{V_{\text{IN}} + 1} = 8.6 \text{ nF}$$

Since the C_{RSS} capacitance of SI4420DY found on page 2–3 of the data sheet is about 0.4 nF, which is much less than 8.6 nF, the result above is valid. The closest standard capacitance value of the C_g is 10 nF, therefore select $C_g = 10 \text{ nF}$.

With selected C_g , the inrush current is:

$$I_{\text{inrush}} = \frac{1 \text{ m}}{10 \text{ n}} \times \frac{12}{12 + 1} \times 14 \mu\text{A} = 1.29 \text{ A}$$

and the turnon time is:

$$t_{ON} = C_g \times \frac{V_{IN} + 1}{14 \mu A} = 9.29 \text{ mS}$$

Because the 1.29-A inrush current is well below the current limit of 3.77 A, the minimum timer capacitance is 1nF and the maximum is 0.39 μ F. In this situation, the system environment should be considered for the timer cap selection. For noisy applications (e.g. switching supply on the load), the timer capacitor value should be larger, such as a 10 nF or higher (but well below 0.39 μ F). For less noisy applications, a small timer capacitor—for example a 3.3-nF ceramic, does the job. Select $C_T = 3.3 \text{ nF}$ for this design example.

STEP 5

Last, choosing $R1 = 100 \text{ k}\Omega$, the bottom resistor of the VSENSE resistor divider can be determined by:

$$R2 = 100 \text{ k}\Omega \times \frac{1.225}{10 - 1.225} = 13.96 \text{ k}\Omega$$

The closest available resistance to this result is 14 k Ω , which almost equals the calculated value, therefore $R2 = 14 \text{ k}\Omega$.

$R3$ and $R4$ can be selected based on equation (25) and equation (26). Since V_{CC} is not given, tie V_{CC} to the output of the hotswap stage, such that $V_{CC} = 12 \text{ V}$. Therefore $R3$ and $R4$ must be greater than 6 k Ω . Since the driving capability of PWRGD and FAULT is not specified, 20 k Ω can be arbitrarily chosen for $R3$ and $R4$.

3.3 Summary of the Example

$V_{IN} = 12 \text{ V}$,
 $I_{MAX} = 3 \text{ A}$,
 $C_{OUT} = 1000 \mu\text{F}$,
 $C_{BULK} = 220 \mu\text{F}$,
 $C_{IN} = 0.1 \mu\text{F}$,
 $C_{byps} = 0.1 \mu\text{F}$,
 $C_{REF} = 0.1 \mu\text{F}$,
 $D1 = 1\text{N}4743\text{A}$,
 $R_{SENSE} = 15 \text{ m}\Omega$,
 $R_{SET} = 1.13 \text{ k}\Omega$,
 $I_{LMT} = 3.77 \text{ A}$,
 $M1 = \text{SI}4420\text{DY}$,
 $C_g = 10 \text{ nF}$,
 $C_T = 3.3 \text{ nF}$,
 $R1 = 100 \text{ k}\Omega$,
 $R2 = 14 \text{ k}\Omega$,
 $R3 = 20 \text{ k}\Omega$,
 $R4 = 20 \text{ k}\Omega$.

4 Design Tool

A TPS23xx design-in calculation tool based on the design approach described in this report is available at

<http://focus.ti.com/analog/docs/sampleutilities.tsp?path=templatedata/cm/utilities/data/tps23xxtool&templateId=2&familyId=64&navigationId=9871>. Or, go to <http://www.ti.com> and search keyword “TPS230x/1x/2x/3x Design-in Calculation Tool”.

With the *Input Cells* information entered step-by-step, the tool can automatically generate design results. Be aware that selection of some components and values at certain steps is required for the calculation.

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