

Clocking for Medical Ultrasound Systems

Ravindra Munvar, Christian Schmoeller, Julian Hagedorn, Leni Skariah, Arvind Sridhar

ABSTRACT

This application note discusses the importance of clocking in Ultrasound and also illustrates how some key TI devices achieve very low end to end jitter and phase noise. The application note also demonstrates how various stages have very low additive jitter.

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1 Introduction

Medical Ultrasound systems use Sound waves to generate images of the body. They do this by transmitting an Ultrasound wave into the body and then receiving the echo. This echo is processed to generate an image.

This transmission and reception of the ultrasound signals has to be highly synchronized – to achieve the best results. Precision Clocking is crucial to ensure that the information displayed has minimum artifacts.

Phase noise (frequency domain) or Jitter (time domain) is a measure of how much a clock signal's phase or switching edge deviates from its ideal position and is an important parameter that can determine the impact of reference clocks on the ultrasound image. For example, ultrasound often uses the Doppler Effect to determine the direction and magnitude of blood flow. Higher phase noise can lead to artifacts occurring in Doppler images – such as speckles – which represent errors in the calculation and display of blood flow. In Doppler imaging, the strong reflection from close surfaces and weak signals from higher depths – results in a high dynamic range and jitter on the reference clock can potentially create undesired artifacts.

TI's high performance AFEs need a jitter performance of less than 800 fs to 1 ps to perform optimally especially in the CW Doppler mode.

There are various subsystems in the Ultrasound systems which need clocking:

1. Front End:

- (a) Transmit Pulsers – Need several copies of very low jitter, high frequency clocks in the range of 160 MHz+ to achieve good beam focusing. (An example of ultra-low jitter reference source from TI is the LMK61E2 family of crystal oscillators. Examples of ultra-low additive jitter buffers from TI that can be used to distribute low noise reference clocks are CDCLVC1310, LMK0030X, and so forth)
- (b) Receive AFEs – Require several low skew copies of highly synchronized clocks for all the AFEs to ensure that the data is sampled simultaneously. Frequencies are in the range of 40 to 80 MHz. (An example of a low skew distribution buffer family from TI is LMK0030X.)
- (c) CW Doppler – Requires two very-low phase noise clocks which are crucial to determine the frequency shift. Range from 2 to 128 MHz. (An example of a high performance dual-loop jitter attenuator/clock generator device family from TI suitable for generating CW Doppler clocks is LMK048xx or LMK0461x.)
- (d) Beam-forming FPGAs – For transmit and receive beam-forming the clocks need to be highly synchronized (LMK0030x fanout buffers). Transmit beam-forming focuses the ultrasound wavefront. Precise timing is required and any variation in the clock edges (jitter) can lead to loss of focus. The losses of precise synchronization between transmit and receive beamforming can also result in loss of image resolution.
- (e) FPGAs can also be used to generate the clocks needed for transmit and receive timing, but the jitter performance of these clocks is typically not nearly as good as specialized clocking ICs. The jitter then needs to be cleaned by external jitter cleaners. (Examples of high-performance, dual-loop jitter attenuators from TI include LMK04610 and LMK0480x.)

2. Power Supply:

- (a) All the power supplies within the Ultrasound system are often synchronized to one master clock to avoid the effects of switching noise appearing as artifacts in the image (through filtering). These power supplies typically operate in the range of 100 kHz to 1 MHz. Higher switching frequencies often result in smaller magnetic components but also operate closer to the dynamic range of the ultrasound signals themselves. Synchronizing all switching power supplies to the same (lower) frequency and then filtering at that frequency can avoid any coupling of this noise into the ultrasound signal chain. In addition, spread spectrum clocking can help to reduce EMI effects. (Examples of flexible clock generators with spread-spectrum generation capability used to minimize EMI in the system includes CDCE913 and CDCE6214)
- (b) Once the signals are digitized and provided to the digital post-processing sub-systems, the jitter is then not as critical. However it is desirable to have clean clocks throughout the entire system – to ensure maximum performance and lower overall noise in the system.

3. Backend:
 - (a) FPGAs – for image processing require frequencies which include the sampling frequency and others needed for communication and internal logic blocks. (CDCM6208, LMK033x8, CDCE6214, LMK60xx)
 - (b) DSPs and Processors – for image processing – require common frequencies like 100 MHz. (CDCM6208, LMK03328, CDCE6214)
 - (c) External communication – PCI, PCI Express, USB, Ethernet, and so forth, that typically require 24-, 48-, and 100-MHz clocks (CDCM6208, CDCE6214)

System designers prefer using clocks with the features as listed as follows:

1. Low power dissipation (LMK04610, CDCE6214)
2. Programmability and scalability – to support additional features or variations at a later date – without change in hardware. (LMK61E2 reference oscillator, any LMK or CDC clock generator)
3. High integration (less number of parts and smaller board real estate) (LMK04610, LMK04803, LMK03328, CDCE913, and so on.)
4. Fully-differential clocking wherever possible in the signal chain (common mode noise rejection).

Precision clocking can be achieved by having ultra-low noise clock sources, generators/dividers, distributors and buffers. The clocks generators are accurate and typically have lower phase noise when integer mode PLL and output dividers are used versus fractional mode PLL and/or fractional output dividers – that could introduce additional phase noise and potentially some small frequency synthesis error.

The impact can be minimized by ensuring that the front-end signal chain uses exclusively integer dividers to generate the clocks needed for the front end.

For the fanout of clock signals it is important to select buffers with very low additive jitter, otherwise the noise floor of a high quality source clock (that is, LMK61E2) would degrade significantly each time it is buffered. Suitable Buffers for this kind of application are the LMK0030x family (differential) and the CDCLVC1310 (LVCMOS), that have very low additive jitter.

TI's clock generator, dividers and low jitter buffers are some key components which help achieve this required performance.

[Table 1](#) and the [Figure 1](#) show a typical clock tree for an Ultrasound system. This clock tree demonstrates the use of various reference clocks for different building blocks – Transmit, Receive, FPGAs, Processors, power supply, and so on.

Table 1. Clock Requirement for 128-Channel Cart-Based Ultrasound System

NO OF CLKS	FREQUENCY	FORMAT	TARGET	PERFORMANCE
128	100 MHz	LVCMOS	DAC + AMP Clock	Good Phase Noise
2	40 MHz	LVCMOS	CW Mixer	Good Phase Noise
2	120 MHz	LVDS	FPGA (AWG)	
2	200 MHz	LVDS	FPAG (Transmit)	
1	200 MHz	LVDS	FPGA (Receive)	
16	100 kHz to 500 kHz	LVCMOS	Power Supply	
8	128 MHz	LVDS	AFE	Good Phase Noise
8	80 MHz	LVDS	AFE	Good Phase Noise
8	8 MHz	LVDS	AFE	Good Phase Noise
1	122.88 MHz	LVDS	DSP	
3	100 MHz	LVDS	DSP	
1	24.576 MHz	LVCMOS	Audio Codec	

Tests were conducted to demonstrate the total additive jitter and also jitter in various clock configurations for the clock tree by using individual evaluation modules from the different clocking components.

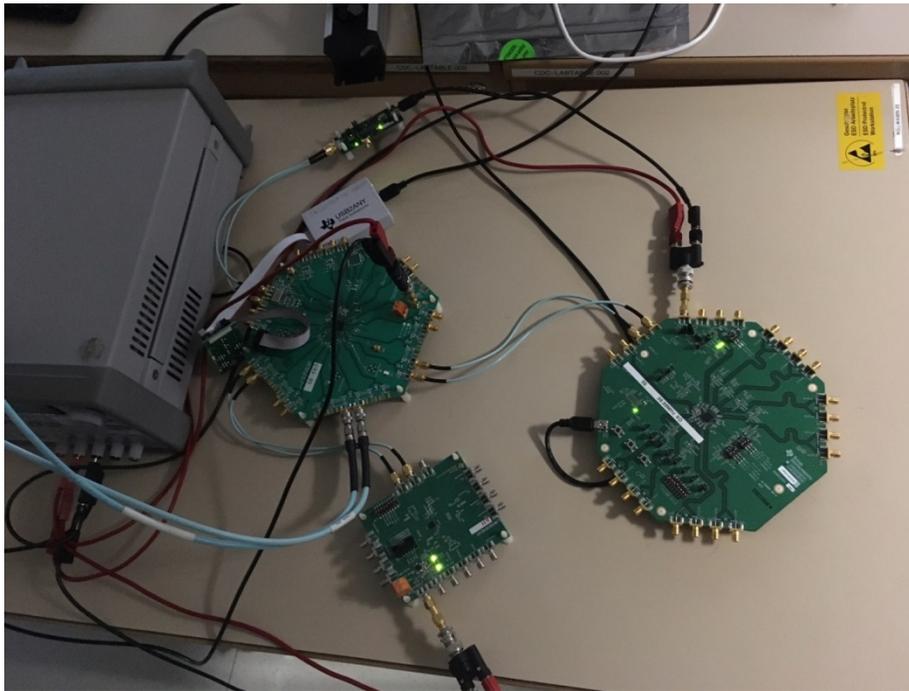
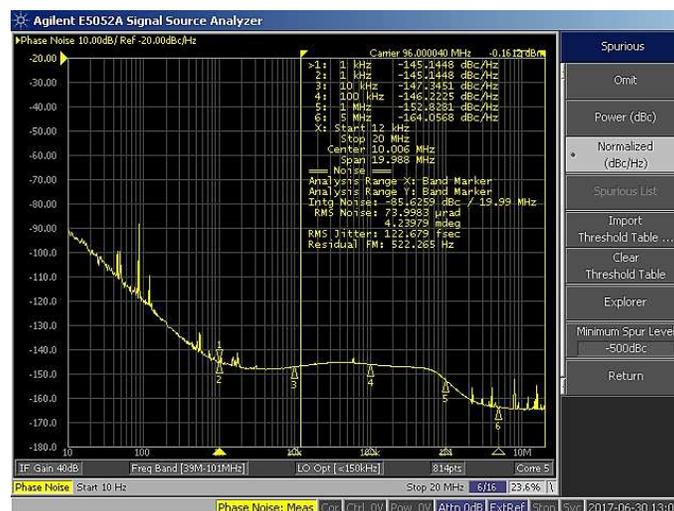


Figure 3. Different Clocking Components

The following graphs demonstrate the noise performance of the actual signals as measured on a signal source analyzer.

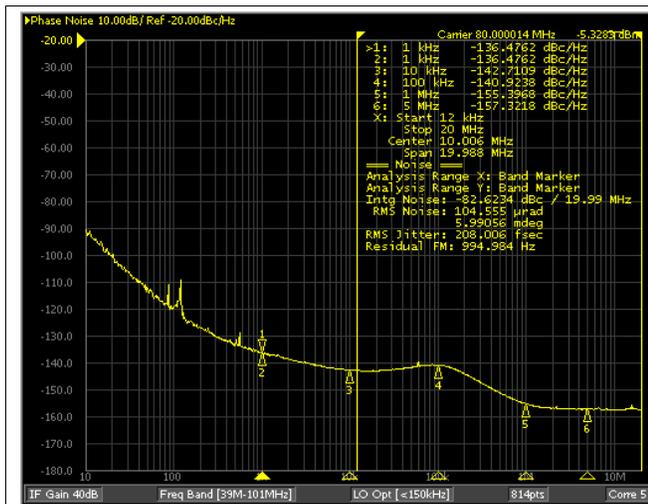
Demonstration 1:



Reference = 80 MHz LVDS (Output signal with and without Spurs) Integrated.
 Integrated RMS Jitter (10 kHz – 20 MHz) – 122 fs

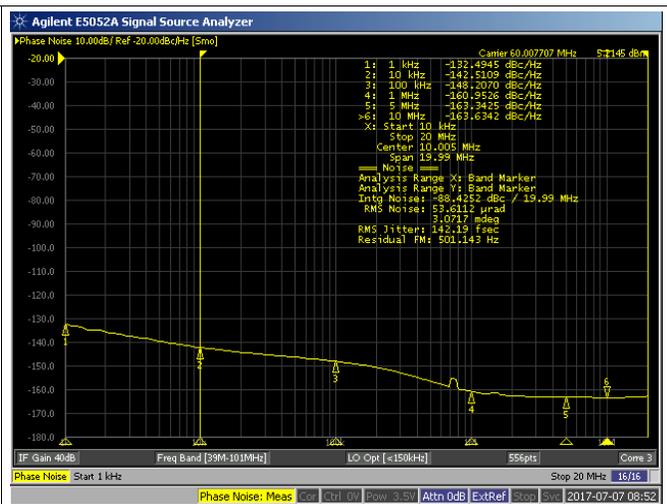
Figure 4. Demonstration 1, LMK61E2

Demonstration 2:



Reference = 80 MHz LVDS
Integrated RMS Jitter (10 kHz – 20 MHz): 208 fs

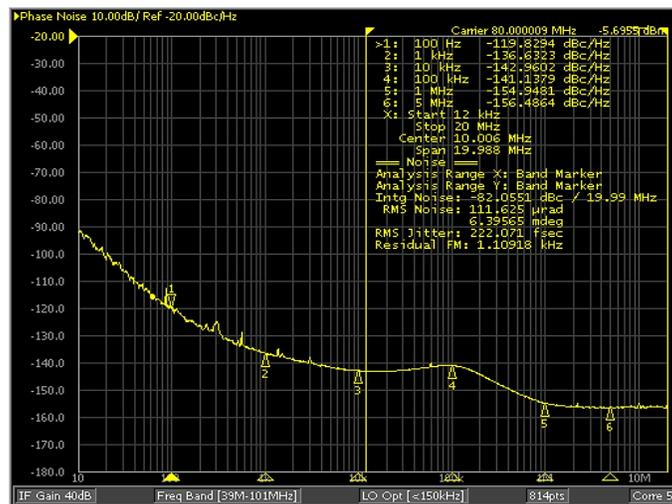
Figure 5. Demonstration 2, LMK04803



Integrated RMS Jitter (10 kHz – 20 MHz): 151 fs

Figure 6. Demonstration 2, LMK04610

Demonstration 3:



80 MHz
Integrated RMS Jitter (10 kHz – 20 MHz) – 222 fs

Figure 7. Demonstration 3, LMK0030X

A comparison of all the three demonstrates the following:

- The integrated RMS jitter from the output of LMK61E2 to LMK04803 increases by +86 fs. The integrated RMS jitter from the output of LMK04803 to LMK0030X increases by 14 fs.
- The total increase in the integrated RMS Jitter from Source to destination is just 100 fs.

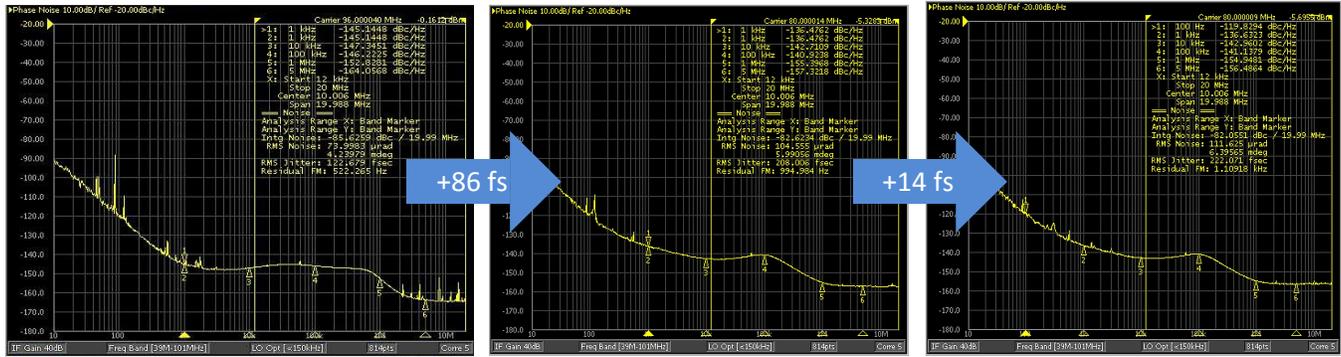


Figure 8. Comparison of LMK04803 to LMK0030X

Using LMK0461X series device helps reduce the total additive jitter as in Figure 9.



Figure 9. Comparison of LMK0461X Series

Using LMK0461X certain frequency combinations can also result in lower jitter as shown in Figure 10. Even if the input Jitter is high, the LMK04610 acts as a jitter cleaner and can deliver much better results – 94 fs Jitter against the input jitter of 122 fs. Figure 10 has input of 40 MHz and an output of 200 MHz. So an appropriate selection of input and output frequencies can deliver good phase noise and jitter along with appropriate Clock generator devices

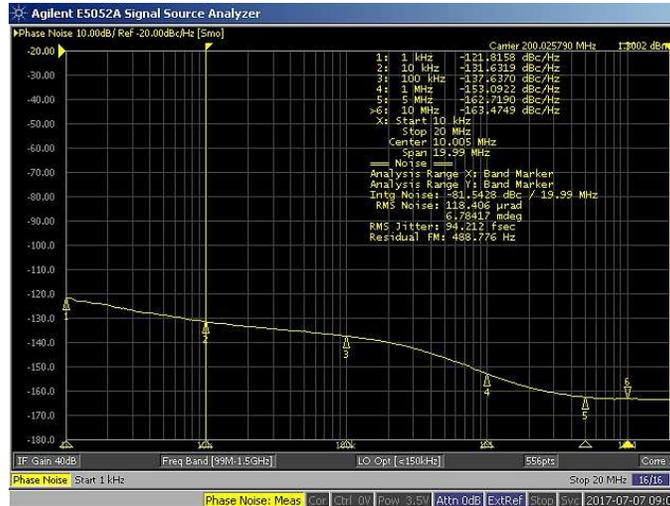


Figure 10. LMK0461X Frequency Combinations

3 Summary and Conclusion

- The TI LMK series of Clock devices offer excellent additive jitter performance throughout the entire clock chain – which are ideally suited for Ultrasound applications.
- As noted above, the end to end jitter is well within the required limits of TI's high performance AFEs to achieve optimal performance. This low end to end jitter of TI's clock devices allows system designers sufficient headroom to take care of other factors and noise that might impact the clock performance in the system.
- For typical Ultrasound applications it is possible to achieve superior clocking performance – by ensuring very low reference clock phase noise and edge jitter.
- With the scheme and block diagram presented in the previous sections, a 320-MHz source provided the best overall clocking system performance.
- If different reference frequencies are selected, TI provides a wide choice of other high performance dual-loop jitter attenuator/clock generator devices like the LMK046XX family – which offers additional benefits as:
 1. Lower noise floor
 2. Higher phase detector operating rates that reduces PLL noise further
 3. Better VCO noise performance
 4. Integrated LDOs
 5. Low power

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