Application Report
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Troubleshooting Guide for PGA411-Q1

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ABSTRACT

Use this guide as the first step in troubleshooting any issues while using the PGA411-Q1 device. This guide includes example waveforms and information on faults that assist in the process to troubleshoot issues.

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1 Getting Started

To read the faults, refer to the DEV_STAT1, DEV_STAT3, DEV_STAT4, and DEV_STAT7 registers in the PGA411-Q1 data sheet (SLASE76). Refer to Table 1 through Table 4 for support on troubleshooting these faults which are read using the registers.

Troubleshooting Note: When FAULTRES is pulled high by the microcontroller (for example to VIO), faults are reported normally. When FAULTRES is pulled low, all the faults are cleared. When FAULTRES is again pulled high, all the faults that exist in the system should be displayed.

Table 1. Error Flags and Quick Checks: DEV_STAT1

FLAG NAME	FLAG CONDITION	TROUBLESHOOTING STEPS
FLOOP_CLAMP	Sensor inputs changing too fast	Decrease the RPMs. Check that the resolver sensor is connected correctly. Refer to Section A.4 to ensure the resolver is connected properly.
FRCRC	Device configuration CRC8 check fail	Confirm that the DEV_CRC register contains the correct CRC8 value for the device configuration. Verify the CRC-8 calculation according to Section A.5.
FCECRC	User EEPROM CRC8 check fail	Confirm that the DEV_CLCRC register contains correct CRC8 value for the user EEPROM. Verify the CRC-8 calculation according to Section A.5.
FTECRC	TI EEPROM CRC8 check fail	Contact e2e.ti.com or the local sales support office.
EXTILIM	Exciter amplifier OEX pins exceeded current limit	Increase the current limit using the EXTILIMTH_XX_X register settings. Make sure that the measured output current of the exciter amplifier does not exceed data sheet specifications. Refer to Section 3 to verify the power supply of the excitation amplifier. Refer to Section A.6 for modifying this setting in the Exciter Amplifier Diagnostics in the EVM GUI.
EXTUV	Exciter amplifier OEX pins differential undervoltage	Increase the differential amplitude using the EXTOUT_GL register setting. Increase the deglitch time of EXTUV using the EXTUVT and EXTUVF_CFG register settings. Refer to Section A.6 for modifying this setting in the Exciter Amplifier Diagnostics in the EVM GUI. Refer to Section 3 to verify OE1 and OE2.
EXTOV	Exciter amplifier OEX pins differential overvoltage	Decrease the differential amplitude using the EXTOUT_GL register setting. Increase the deglitch time of EXTOV using the EXTOVT register setting. Refer to Section A.6 for modifying this setting in the Exciter Amplifier Diagnostics in the EVM GUI.
FLOOPE	Tracking loop error threshold exceeded	Make sure that the resolver sensor is connected correctly. Refer to Section A.4 to ensure the resolver is connected properly. Measure the IZx pin voltages on an oscilloscope to make sure the resolver sensor output waveform is within the data sheet specification. Refer to Section 4 to verify the IZx pins and the OSIN and OCOS pins. Increase the error threshold of the tracking loop using the LPETHX register settings. Increase the deglitch time of the tracking loop error using the TRDHL register setting. Refer to Section A.8.
FOCOSOPL	OCOS pin short to GND(1)	Make sure that the IZx pins are not shorted (see Section 4 to verify the IZx pins and the OSIN and OCOS pins). Observe the OCOS pin voltage and make sure it is centered around 0.5 × VCC. Lower the FOCOSOPL threshold voltage using the OOPENTHL register setting. Increase the deglitch time of FOCOSOPL using the TOPEN register setting. Decrease the analog front-end (AFE) gain using the GAINSIN and GAINCOS register settings. Refer to Section A.7 for changing this setting.
FOSINOPL	OSIN pin short to GND(1)	Make sure that the IZx pins are not shorted. Observe the OSIN pin voltage and make sure it is centered around 0.5 × VCC. Lower the FOSINOPL threshold voltage using the OOPENTHL register setting. Increase the deglitch time of FOSINOPL using the TOPEN register setting. Decrease AFE gain using the GAINSIN and GAINCOS register settings. Refer to Section A.7 for changing this setting.

(1) A short on the OCOS pin does not trigger not trigger this short; it detects shorts on the IZx pin.

Table 1. Error Flags and Quick Checks: DEV_STAT1 (continued)

FLAG NAME	FLAG CONDITION	TROUBLESHOOTING STEPS
FOCOSOPH	OCOS pin short to supply(1)	Make sure that the IZx pins are not shorted. Observe the OSIN pin voltage and make sure it is centered around 0.5 × VCC. Increase the FOCOSOPH threshold voltage using the OOPENTHH register setting. Increase the deglitch time of FOCOSOPH using the TOPEN register setting. Decrease AFE gain using the GAINSIN and GAINCOS register settings. Refer to Section A.7 for changing this setting.
FOSINOPH	OSIN pin short to supply(1)	Make sure that the IZx pins are not shorted. Observe the OSIN pin voltage and make sure it is centered around 0.5 × VCC. Increase the FOSINOPH threshold voltage using the OOPENTHH register setting. Increase the deglitch time of FOSINOPH using the TOPEN register setting. Decrease AFE gain using the GAINSIN and GAINCOS register settings. Refer to Section A.7 for changing this setting
SPI STAT[1:0]	SPI communication errors: 0b01: Invalid CRC or invalid SPI clock during previous frame 0b10: Data output mismatch during previous frame 0b11 Invalid address during previous frame	0b01: Make sure the SPI CRC6 value is correct, and that the frame contains 32 clock pulses. Check for glitches on the SCLK pin. 0b10: Make sure the SDO pin does not have any shorts. 0b11: Make sure that the sent register address is the intended value. Make sure the device is in the correct device mode for reading writing certain registers(such as normal mode, diagnostic mode, or device unlock mode).
FGOPEN	Ground pins are open	Check the ground pin connections.
FOSHORT	OCOS, OSIN pin short to COMAFE	Check the IZx pins for pin-to-pin shorts (refer to Section 4 to verify the IZx pins and to verify the OSIN and OCOS pins). Adjust FOSHORT thresholds closer to 0.5 × VCC using the OSHORTX register settings. Increase the deglitch time of FOSHORT using the TSHORT register setting. Increase AFE gain using the GAINSIN and GAINCOS register settings. Refer to Section A.7 for changing this setting.

Table 2. Error Flags and Quick Checks: DEV_STAT3

FLAG NAME	FLAG CONDITION	TROUBLESHOOTING STEPS
OMIZxL	IZx pin short to GND	Check the IZx pins for a short (see Figure 3). Decrease the OMIZxL threshold voltage using the DVMSENL register setting. Refer to Section A.7 for changing this setting.
OMIZxH	IZx pin short to supply	Check the IZx pins for a short (see Figure 3). Increase the OMIZxH threshold voltage using the DVMSENH register setting. Refer to Section A.7 for changing this setting.
FIZLx	IZx pin short to GND	Check the IZx pins for a short (see Figure 3). Decrease the FIZLX threshold voltage using the OVIZL register setting. Increase the deglitch time using the IZTHL register setting. Refer to Section A.7 for changing this setting.
FIZHx	IZx pin short to supply	Check the IZx pins for a short (see Figure 3). Increase the FIZHX threshold voltage using the OVIZH register setting. Increase the deglitch time using the IZTHL register setting. Refer to Section A.7 for changing this setting.

Table 3. Error Flags and Quick Checks: DEV_STAT4

FLAG NAME	FLAG CONDITION	TROUBLESHOOTING STEPS
FEXTMONx	IEx pin open/short	Check that the IEX pins are connected to the OEX pins, and that the IEX pin voltages are within the data sheet specification. Refer to Section 5. Make sure the IE1 and IE2 are complementary sine waves.
SPI_ERR	Logical OR of STAT[1:0] fault flag bits	Read the STAT[1:0] register field for more detailed SPI fault reporting.
FBSTOV	VEXT pin overvoltage	Check that the VEXT pin voltage is within the data sheet specification for the programmed MODEVEXT register setting (refer to Section 2). Check for shorts to battery.

Table 3. Error Flags and Quick Checks: DEV_STAT4 (continued)

FLAG NAME	FLAG CONDITION	TROUBLESHOOTING STEPS
FVDDOC	VDD pin overcurrent	Check that the VDD pin current is within the data sheet specification.
FTSD2	Overtemperature warning	Make sure the package cooling solution for the PGA411-Q1 device is adequate.
FEXTMODE	EXTMODE programmed to invalid setting	Make sure the EXTMODE register field is only programmed to 0b01 or 0b10.
ABISTF	ABIST failed	If the VEXT pin is not planned to be powered during the device startup, program BOOST_VEXT_MASK to 1 in the user EEPROM. Make sure the external crystal is at 20 MHz when running the device with the ECLKSEL pin high.
LBISTF	LBIST failed	Contact e2e.ti.com or the local sales support office.
FVCCOV	VCC pin overvoltage	Check the VCC pin voltage.
FVDDOV	VDD pin overvoltage	Check the VDD pin voltage.
IOFAULT	FAULT pin output mismatch	Make sure that the FAULT pin is not strongly shorted.
SFAULT	Fault pin signal monitor	Indicates faults in the system or that a FAULT pin is shorted.

Table 4. Error Flags and Quick Checks: DEV_STAT7

FLAG NAME	FLAG CONDITION	TROUBLESHOOTING STEPS
FAFECAL	AFE autocalibration failed	Contact e2e.ti.com or the local sales support office.

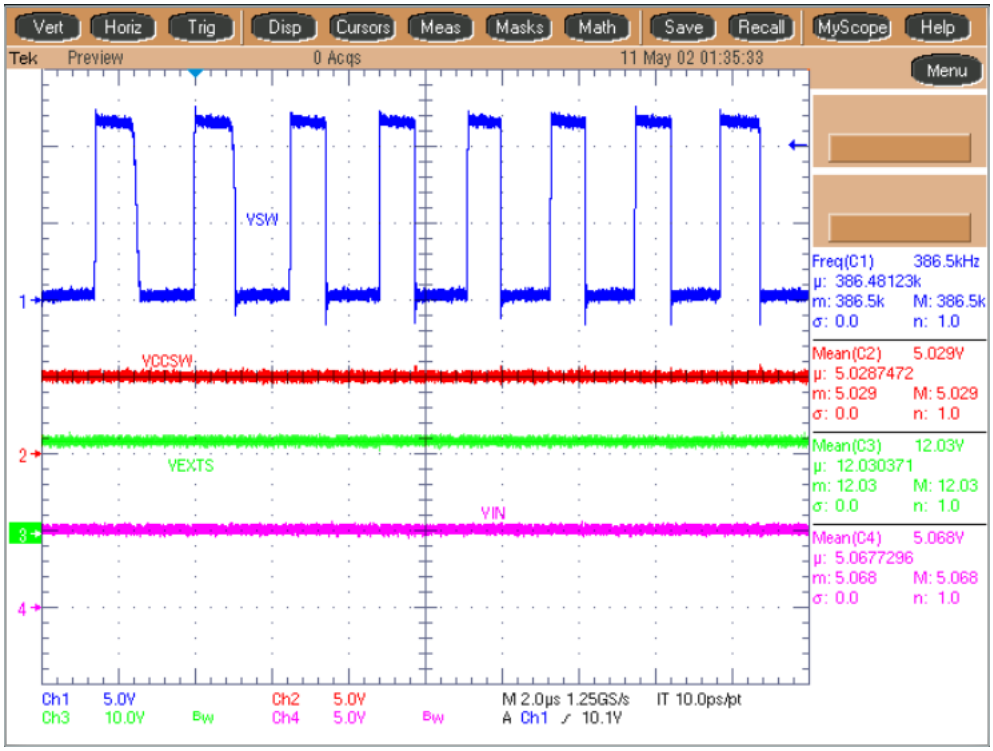
For additional troubleshooting help, see the following sections:

- FAULTRES operation, Section A.1
- Reading non-zero velocity from the PGA411-Q1 output, Section A.2
- Boost supply operation issues, Section 2
- Tracking loop operation (including AOUT), Section 5 and Section A.8

2 Boost Supply

Ensure that the boost supply is switching properly and that no unexpected noise exists in the system.

Figure 1 shows the boost example from 5 V to 12 V. The switching frequency can vary from approximately 380 kHz to 420 kHz. The typical switching frequency is approximately 414 KHz.



For a target voltage of 12 V.

VSW — is the boost switching node of PGA411-Q1

VCCSW — is the input supply of the boost

VEXTS — is the boost regulator feedback pin; the diagnostics monitoring is on the VEXT pin

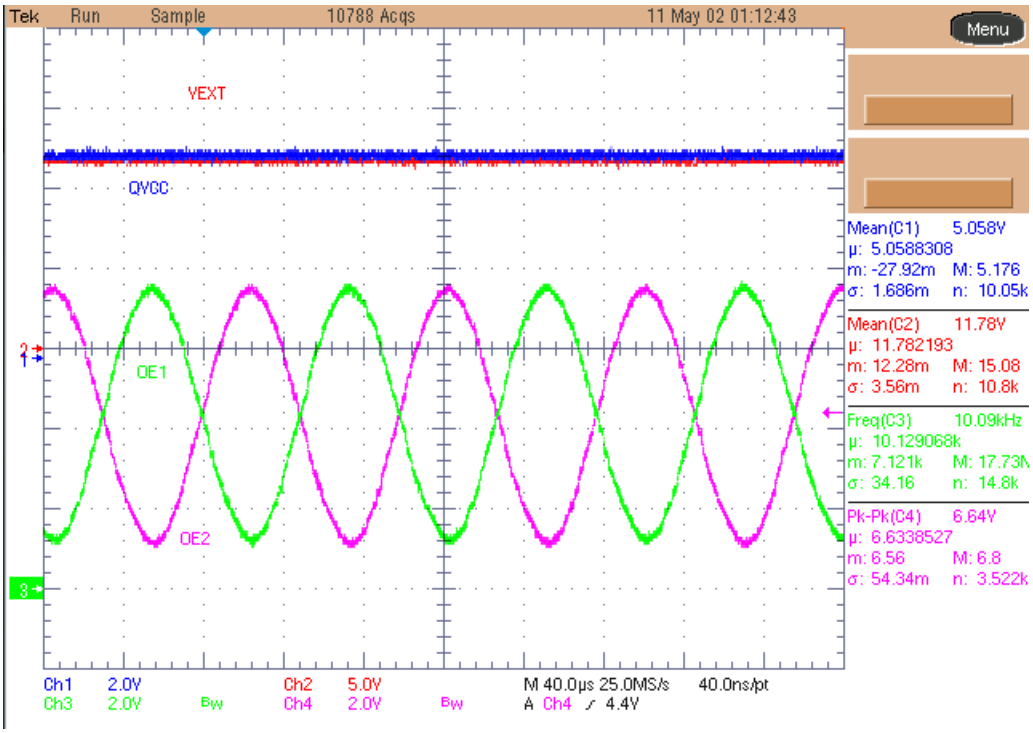
VIN — is the input to the board

Figure 1. Boost Supply Operation

Troubleshooting Note: Check the input voltage and output voltage of the boost supply. Otherwise, check the power supply source and values of the components used in the boost supply. If the boost power supply is not stable, ensure these values match those recommended in the data sheet. Also, ensure that the layout of the power supply board follows the recommendations listed in the PGA411-Q1 data sheet.

3 Excitation Amplifier

Figure 2 shows the excitation amplifier outputs (OE1 and OE2) referenced to ground. To help troubleshoot excitation amplifier, first make sure that the OE1 and OE2 waveforms look like those shown in Figure 2 when the resolver is not connected. Also, make sure QVCC and VEXT are in the expected range according to the PGA411-Q1 data sheet specifications.



QVCC — is the quiet VCC for PGA411-Q1

VEXT — is the exciter power-supply output or exciter-amplifier input supply

OE1 — is the output of exciter amplifier (referenced to ground)

OE2 — is the output of exciter amplifier (referenced to ground)

Figure 2. Excitation Amplifier Operation

Troubleshooting Note: The quiet VCC (QVCC) and exciter power supply (VEXT) should have good-quality decoupling capacitors at the device pins to prevent noise that can cause disturbance in device operation.

4 Analog Front-End Inputs (IZx) and Outputs (OSIN and OCOS)

With resolver connected, review the IZ1, IZ2, IZ3, and IZ4 inputs. Different types of resolver sensors can have a different transfer coefficient which is usually in the range of 0.35 to 0.5. Therefore, additional resistance may be needed in the input signal path to further attenuate the input signal which otherwise would cause the OSIN and OCOS outputs to saturate.

Troubleshooting Note: Use the equations from the data sheet to calculate component values and to select the value of the resistors at the AFE input. Again, depending on the resolver, the SIN and COS signals must be adjusted so that the OSIN and OCOS output swing follows the input requirements listed in the data sheet specifications. Adjust GAINCOS or GAINSIN to a lower setting if OCOS or OSIN are not within the specifications.

Figure 3 shows the IZ signals.

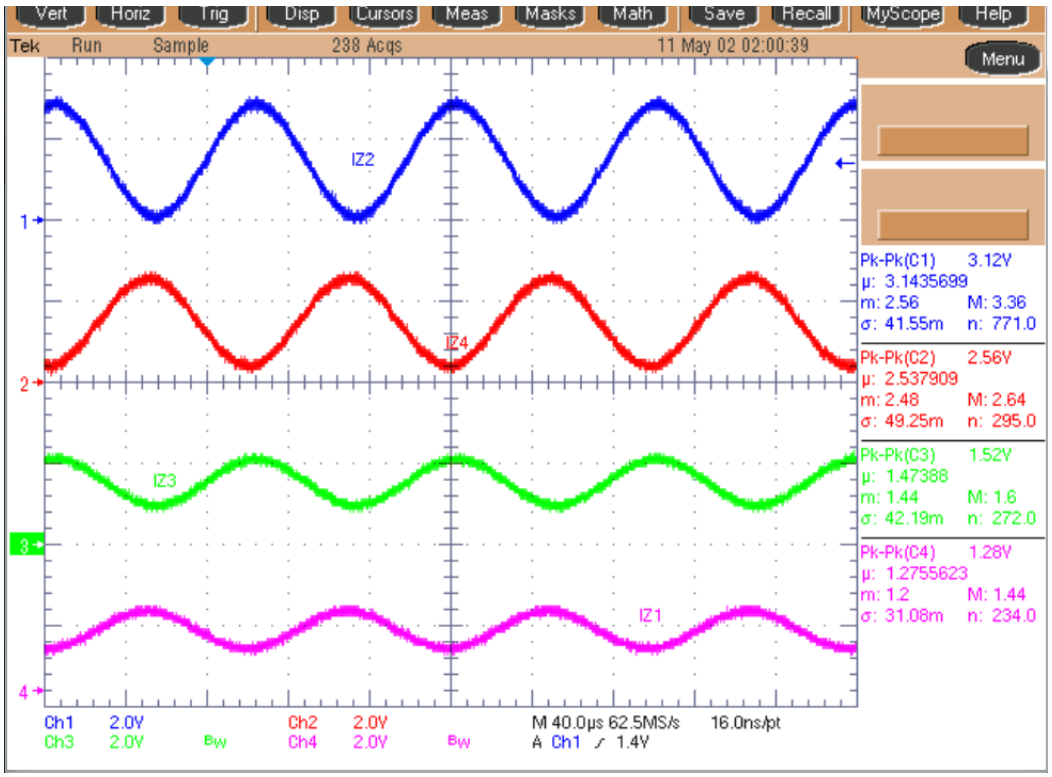


Figure 3. Inputs at IZx Pins

The AFE is referenced to the quiet ground pin (QGND) and powered by the quiet voltage supply pin (QVCC). The supply for the QVCC pin must go high at the same time as VCC for normal operation of the device. TI recommends tying QVCC to VCC with additional local capacitance to filter further noise from being introduced.

Figure 4 shows the OSIN and OCOS signals.

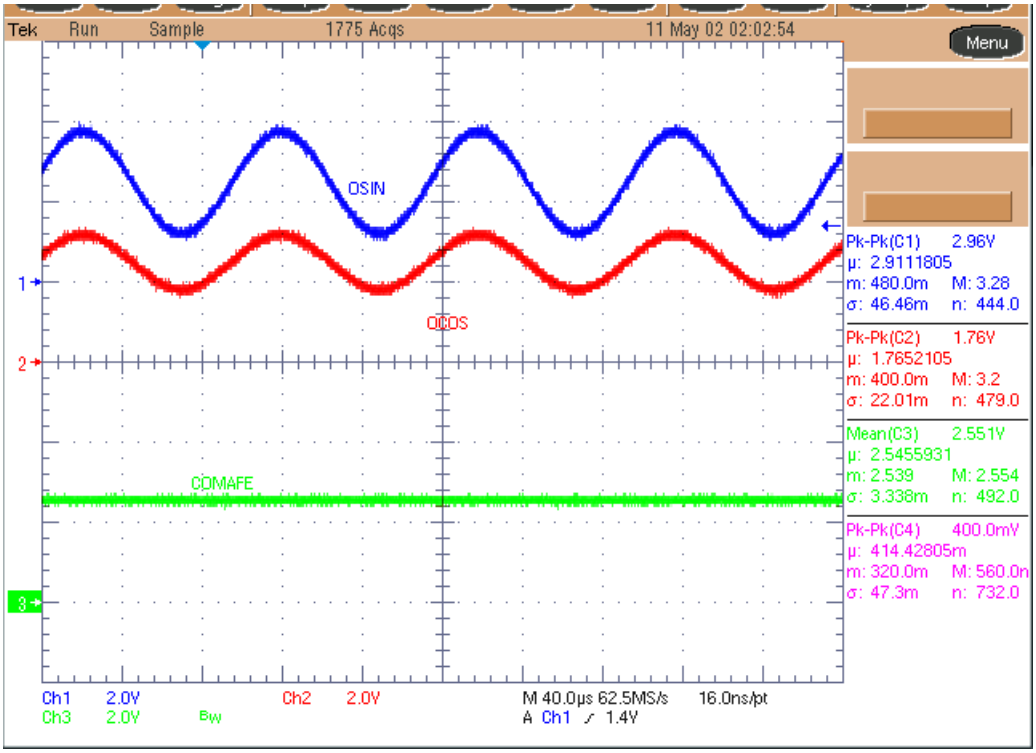


Figure 4. OSIN and OCOS Outputs

5 Tracking Loop

Figure 5 shows the AOUT performance when the RDC is working correctly and the resolver sensor is rotating with constant velocity.

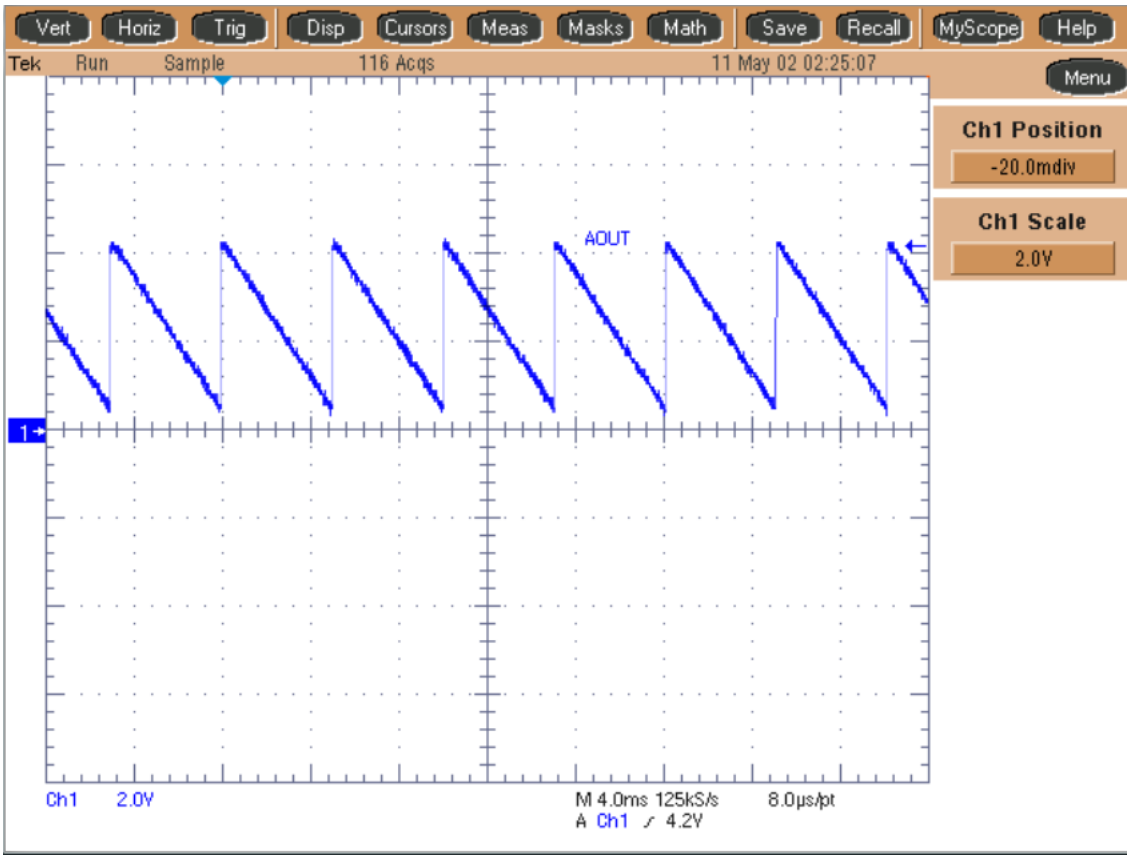


Figure 5. Test Output of Analog DAC

The AOUT has a fixed angular position when the resolver is not moving. Figure 6 shows the OE1, OE2, and AOUT pins for a complete picture of the system function.

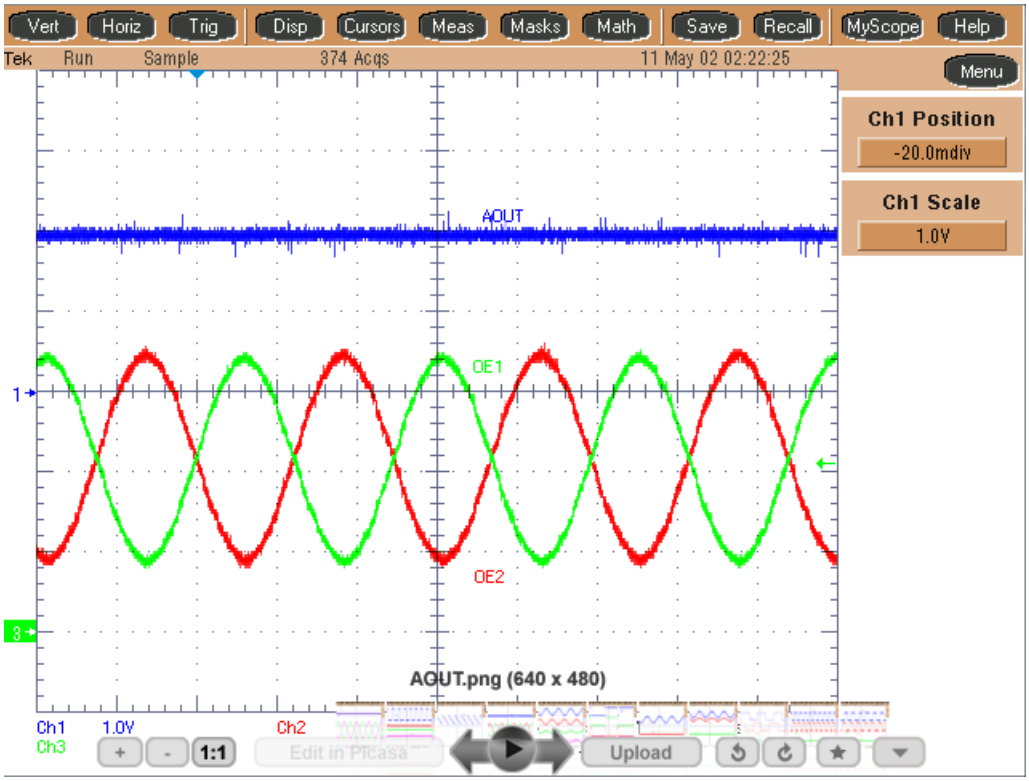


Figure 6. Tracking Loop Locked (AOUT Output is a Fixed Value)

Capture all the waveforms. For any additional questions, contact e2e.ti.com or the local sales support office.

Troubleshooting Note: Figure 6 shows AOUT if the tracking loop is locked.

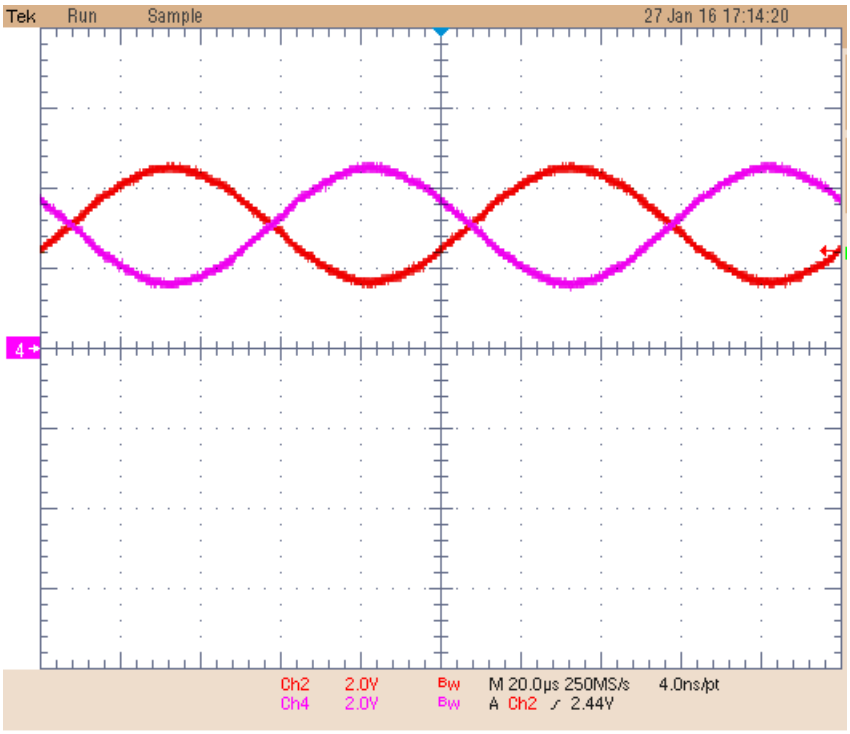


Figure 7. IE1 and IE2 Inputs

The IE1 and IE2 inputs are used as a feedback from the exciter signal path for monitoring and diagnostics of the exciter signal. This exciter monitor circuit is also used by the phase-offset correction circuit for detecting and synchronizing the exciter signal together with the SIN and COS signals in the tracking loop.

Additional Troubleshooting Notes

A.1 FAULTRES Operation

TI recommends to keep FAULTRES low for initial tests on the board. When FAULTRES is connected to GND, the PGA411-Q1 device clears all the faults. When FAULTRES is tied to VIO, no action occurs. When FAULRES is connected back to VIO, all the faults present in the system should appear.

The DEV_STAT1, DEV_STAT3, DEV_STAT4, and DEV_STAT7 registers store the fault information. The registers are cleared when read, therefore, these registers must only be read once. Refer to the data sheet for more information about these registers.

In the GUI designed for the EVM board, when the *FAULTRES* checkbox is checked in the block diagram, the faults can appear in the GUI (see Figure 8). To clear the faults, uncheck the *FAULTRES* checkbox and click the *Update* button (see Figure 9).

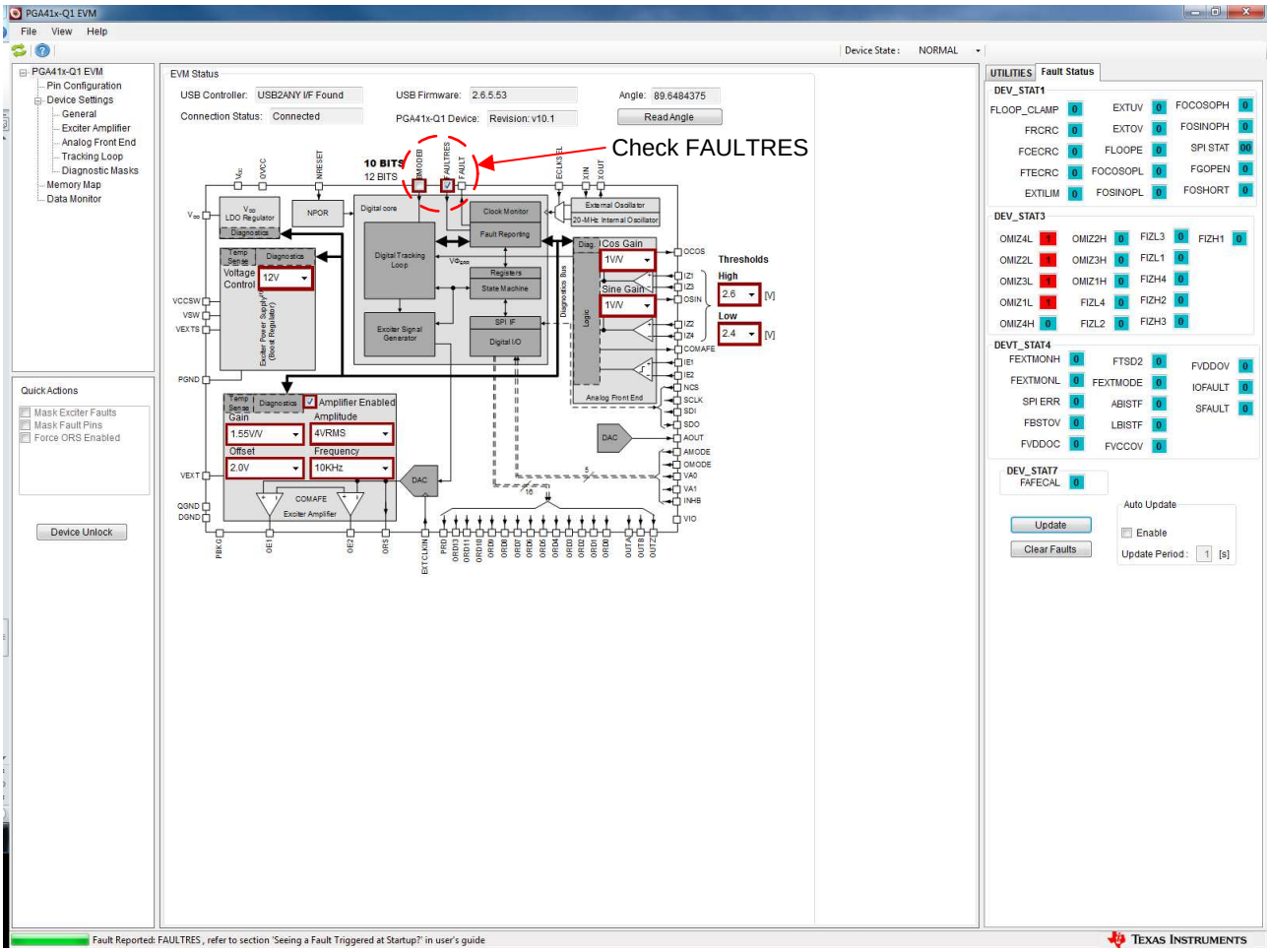


Figure 8. Checked FAULTRES Box in the PGA41x-Q1 EVM GUI

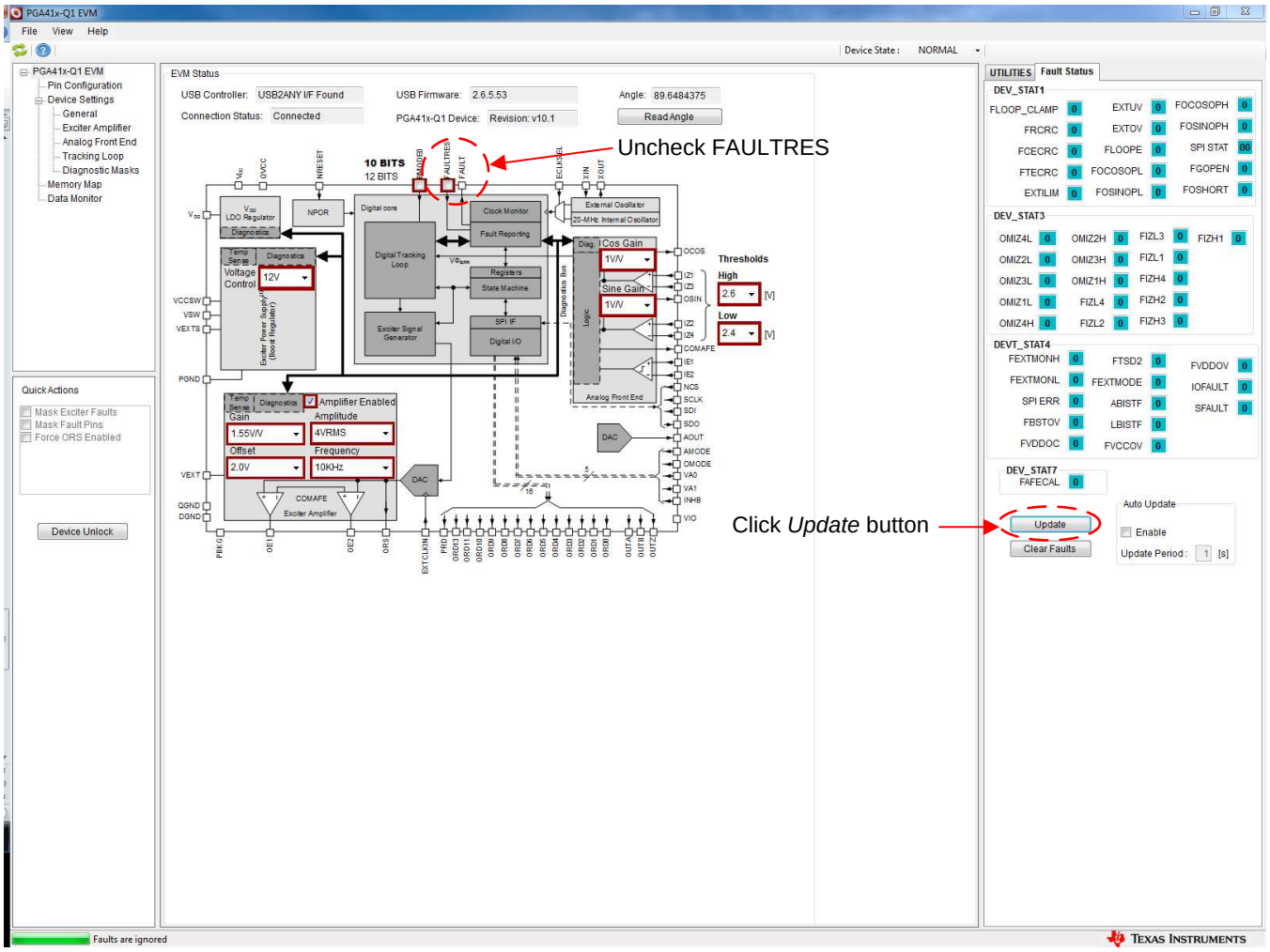


Figure 9. Clearing Faults in the PGA41x-Q1 GUI

A.2 Non-Zero Velocity When Reading from PGA411-Q1

ORDVELOCITY stores the velocity value as the signed 2s compliment with the MSB as the sign based on the resolution selected (bit 9 for 10-bit, or bit 11 for 12-bit). Use the *Calibrate* button as shown in Figure 10 to delete the initial offset from the ORDVELOCITY register.

- 10-bit velocity:

$$\vartheta\,(\text{RPM}) = 60 \times \frac{f_{\text{clk}} \times \text{ORDx}}{2^{21}} \quad (1)$$

where

- where f_{clk} is the device clock frequency (typically 20 MHz)

- 12-bit velocity

$$\vartheta\,(\text{RPM}) = 60 \times \frac{f_{\text{clk}} \times \text{ORDx}}{2^{25}} \quad (2)$$

NOTE: An important takeaway from these velocity calculations is that the minimum change in velocity that can be read is 36 RPM in 12-bit mode and 572 RPM in 10-bit mode.

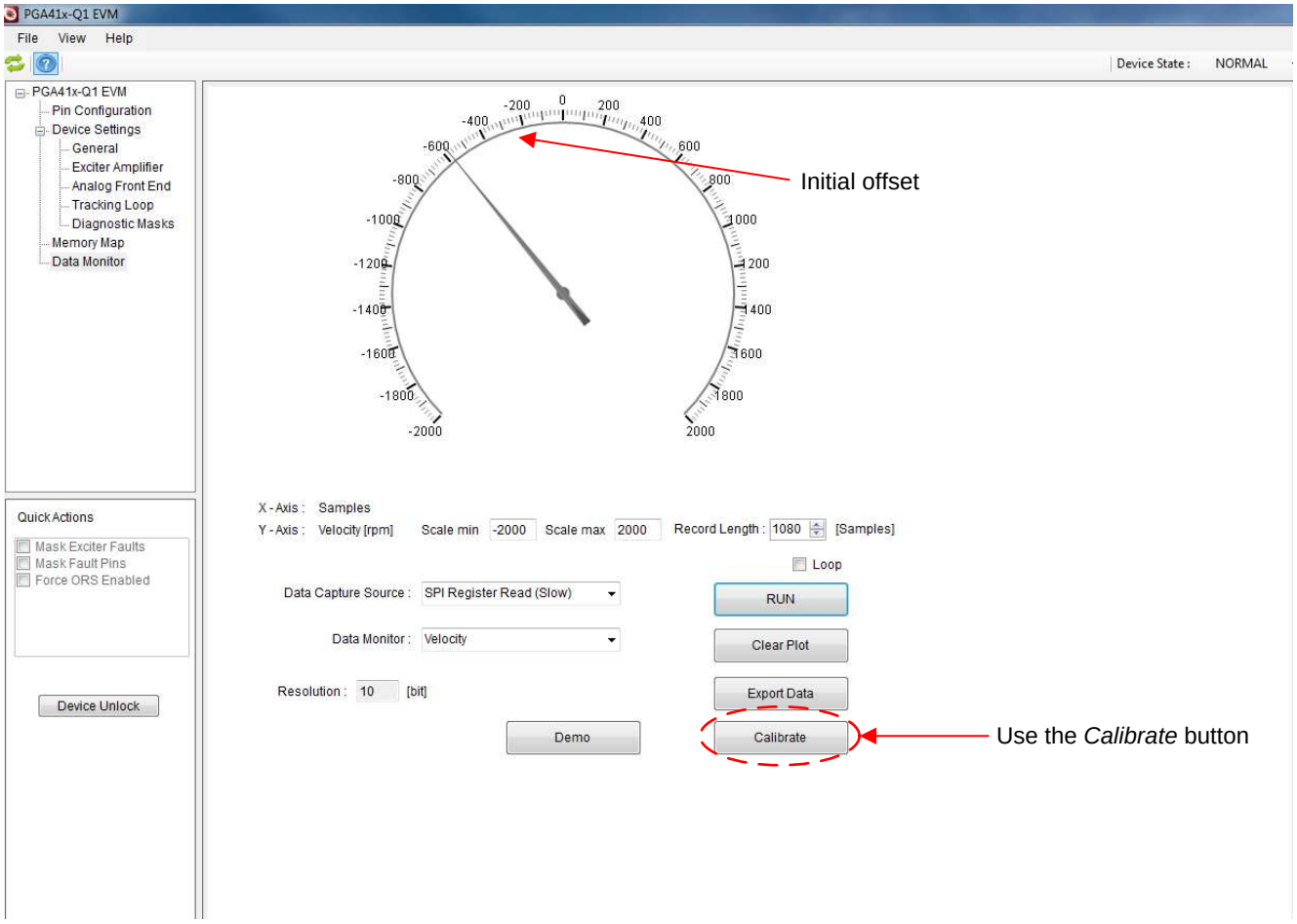


Figure 10. Click *Calibrate* in the PGA41x-Q1 EVM GUI

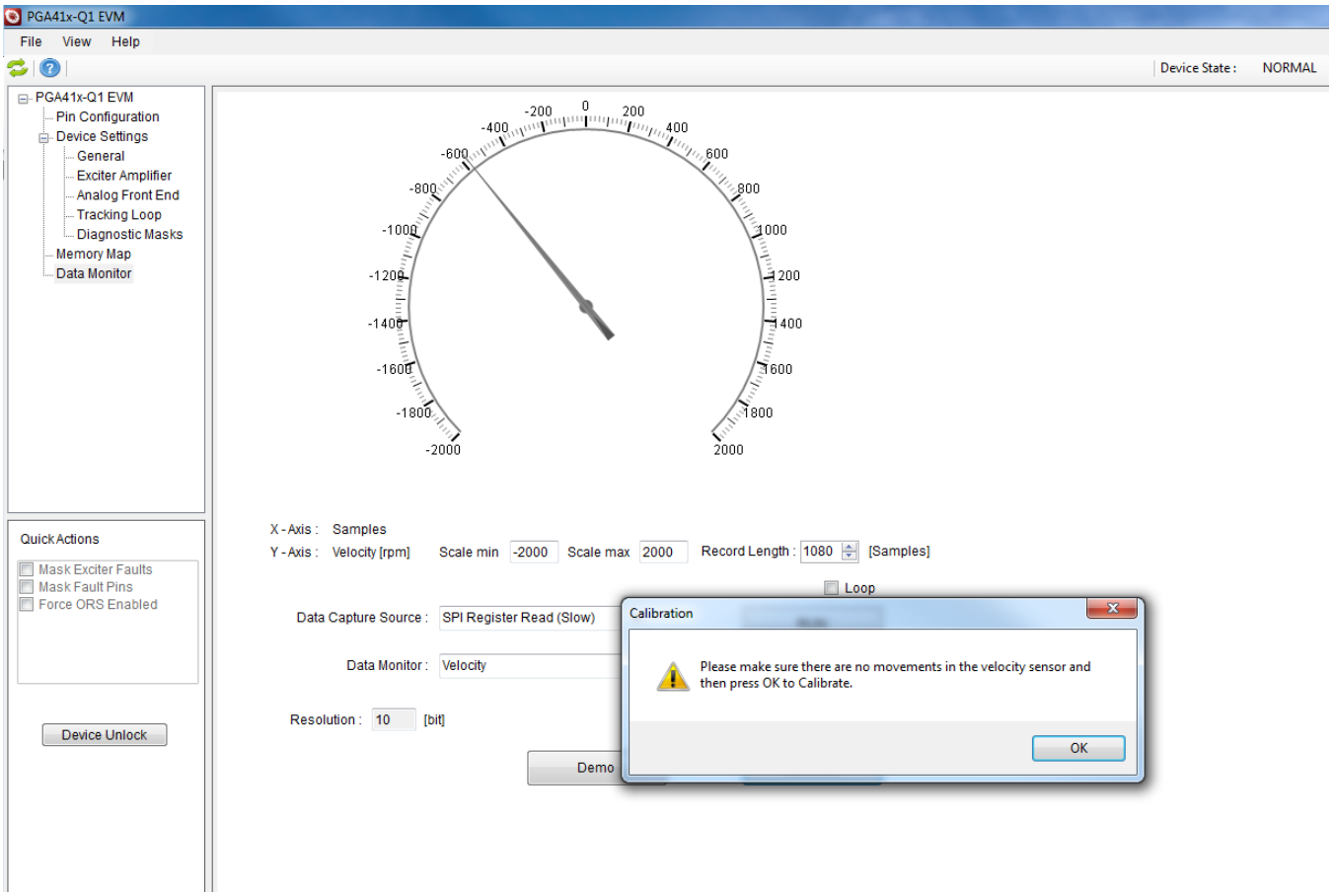


Figure 11. Click on *OK* in the Calibration Window

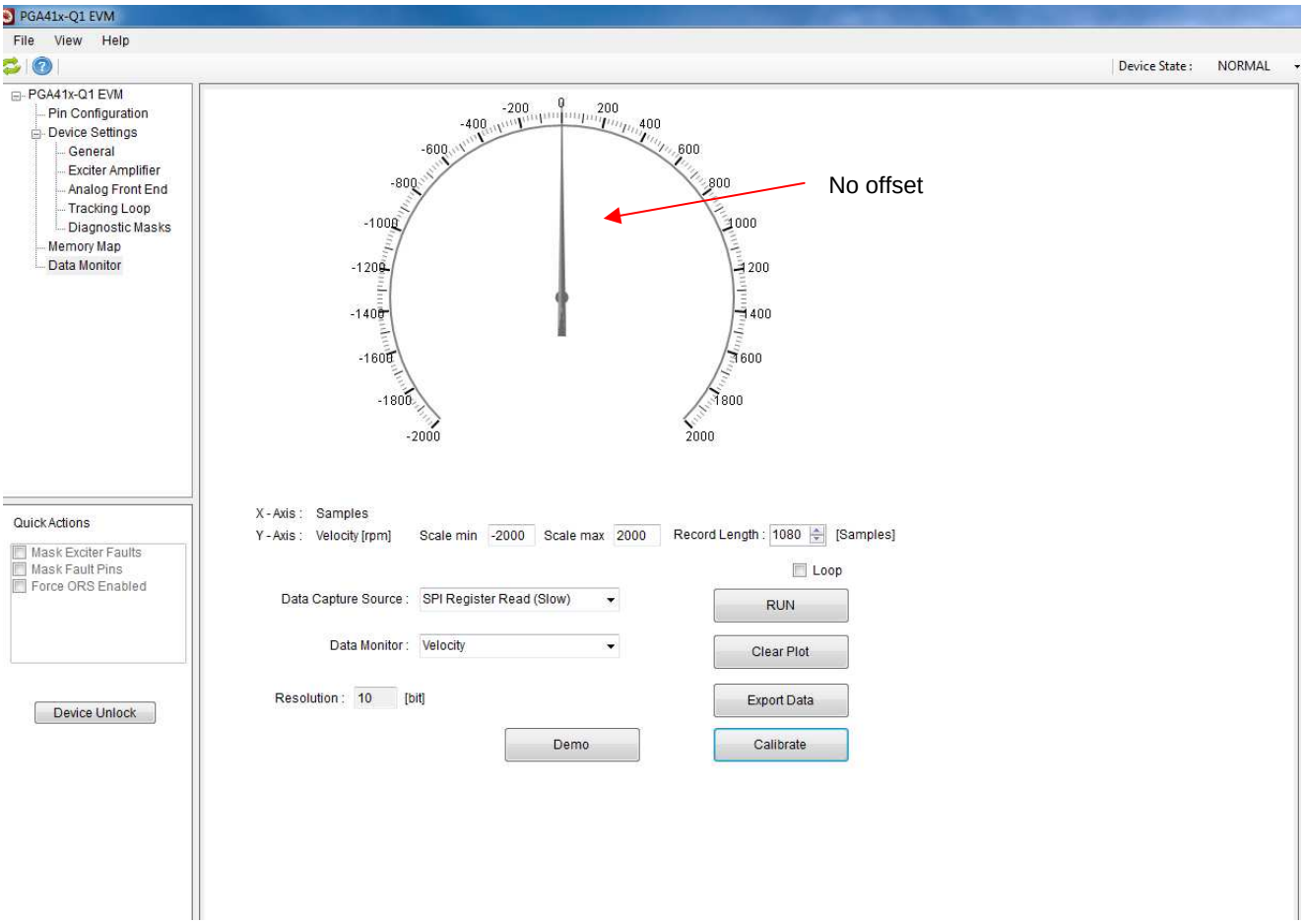


Figure 12. Velocity Displays Zero Value

A.3 How to Clear OMIZx Faults

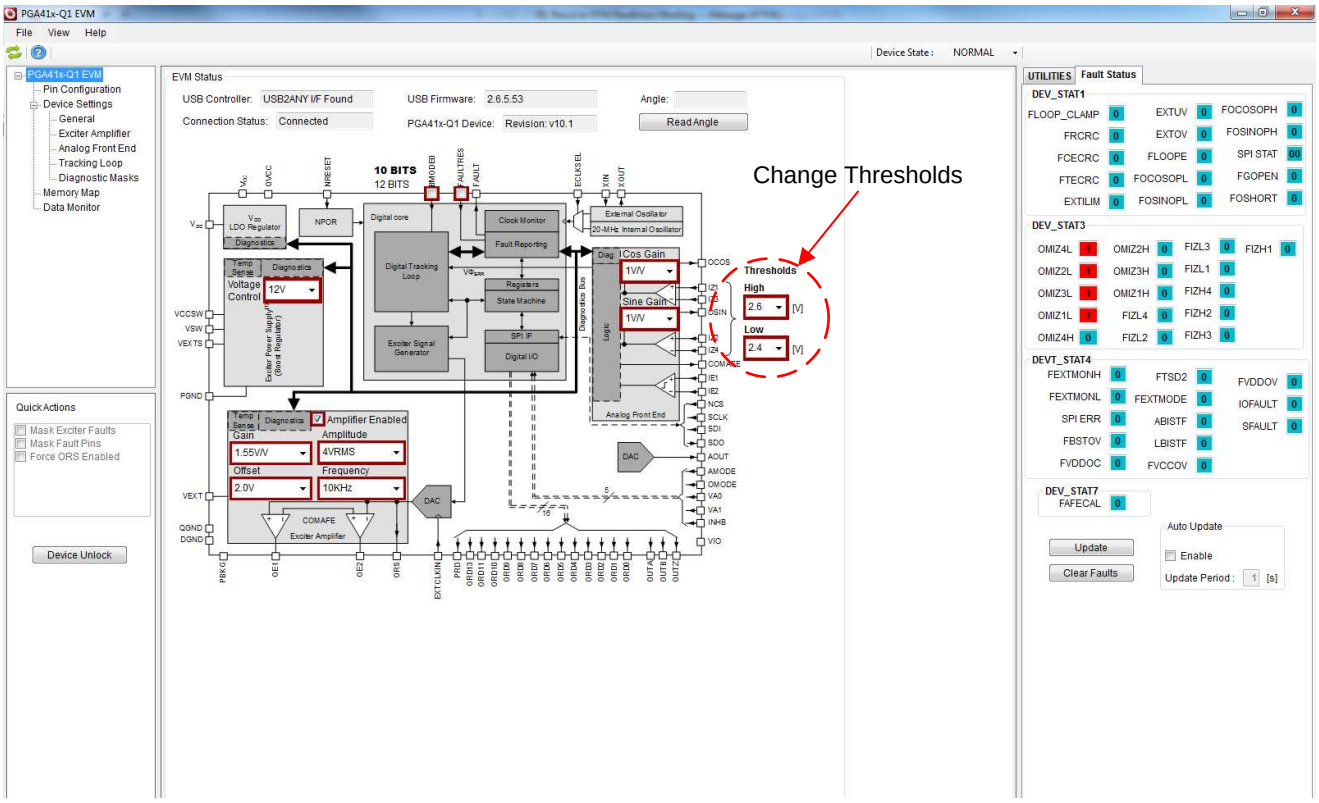


Figure 13. Clearing OMIZx Faults

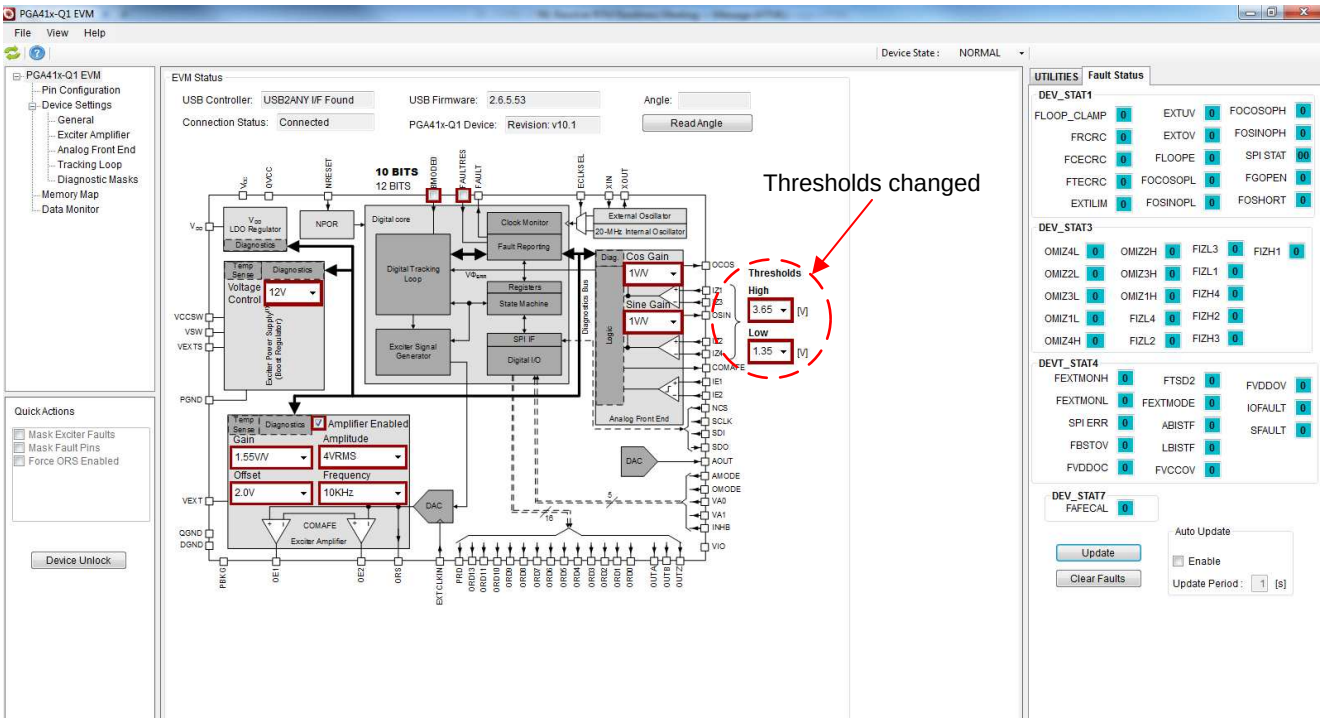


Figure 14. Clearing OMIZx Faults

A.4 Check Resolver Connection

The resolver sensor connects to the blue terminals in Figure 15.

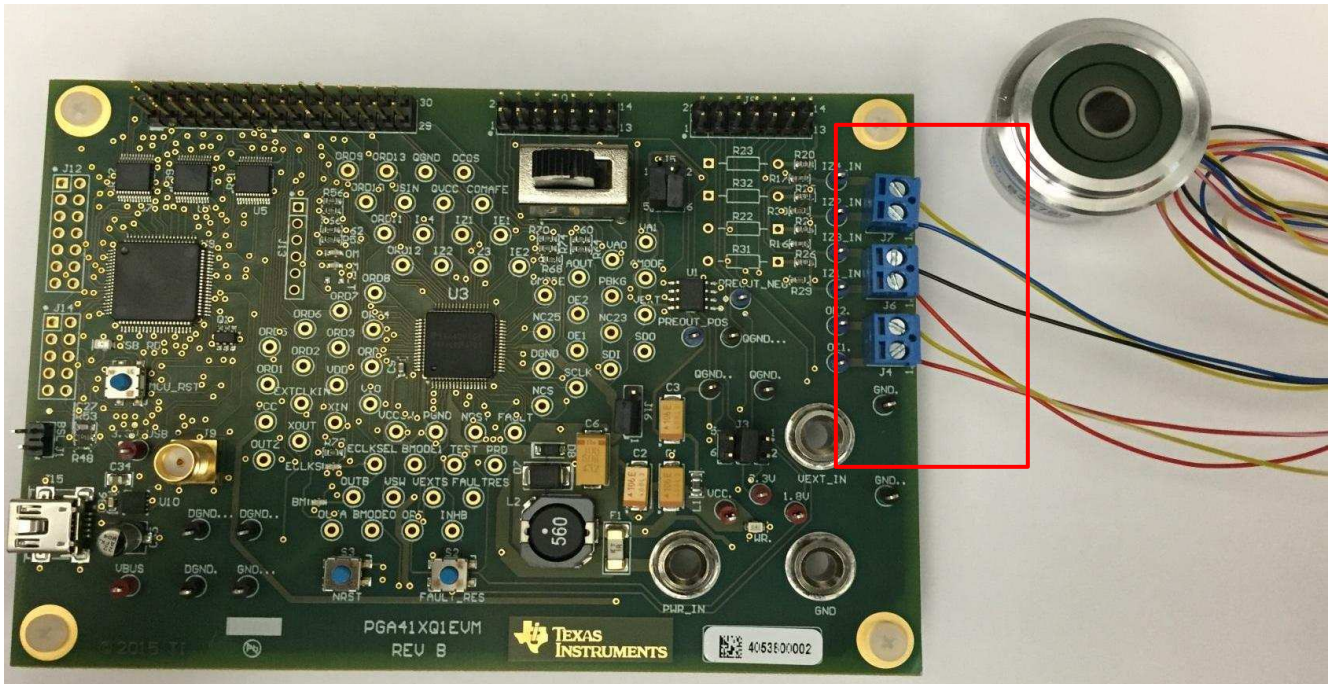


Figure 15. Resolver Sensor Connection

Resolver cabling nomenclature may vary across manufacturers, therefore TI recommends to confirm nomenclature with the resolver data sheet. The most common nomenclature is listed as follows:

IZ4 — Yellow wire

IZ2 — Blue wire

IZ3 — Black wire

IZ1 — Red wire

OE1 — Yellow, striped wire

OE2 — Red, striped wire

A.5 Device Configuration and User EEPROM Section

The CRC check uses a standard CRC-8 (ATM HEC) polynomial, X8 + X2 + X + 1, with an initial seed value 0xFF. The calculation is broken up into 8-bit chunks to optimize implementation with the ordering convention from LS Byte to MS Byte going from LS bit to MS bit.

Table 5. Device Configuration CRC-8 Calculation Examples

192-BIT BUS ORDERING VALUE	CRC-8
0 x 0505050505050505050505050505050505050505050505050505	0xBD
0 x 0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A	0xA9
0 x 53E53E53E53E53E53E53E53E53E53E5353E53E53E53E53E5	0x2C
0 x 4AC4AC4AC4AC4AC4AC4AC4AC4AC4A4AC4AC4AC4AC4AC4	0xAE
0 x 78F78F78F78F78F78F78F78F78F7878F78F78F78F78F7	0x5E

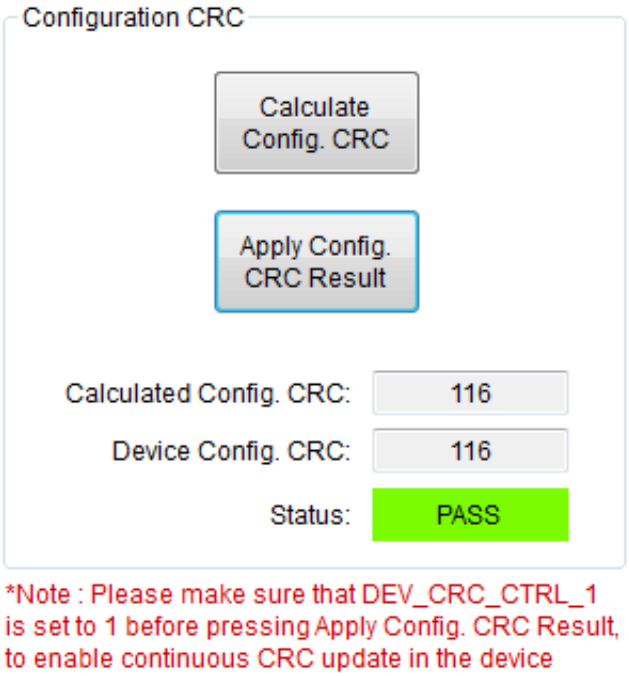


Figure 16. Verifying the Configuration CRC in the EVM GUI

If the calculated value from device configuration and the applied value is identical, the status are indicated as *PASS*. The following is example code to calculate the CRC.

```
   crc_data = {32'h0000_0000,
               EEPROM_val[6][7:0],
               EEPROM_val[5],
               EEPROM_val[4],
               EEPROM_val[3],
               EEPROM_val[2],
               EEPROM_val[1],
               EEPROM_val[0]};


   crc_calc = 8'hff;
   for (i=0; i<17; i=i+1) begin
      crc_byte = crc_data[7:0];
      crc_calc = nextCRC8_D8(crc_byte, crc_calc);
      crc_data = crc_data >> 8;
   end


// 8-bit CRC
   // polynomial: (0 1 2 8)
   // data width: 8
   // convention: the first serial data bit is D[7]
   function [7:0] nextCRC8_D8;
      input [7:0] Data;
      input [7:0] CRC;
      reg [7:0] D;
      reg [7:0] C;
      begin
                  D = Data;
                  C = CRC;
                  nextCRC8_D8[0] = D[7] ^ D[6] ^ D[0] ^ C[0] ^ C[6] ^ C[7];
                  nextCRC8_D8[1] = D[6] ^ D[1] ^ D[0] ^ C[0] ^ C[1] ^ C[6];
```

```
                nextCRC8_D8[2] = D[6] ^ D[2] ^ D[1] ^ D[0] ^ C[0] ^ C[1] ^ C[2] ^ C[6];
                nextCRC8_D8[3] = D[7] ^ D[3] ^ D[2] ^ D[1] ^ C[1] ^ C[2] ^ C[3] ^ C[7];
                nextCRC8_D8[4] = D[4] ^ D[3] ^ D[2] ^ C[2] ^ C[3] ^ C[4];
                nextCRC8_D8[5] = D[5] ^ D[4] ^ D[3] ^ C[3] ^ C[4] ^ C[5];
                nextCRC8_D8[6] = D[6] ^ D[5] ^ D[4] ^ C[4] ^ C[5] ^ C[6];
                nextCRC8_D8[7] = D[7] ^ D[6] ^ D[5] ^ C[5] ^ C[6] ^ C[7];
    end
endfunction
```

Table 6. User EEPROM CRC Bus Order

USER EEPROM REGISTER		136-BIT BUS ORDERING
NAME	DATA SPLIT	
	0s Pad [31:0]	[MSB] 135:104
DEV_CONFIG1	DEV_CONFIG1 [7:0]	103:96
DEV_OVUV5	DEV_OVUV5 [12:10]	95:93
DEV_AFE_CFG	DEV_AFE_CFG [3:0]	92:89
DEV_OVUV2	DEV_OVUV2 [8:0]	88:80
DEV_OVUV4	DEV_OVUV4 [10:5]	79:74
DEV_OVUV6	DEV_OVUV6 [9:0]	73:64
DEV_OVUV4	DEV_OVUV4 [4:0]	63:59
DEV_TLOOP_CFG	DEV_TLOOP_CFG [10:0]	58:48
DEV_PHASE_CFG	DEV_PHASE_CFG [15:0]	47:32
DEV_OVUV1	DEV_OVUV1 [15:0]	31:16
DEV_OVUV3	DEV_OVUV3 [15:0]	15:0 [LSB]

Table 7. Configuration CRC Data Bus Order

REGISTER		192-BIT BUS ORDERING
NAME	DATA SPLIT	
DEV_OVUV1	DEV_OVUV1 [15:0]	[MSB] 191:176
DEV_OVUV2	0s pad [15:9]	175:169
	DEV_OVUV2 [8:0]	168:160
DEV_OVUV3	DEV_OVUV3 [15:0]	159:144
DEV_OVUV4	0s pad [15:11]	143:139
	DEV_OVUV4 [10:0]	138:128
DEV_OVUV5	0s pad [15:13]	127:125
	DEV_OVUV5 [12:10]	124:122
	0s pad [9:0]	121:112
DEV_OVUV6	0s pad [15:10]	111:106
	DEV_OVUV6 [9:0]	105:96
DEV_TLOOP_CFG	0s pad [15:11]	95:91
	DEV_TLOOP_CFG [10:0]	90:80
DEV_AFE_CFG	0s pad [15:4]	79:68
	DEV_AFE_CFG [3:0]	67:64
DEV_PHASE_CFG	DEV_PHASE_CFG [15:0]	63:48
DEV_CONFIG1	0s pad [15:9]	47:41
	DEV_CONFIG1 [8:7]	40:39
	0s pad [6]	38
	DEV_CONFIG1 [5:0]	37:32

Table 7. Configuration CRC Data Bus Order (continued)

REGISTER		192-BIT BUS ORDERING
NAME	DATA SPLIT	
DEV_CONTROL1	0s pad [15:14]	31:30
	DEV_CONTROL1 [13]	29
	0s pad [12]	28
	DEV_CONTROL1 [11:0]	27:16
DEV_CONTROL2	0s pad [15:6]	15:6
	DEV_CONTROL2 [5:0]	5:0 [LSB]

A.6 Exciter Amplifier

Figure 17 shows the section for exciter amplifier.

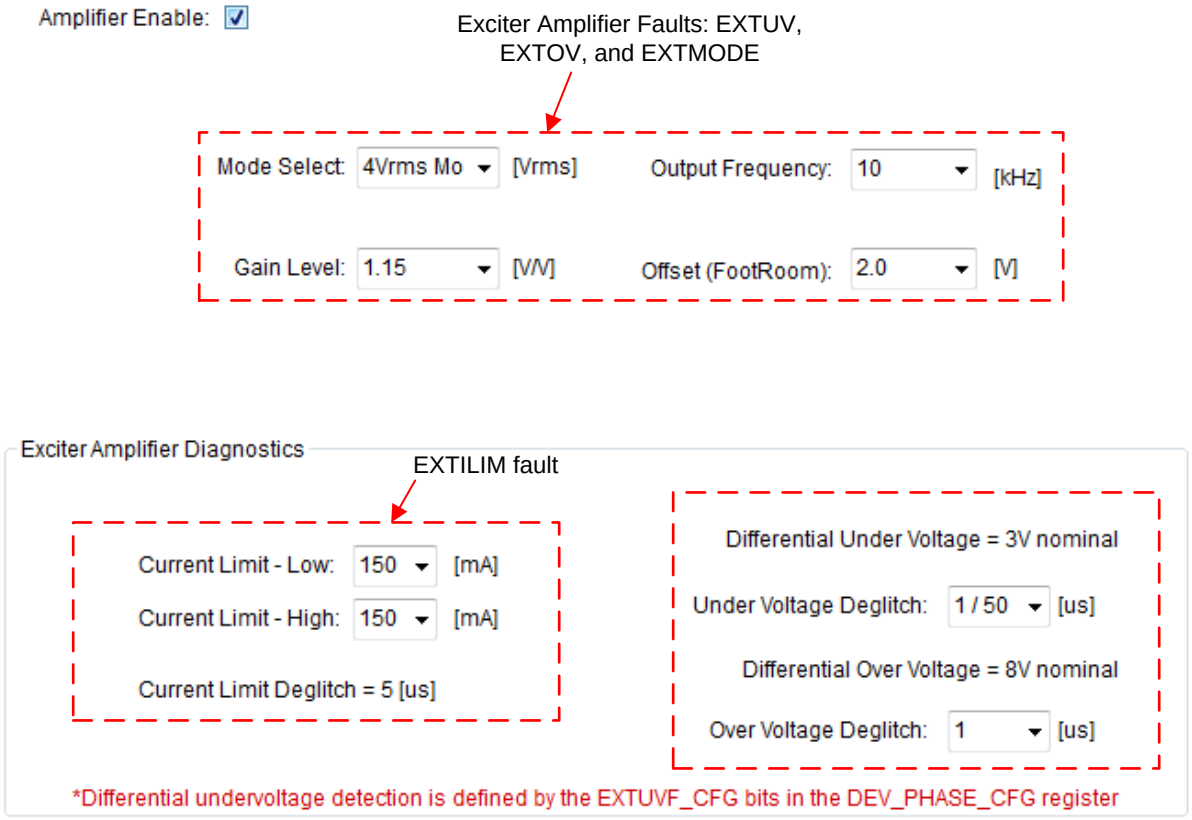


Figure 17. Exciter Amplifier Section in the EVM GUI

A.7 Analog Front End (AFE) Diagnostics Section

Figure 18 shows the section for the AFE diagnostics.

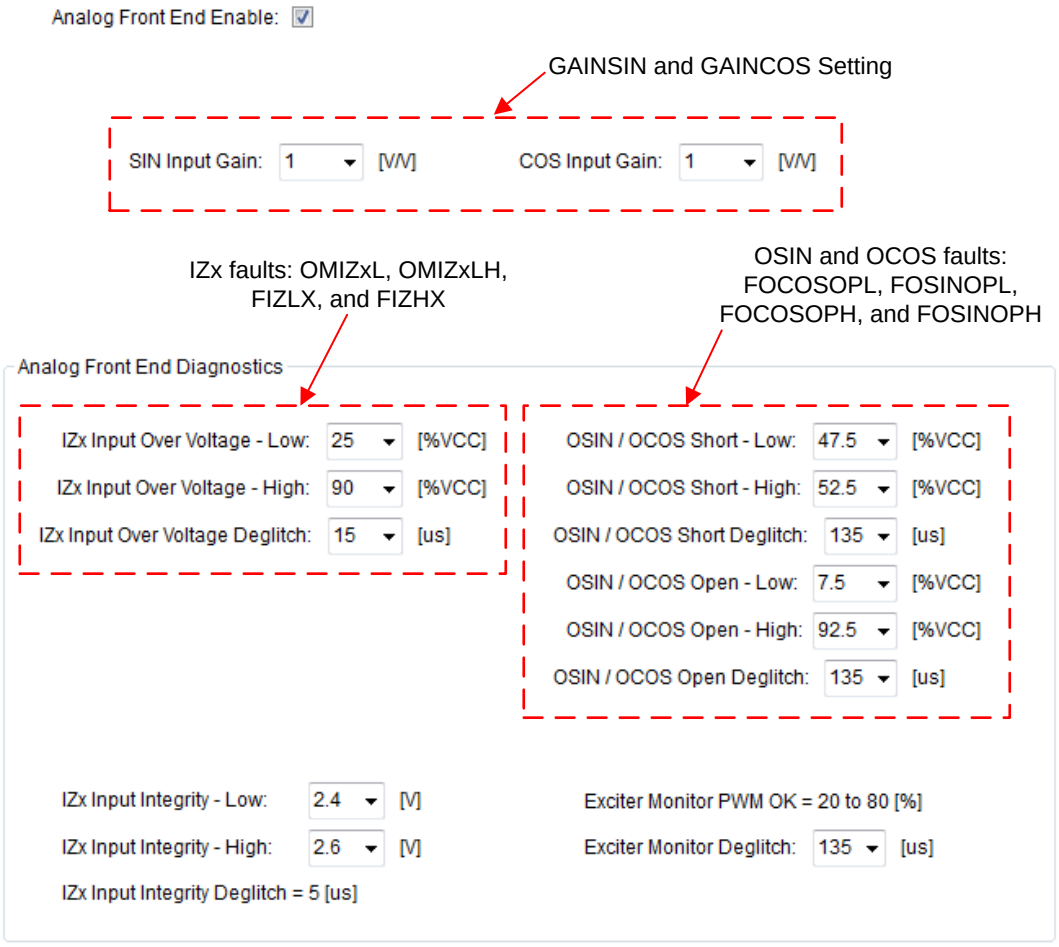


Figure 18. Analog Front End (AFE) Diagnostics in the EVM GUI

A.8 Tracking Loop Diagnostics

Figure 19 shows the tracking loop diagnostics.

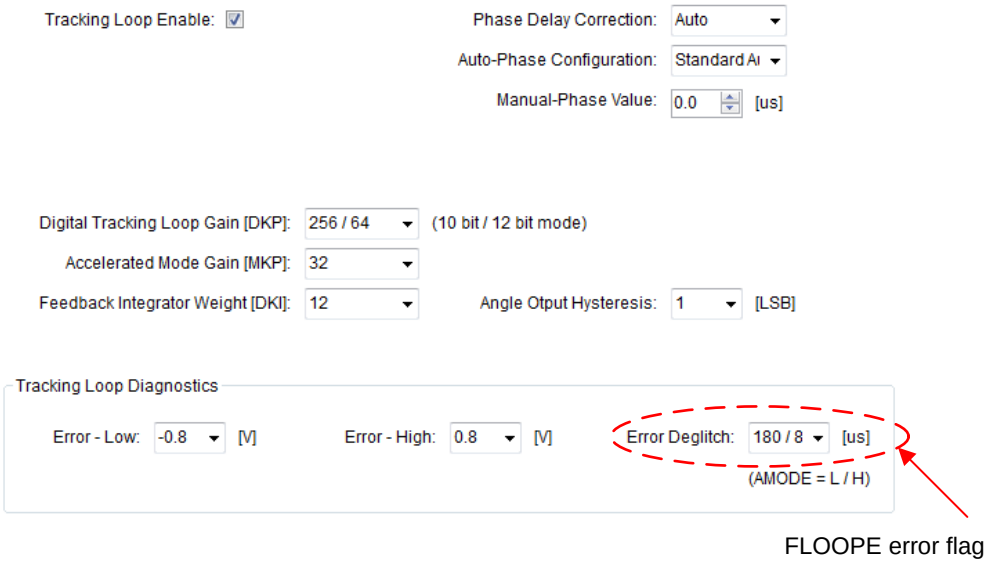


Figure 19. Tracking Loop Diagnostics

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